University of Toronto
Faculty of Applied Science and Engineering
Final Examination

ECE 241S - Digital Systems 2003
Examiner: Belinda Wang, Jianwen Zhu

Duration: 2.5 Hours

ANSWER QUESTIONS ON THESE SHEETS, USING THE BACKS IF NECESSARY.

1. No calculator is allowed.
2. Weight for each question is indicated in []. Attempt all questions, since a blank sheet will certainly get a zero.

Last Name: _____

First Name: _____

Student Number: _____

Lecture Section:

Section 01 (Zhu) [ ]

Section 02 (Wang) [ ]

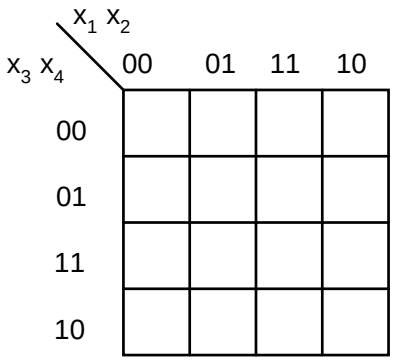
Maximum grade = 100

Question	Mark
1	
2	
3	
4	
5	
6	
7	
8	
Total	

Problem 1 [20] A 2-bit digital output of each of two sensors along an assembly line conveyor belt is proportional to the number of parts that pass by on the conveyor belt in a 30-s period. Design a logic circuit that reports an error if the outputs of the two sensors differ by more than one part per 30-s period.

1. Develop a truth table.

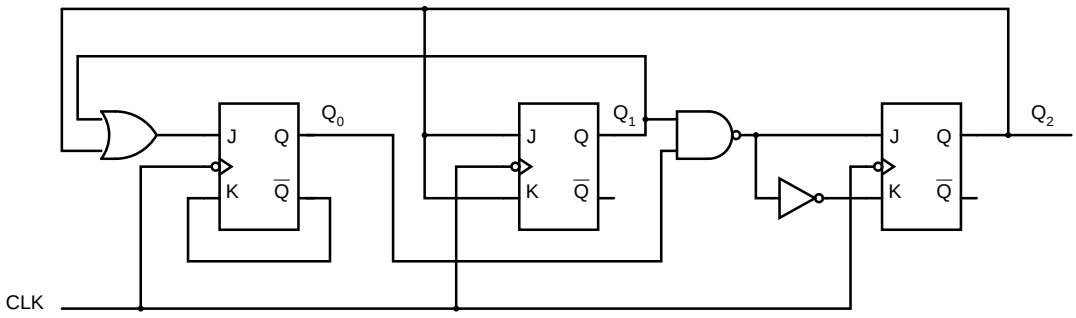
2. Express the error function (f) in SOP form by making use of a K-map.



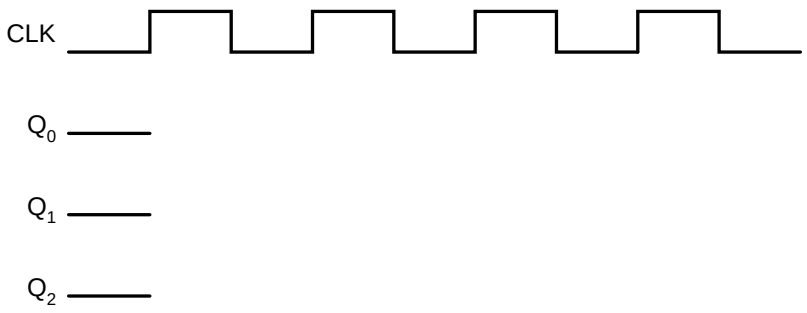
$f =$

3. Use only 4-to-2 and/or 2-to-1 multiplexers, but as fewer as possible to implement the error function f.

Problem 2 [5] Flip-flop and counters.



Draw a timing diagram (four complete clock cycles) for Q_0, Q_1 and Q_2. Assume that all initial values are 0. Note that all flip-flops are negative edge-triggered.



Problem 3 [25] Given the state table as follows.

Present State	Next State/Z	
	x = 0	x= 1
A	B/0	G/0
B	B/1	H/1
C	F/1	D/0
D	B/0	H/0
E	F/1	D/0
F	F/0	C/1
G	E/0	A/0
H	E/0	A/0

1. Obtain a minimal reduced state table (letting new state A be the block in which the old state A appears and so on).

2. Draw the equivalent state diagram using the reduced states.

3. For the following input sequence (X) with the machine initially in state A, determine the resulting output sequence.

X: 1 0 0 1 1 1 0 1 0 1 1 0 0 1

Z:

4. Draw the state-assignment table.

5. Determine the minimum-cost expression for all next state variables and the output (Z).

Problem 4 [10] A synchronous sequential circuit has two input lines, x_1 and x_2, an output line, Z. The data line is x_1 and x_2 is reset line. Whenever $x_2 = 1$, the circuit is reset. When x_2 becomes 0, the first 4 bits on the data line constitute a message word. The output is to become 1 if the message received is 1010. At the end of the fourth bit of any word received when $x_2 = 0$, the circuit is to enter a waiting state, where it remains until it is reset and where the output is 0 for any input bits after the fourth bit.

1. Construct an ASM chart.

2. Construct an equivalent state diagram.