University of Toronto
Faculty of Applied Science and Engineering
Final Examination

ECE 241S - Digital Systems
Examiner: Belinda Wang, Jianwen Zhu

2:00 - 4:30pm, April 26th, 2004
Duration: 150 minutes (2.5 hours)

ANSWER QUESTIONS ON THESE SHEETS, USING THE BACKS IF NECESSARY.

1. No calculator is allowed.

2. Weight for each question is indicated in []. Attempt all questions, since a blank sheet will certainly get a zero.

Last Name: _____

**First Name:** _____

Student Number: _____

Lecture Section:

    Section 01 (Zhu)   [ ]

    Section 02 (Wang) [ ]

Maximum grade = 100

| Question	Mark
1	
2	
3	
4	
5	
6	
7	
Total	

Problem 1 [20 marks]

We want to build a NAND gate circuit to compute the parity of an n-bit unsigned number. The parity is defined as 1 if and only if there are an odd number of 1's in the number. One way of doing this is to build the circuit 1 bit at a time (as in the adder), such that the circuit computes the parity after that bit as a function of the parity up to that bit and the one input bit. A block diagram of the first few bits of such circuit is shown below.
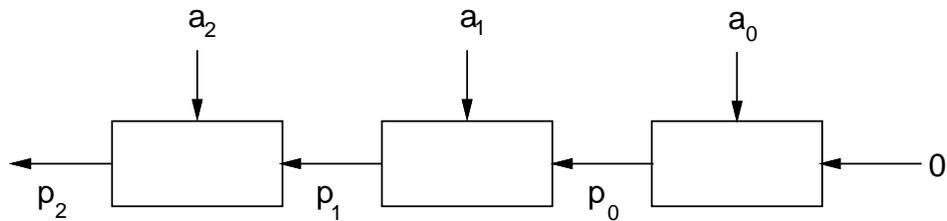
(a) **[8]** Show an NAND gate circuit to implement 1 bit and compute the delay of n bits. Assume that the delay for an NAND is $1+0.1*(\#$ of inputs) ns.

(b) **[12]** Reduce the delay by implementing 2 bits at a time as shown below. Draw the NAND gate circuit. Compute the delay for n bits in this case.

$$
\begin{array}{ccc}
 & a \quad b & \\
 & \downarrow \quad \downarrow & \\
p_{out} \longleftarrow & \boxed{} & \longleftarrow p_{in}
\end{array}
$$
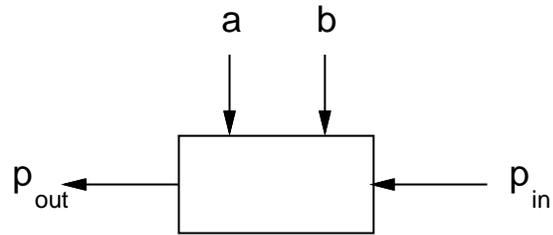
Problem 2 [20 marks]

Consider the three functions, the K-map of which are given below. You have available as components, OR gates and 2-to-4 decoders (as shown in the diagram below). Write down the logic expressions (in the forms that can be implemented using the given components) and draw the circuit diagrams for all three functions (highest mark will be given to those designs with fewer decoders, gates and minimal number of inputs to the gates).

$\frac{wx}{yz}$	00	01	11	10
00				1
01	1	1		
11	1	1	1	1
10	1	1		1

f

$\frac{wx}{yz}$	00	01	11	10
00		1	1	1
01				
11			1	
10	1	1	1	

g

$\frac{wx}{yz}$	00	01	11	10
00		1		1
01	1	1		
11	1	1	1	
10		1		

h

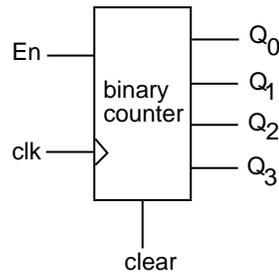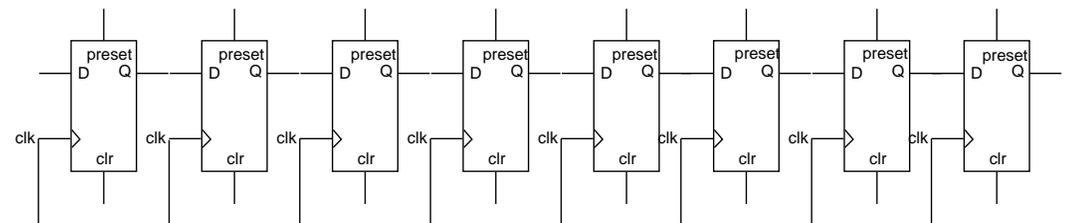2-to-4 decoder with inputs a, b, Enable, and outputs y_0, y_1, y_2, y_3.
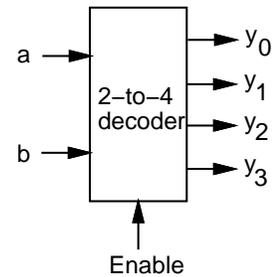
Problem 3 [10 marks]

Design a system that has an output (z) of 1 when input (x) has been 0 for exactly seven clock cycles. In addition to combinational logic gates, one of the following component is available:

(a) **[5]** A 4-bit counter (with asynchronous clear)

(b) **[5]** An 8-bit shift register (with asynchronous preset and clear)

Problem 4 [15 marks]

You are building an adder to add the 32-bit constant (10101010101010101010101010101010) to an arbitrary 32-bit number. You can implement this with 16 identical adder modules, each of which will add 2 bits of the number to the constant (10) and a carry from the previous lower pair of bits and produce 2 bits of the sum and the carry to the next pair. A block diagram of part of the design is shown below:
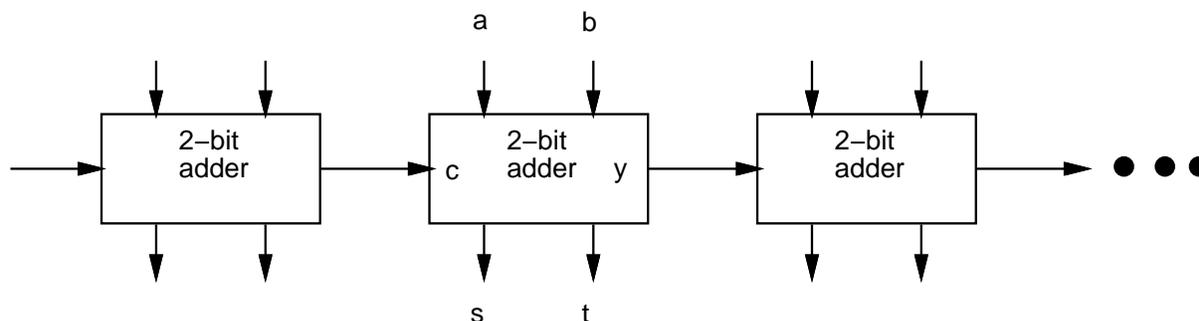
The problem each 2-bit adder solve is:

$$\begin{array}{ccc} & & c \\ a & b \\ + & 1 & 0 \\ \hline y & s & t \end{array}$$

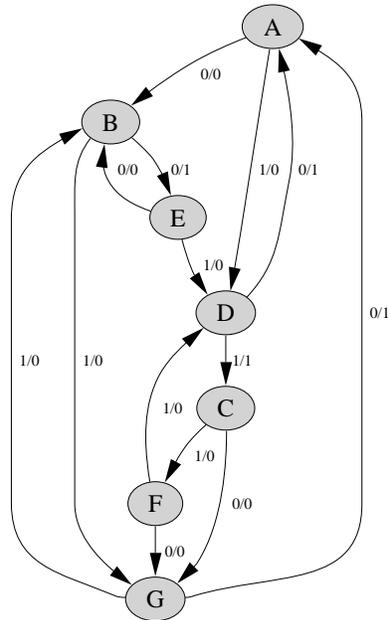(a) **[7]** Show a truth table for the 2-bit adder (It has three inputs: a, b, c; three outputs: y, s, and t.)

(b) **[6]** Write the minimum cost expressions for all outputs (y, s and t), if only NOR gates are available for implementation.

(c) **[2]** Assume each NOR gate has an 1 ns delay, compute the delay from the c input of each module to the y output of the module and the total delay for the 32 bits (from c_0 to y_{31})

Problem 5 [20 marks]

Consider a sequential system with a single input *w* and single out *z*. The state diagram of the system is shown below.

(a) **[3]** Draw the state table of the sequential system.

(b) **[6]** Reduce the system to one with the minimum number of states, and draw the reduced state table.

(c) **[3]** Draw the state diagram of (b).

(d) **[3]** Given the following input pattern(x), fill out the expected output pattern (z). Assume that you start at state A.

| x	0	1	1	1	0	0	1	1	0	1	1	1	1	0
z														

Problem 6 [5 marks]

Consider a sequential system with a single input w and single out z. The state diagram of the system is shown below.
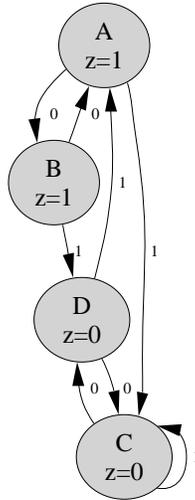
Design a sequential circuit using **one-hot encoding**. Draw the circuit diagram below.

Problem 7 [15 marks]

Imagine it is your first day in a hot startup company in silicon valley called *ZINI* (an acronym for Zini Is Not Intel). Your manager, Dr. Build Gates, is a well-known architect in chip design. Dr. Gates asked you to design a critical component in a new microprocessor, called the **page manager**, whose specification is shown below.
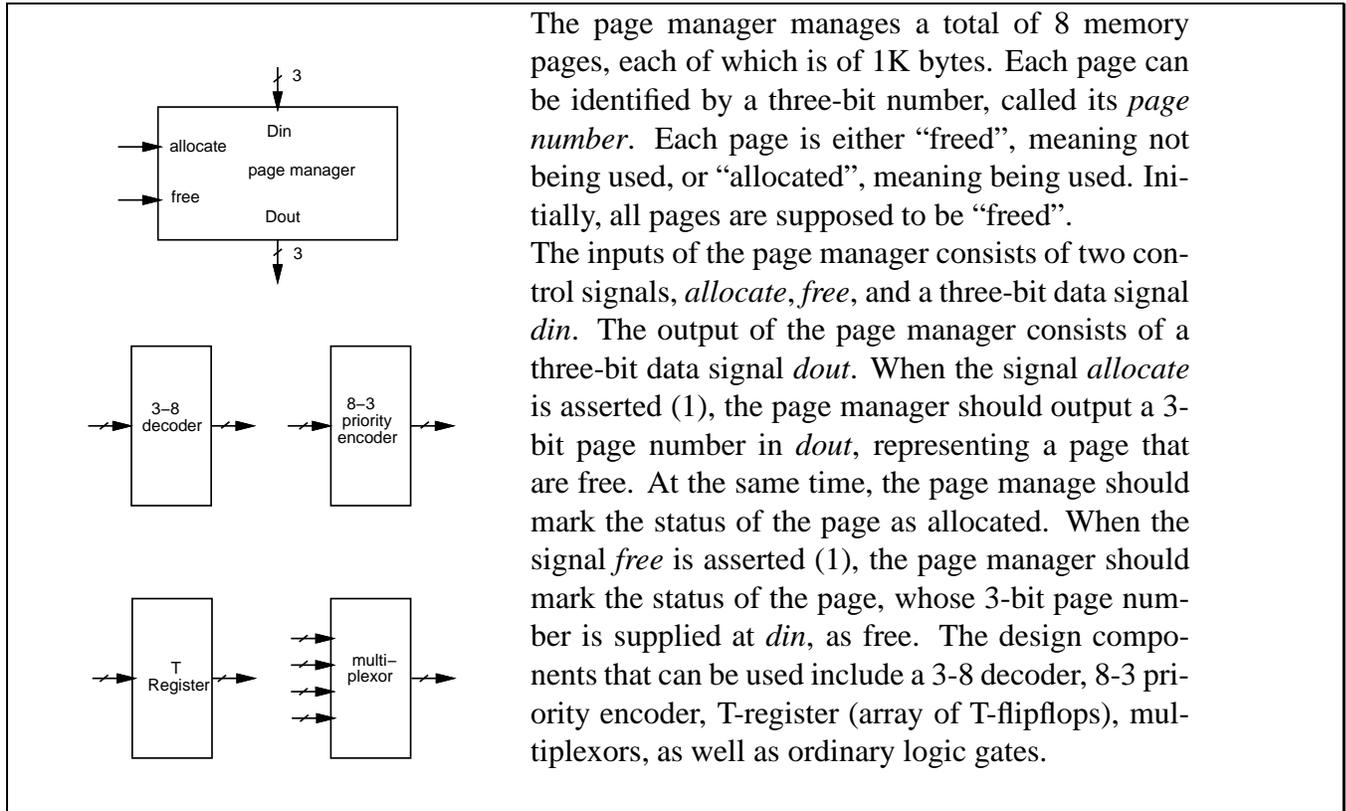
The page manager manages a total of 8 memory pages, each of which is of 1K bytes. Each page can be identified by a three-bit number, called its *page number*. Each page is either "freed", meaning not being used, or "allocated", meaning being used. Initially, all pages are supposed to be "freed".

The inputs of the page manager consists of two control signals, *allocate*, *free*, and a three-bit data signal *din*. The output of the page manager consists of a three-bit data signal *dout*. When the signal *allocate* is asserted (1), the page manager should output a 3-bit page number in *dout*, representing a page that are free. At the same time, the page manage should mark the status of the page as allocated. When the signal *free* is asserted (1), the page manager should mark the status of the page, whose 3-bit page number is supplied at *din*, as free. The design components that can be used include a 3-8 decoder, 8-3 priority encoder, T-register (array of T-flipflops), multiplexors, as well as ordinary logic gates.

(a) **[5]** Show the truth-table of a priority encoder, Assume the inputs are $D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0$ and the outputs are A_2, A_1, A_0.

[10] Draw the circuit diagram of the page manager you designed.