

**University of Toronto**  
**Faculty of Applied Science and Engineering**  
**Midterm Examination**

ECE 241S - Digital Systems  
Examiner: Belinda Wang, Jianwen Zhu

February 27th, 2002  
Duration: 90 minutes

ANSWER QUESTIONS ON THESE SHEETS, USING THE BACKS IF NECESSARY.

1. No calculator is allowed.
2. Weight for each question is indicated in []. Attempt all questions, since a blank sheet will certainly get a zero.

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**Last Name:** \_\_\_\_\_

**Maximum grade = 100**

**First Name:** \_\_\_\_\_

**Student Number:** \_\_\_\_\_

**Lecture Section:**

Section 01 (Zhu) [ ]

Section 02 (Wang) [ ]

Question	Mark
1	
2	
3	
4	
5	
6	
Total	

**Problem 1** [20 marks] Circle T (for True) or F (for False) in statement below.

**IMPORTANT NOTE:** For each question, right answer gets “2”, wrong answer gets “-2”, no answer (no circle) gets “0”.

**T F** The following are all valid representations of Boolean function.

- Truth table
- Karnaugh map
- Venn diagram
- Timing diagram
- Sum-of-product Boolean expression

**T F** Any Boolean function can be implemented exclusively by NAND gates.

**T F** Any Boolean function can be expressed as the sum of its essential prime implicants.

**T F**  $(00011010)_2 = (32)_8 = (1B)_{16} = (26)_{10}$

**T F** For a complex logic function, a multi-level implementation is often favored over two-level implementation due to its lower cost.

**T F** Any logic function can be implemented by a multi-level network of multiplexors.

**T F** In CMOS technology, a 2-input AND gate is faster than a 2-input NAND gate, provided that all transistors have equal sizes.

**T F** For any Boolean function  $f$ , there exists one and only one optimal PLA implementation.

**T F** The pull-down network of a CMOS gate can be implemented by PMOS transistors equally well as the NMOS transistors.

**T F** A multi-level logic circuit can be improved by applying logic transformations such as functional decomposition and factoring.

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**Problem 2** [10 marks] Reduce the following Boolean expressions to the indicated number of literals.

(1)  $\overline{\overline{A} \overline{B} + C} + C + AB + CD$  (to three literals). [5 marks]

(2)  $\overline{A}B(\overline{D} + \overline{C}D) + B(A + \overline{A}CD)$  (to one literal). [5 marks]

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**Problem 3** [15 marks] Obtain the truth table of the function  $f$  and express  $f$  in canonical sum-of-product (sum-of-minterm) and canonical product-of-sum (product-of-maxterm) forms.

$$f = (x_1x_2 + x_3)(x_2 + x_1x_3)$$

(1) Truth table. [5 marks]

(2) Sum-of-minterm form. [5 marks]

(3) Product-of-maxterm form. [5 marks]

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**Problem 4** [20 marks] Given the Boolean function

$$f = x_1\bar{x}_2x_3 + \bar{x}_1\bar{x}_2x_3 + \bar{x}_4x_1x_2 + x_4\bar{x}_1x_2 + x_4x_1x_2$$

(1) Obtain the K-map of the function. [5 marks]

(2) Simplify the function to a minimal number of literals. [5 marks]

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(4) Show the logic diagram from the simplified expression, assuming for all  $i$ , both  $x_i$  and  $\bar{x}_i$  are available as the primary inputs. [5 marks]

(4) Evaluate the cost of the logic diagram in (3). [5 marks]

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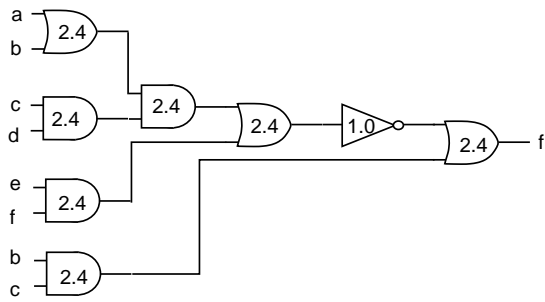
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**Problem 5** [15 marks]

- (1) Show the implementation of a CMOS gate  $Y = \overline{A\bar{B}C + (C + D)\bar{E}}$  as a network of NMOS and PMOS transistors. Identify the pull-up network and pull-down network. [5 marks]

- (2) Assuming all transistors have the same size, How does the delay of an gate in (1) compared to the delay of an inverter? State your reason. [5 marks]

(3) For the following logic diagram, where each gate is labeled with its delay, calculate the total delay from primary inputs to primary outputs  $f$ . [5 marks]





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**Problem 6** [20 marks]

Implement a logic circuit that can detect whether a binary coded decimal (BCD) digit (from 0 to 9), which can be represented by the four Boolean variables  $x_1, x_2, x_3, x_4$ , is a prime number. Note that a prime number is a number that can only be factored as a product of 1 and itself. Also note that 0 and 1 are not considered prime numbers.

(1) Obtain the K-map of the circuit. [5 marks]

(2) Obtain the simplified Boolean expression. [10 marks]

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- (3) Implement the simplified Boolean expression using NOR gates, assuming for all  $i$ , both  $x_i$  and  $\bar{x}_i$  are available as primary inputs. [5 marks]