University of Toronto

Faculty of Applied Science and Engineering

Midterm Examination

ECE 241F - Digital Systems
Wednesday October 15, 2003, 6:00pm

Duration: 90 minutes
Examiners: J. Rose and B. Wang

ANSWER ALL QUESTIONS ON THESE SHEETS, USING THE BACK SIDE IF NECESSARY.
1. No calculator is allowed.
2. The number of marks available for each question is indicated in the square brackets [].
3. There are two extra blank pages at the end of the test for rough work.

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Last Name: _____

First Name: _____

Student Number: _____

Lecture Section: **Section 01 (Rose) [ ]**
Section 02 (Wang) [ ]

Total Available Marks: 71

Question	1	2	3	4	5	6	7	8	9	10	11	Total
Marks Available	5	10	3	7	10	6	5	5	10	5	5	71
Marks Achieved												

[5] Q1. Is the following Boolean equality correct? Answer yes or no, and then use Boolean algebra to prove or disprove it.

$$\bar{x}y + \bar{y}z + y\bar{z} = \bar{x}z + \bar{y}z + y\bar{z}$$

Circle Answer: YES NO

Provide Algebraic steps that prove your answer:

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[10] Q2. Using **only 2-input NOR gates**, give the circuit diagram for the function:

$$f = \overline{x_1}x_2 + x_1x_3 + \overline{x_1}\,\overline{x_3}$$

using as <u>few</u> gates as possible. Do <u>not</u> assume that the inputs are available for free in complemented (inverted) form.

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[3] Q3. Complete the Karnaugh map below to represent the following logic function:

$$f = \overline{x_1}\,\overline{x_3}\,\overline{x_4} + x_2\overline{x_3}x_4 + x_1x_3x_4 + x_1\overline{x_2}x_3 + \overline{x_1}\,\overline{x_2}\,\overline{x_4} + x_1x_2\overline{x_3}\,\overline{x_4} + x_1\overline{x_2}\,\overline{x_3}\,\overline{x_4}$$

x_3x_4 \ x_1x_2	00	01	11	10
00				
01				
11				
10				

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[7] Q4. For the function represented in the Karnaugh map below,

a) Find the Boolean expressions representing the <u>minimal</u> cover in both the sum-of-products (SOP) and product-of-sums (POS) forms.

x_1x_2 / x_3x_4	00	01	11	10
00	1	1	1	1
01	0	1	1	0
11	0	0	1	1
10	1	0	0	1

SOP Form:

POS Form:

b) Compute the cost of implementing both in two levels of logic. Assume that only the non-inverted inputs are available (i.e. you must include the cost related to inverters).

Cost of SOP form =

Cost of POS form =

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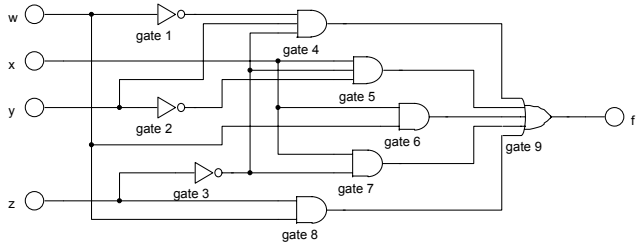
[10] Q5. Synthesize the following 3-input, 3-output logic function (the inputs are a, b and c and the outputs are f_1, f_2, and f_3) to obtain a minimum overall (total) cost implementation using only AND, OR and NOT gates. Do <u>not</u> assume that inputs are available in the complemented (inverted) form. Show all of your work. Your final answer should be a circuit diagram.

a	b	c	f_1	f_2	f_3
0	0	0	0	1	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	0	0	x

[6] Q6. Using the Karnaugh map below, determine which gate(s) can be removed from the following circuit to reduce the cost as much as possible. Note that you may not create any new gates, only remove the existing one(s). Assume that every gate and wire you see on this diagram costs something.



wx / yz	00	01	11	10
00				
01				
11				
10				

Answer: The gates to remove are: _____

[5] Q7. Give the schematic diagram for the following Verilog code. Be sure to label your schematic with the same names as given in the code.

```
module q7 (x1,x2,x3,f1,f2,clock);

input x1,x2,x3,clock;
output f1,f2;
reg f1,f2;

always @(posedge clock)
begin
     f1 <= x1 & x2 | (!x3);
     f2 <= x1 | x3;
end
endmodule
```

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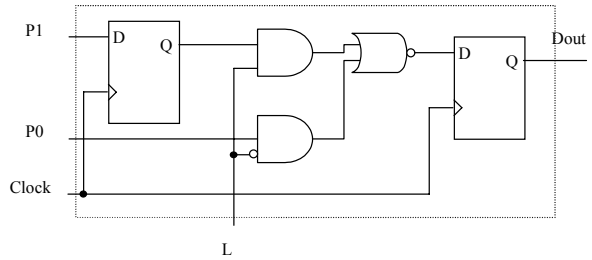
[5] Q8. Give the Verilog code for the following schematic. Use the same names in your code as given on the schematic.



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[10] Q9. Using *only* positive-edge triggered D-type flip flops and any logic gates necessary, design a synchronous counter that counts through the sequence: 0, 1, 2, 4, 6 and then repeats.

a) Give the sequence of the 5 binary numbers that the counter steps through:

b) Give the design of the circuit:

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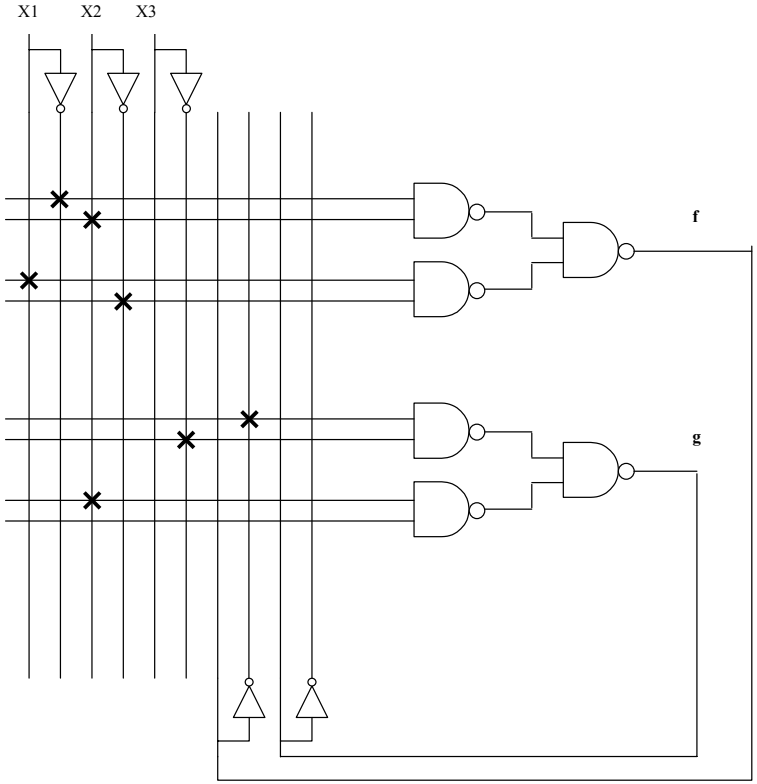
[5] Q10. The following schematic represents a programmable logic device that has been programmed. Assume that when two wires that cross are annotated as follows:

it means that the wires are connected, while wires that cross without the "X" are not connected. Also, assume that gates whose inputs are not connected to anything will take that inputs as a logical "1".

Determine the logic function for **f** and **g** in terms of **x1**, **x2**, and **x3.** Do not simplify or optimize the function.



f = _____

g = _____

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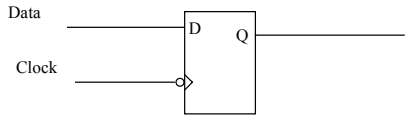
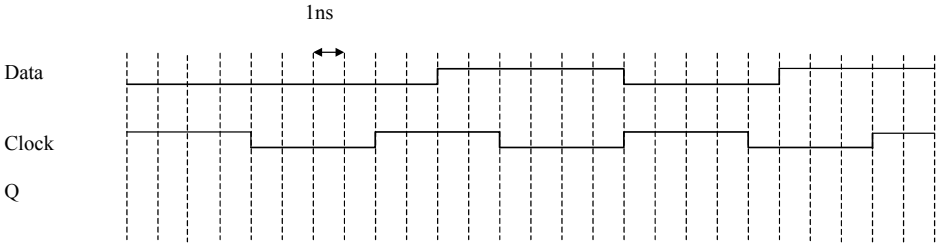
[5] Q11. Consider the following *negative* edge-triggered D-type flip-flop. It has a set-up time of 4ns, a hold time of 2ns and a clock-to-Q time of 3ns.



The following timing diagram (in which the dashed lines are spaced by 1 ns of time) shows the signals incident on the flip-flop over a period time.

a) Fill in the correct timing for the output Q (across the entire page). Assume that Q starts at the value 1. If the value of Q is not known at any point in time, put an **X** in that 1ns time slot.

b) Indicate on the timing diagram any point at which the flip-flop will not operate correctly, and give the name of the problem.



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EXTRA SPACE - USE ONLY IF NEEDED