Last Name_____Student Number_____

University of Toronto

Faculty of Applied Science and Engineering

Department of Electrical and Computer Engineering

Midterm Examination

ECE 241F - Digital Systems
Wednesday October 13, 2004, 6:00pm

Duration: 90 minutes
Examiners: S Brown, J. Rose, K. Truong and B. Wang

ANSWER ALL QUESTIONS ON THESE SHEETS, USING THE BACK SIDE IF NECESSARY.
1. No calculator and no cellphones are allowed.
2. The number of marks available for each question is indicated in the square brackets []; each portion of a question also shows how many marks are allocated to it.
3. There are two extra blank pages at the end of the test for rough work.

AID ALLOWED: The Course Textbook, **Fundamentals of Digital Logic with Verilog Design.**

Last Name: **SOLUTIONS**

First Name: _____

Student Number: _____

Lecture Section:
Section 01 (Rose) [ ]
Section 02 (Wang) [ ]
Section 03 (Brown) [ ]
Section 04 (Truong) [ ]

Total Available Marks:

Question	1	2	3	4	5	6	7	8	9	Total
Marks Available	5	6	5	9	5	10	6	5	4	55
Marks Achieved										

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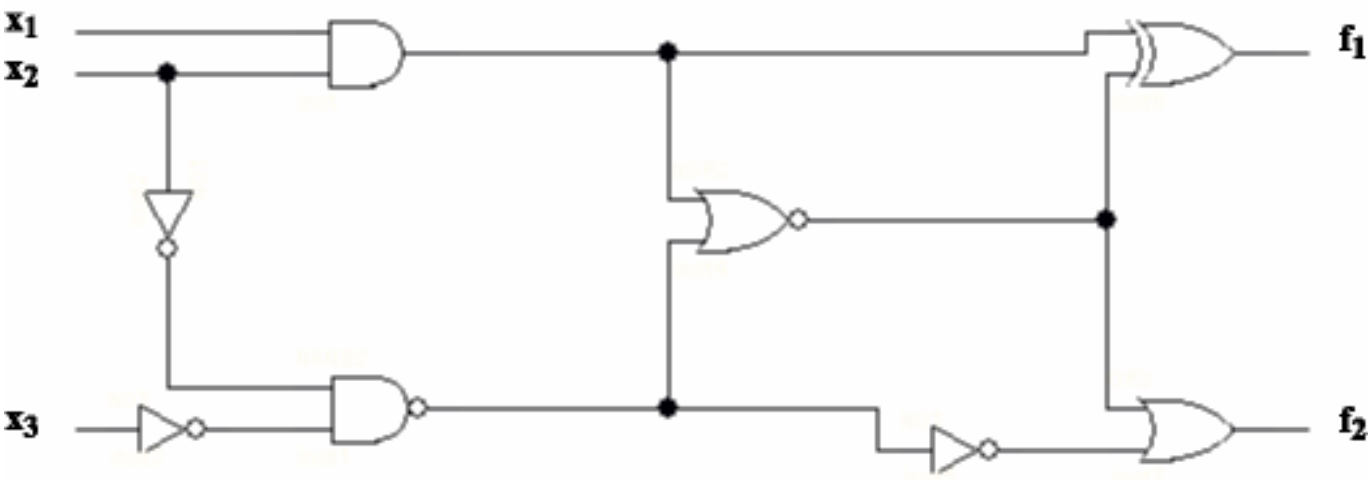
[5] Q1. For the below circuit, write the minimal sum of products form of the logic function of f_1 and f_2 in terms of x_1, x_2, and x_3.



ANSWER:

[0.5 mark] Term after AND gate: x_1x_2
[0.5 mark] Term after NAND gate: $x_2 + x_3$
[0.5 mark] Term after NOR gate: $x_2'x_3'$

[2 marks total] Solving for f_1 (each step 1 mark):

$f_1 = (x_1x_2)'(x_2'x_3') + (x_1'x_3')'(x_1x_2)$
$= (x_1' + x_2')(x_2'x_3') + (x_2+x_3)(x_1x_2)$
$= x_1'x_2'x_3' + x_2'x_3' + x_1x_2 + x_1x_2x_3$
$= x_2'x_3' + x_1x_2$

[1.5 marks total] Solving for f_2 (each step 1 mark):

$f_2 = (x_2'x_3') + (x_2 + x_3)'$
$= (x_2'x_3') + (x_2'x_3') = (x_2'x_3')$

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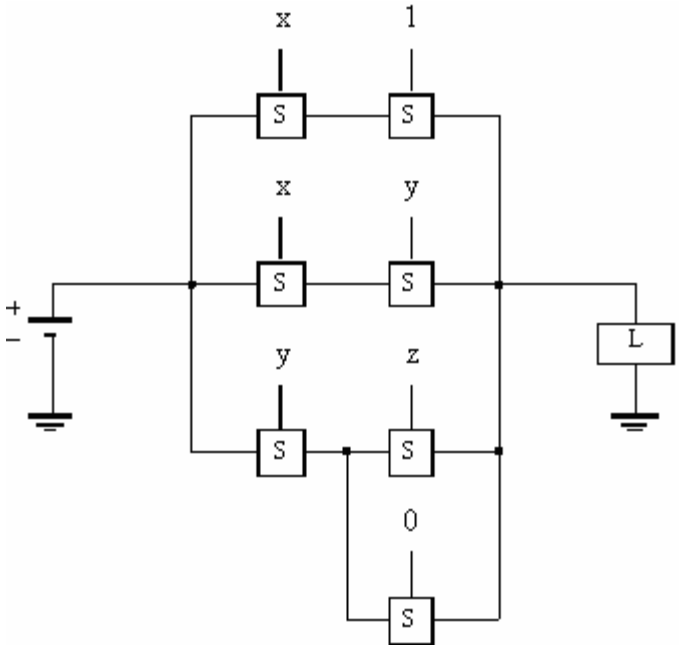
[6] Q2 In Section 2.1 of the textbook, circuits that turn a simple light, *L*, on or off are used to illustrate some basic logic functions. This questions involves some similar circuits with switches controlled by inputs *x*, *y*, or *z*, or the constant values 0 or 1. A switch controlled by 0 is turned off, and a switch controlled by 1 is turned on.

[2] **(a)** Consider the circuit diagram shown below. You are to write a logic expression, in sum of products form, for the function *L*, where *L* is 1 when the light is on and 0 when the light is off. Higher marks will be given for determining the simplest SOP expression possible.



ANSWER (it is **not necessary** to show the steps used to derive your answer):

L = x (1) + xy + y (z + 0)

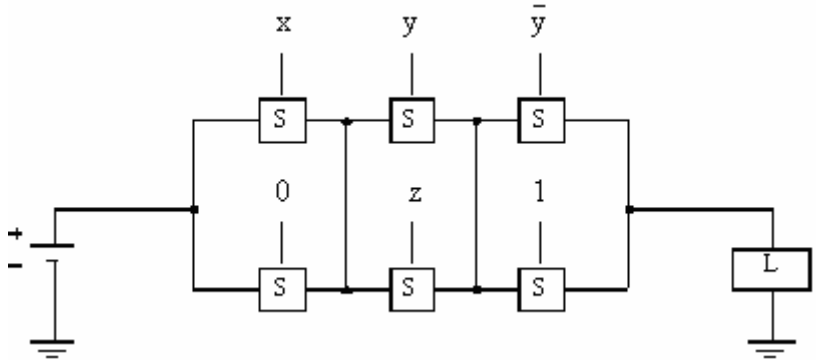
= x + xy + yz

= x + yz

2 marks for final answer
1 mark for right answer, but not minimal
0 otherwise

Q2, continued

[2] **(b)** Consider the circuit diagram shown below. You are to write a logic expression in *products of sums* form for the function *L*. Higher marks will be given for the simplest POS expression possible.



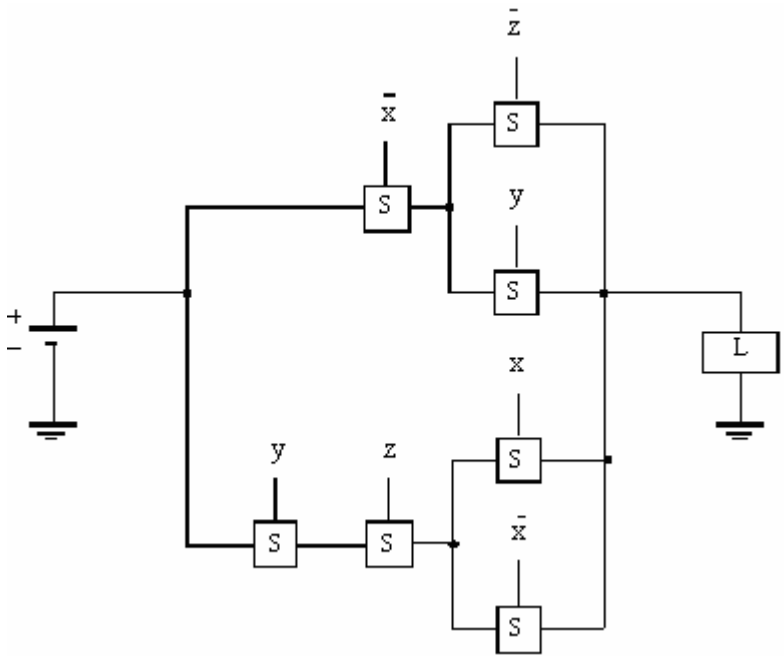
ANSWER (it is **not necessary** to show the steps used to derive your answer):

L = (x + 0) (y + z) (y' + 1)
= x (y + z)

2 marks for final answer
1 mark for right answer, but not minimal
0 otherwise

Q2, continued

[2] **(c)** Consider the circuit diagram shown below. You are to write a logic expression in sum of products form for the function *L*. Higher marks will be given for the simplest SOP expression possible.



ANSWER (it is **not necessary** to show the steps used to derive your answer):

L = x'(z'+y) + y z (x + x')
  = x'z' + x'y + yz (**)
  = x'z' + yz (by consensus)

2 marks for final answer
1 mark for **
0 otherwise

[5] Q3. Short answer, lab-related questions.

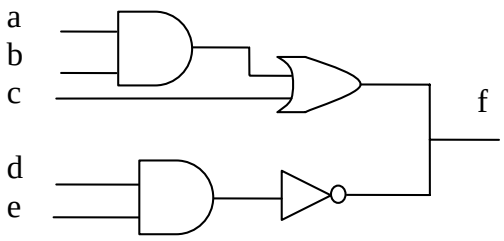
[0.5] (a) When using Quartus to design a circuit with the block/schematic editor, is it *necessary* to also provide to Quartus the equivalent Verilog code before you can successfully compile the schematic?

CIRCLE ANSWER: YES (NO)

[1] (b) What is the purpose of the logic probe in the lab?

To measure circuit outputs so as to be able to determine errors (debug) the circuit.

[2] (c) What is wrong with the following circuit? State why it is wrong.

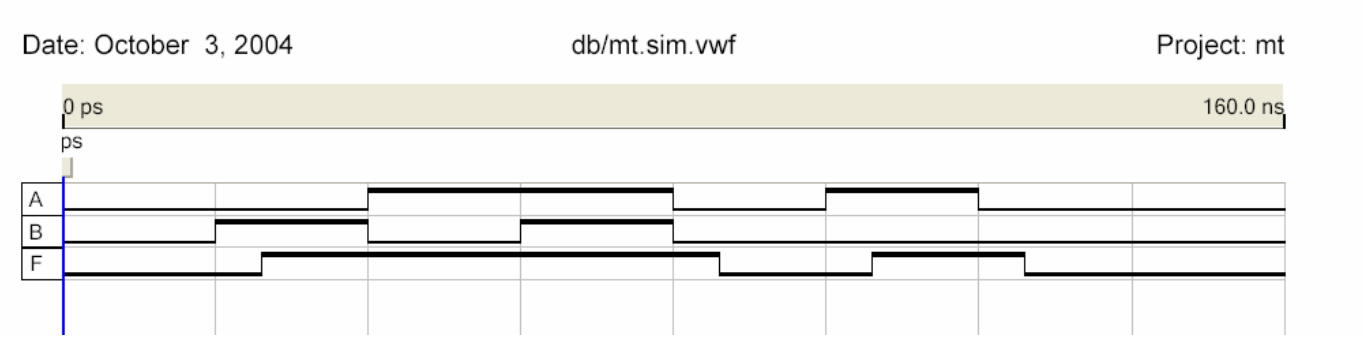


ANSWER:

Two outputs of logic gates are connected together. This is wrong because each gate drives an independent voltage, and it makes no logical sense to force one wire to (likely) two different values. 2 marks, 1 for each.

Question 3, continued

[1.5] (d) Observe the following output from the Quartus simulator, which shows a simulation of a digital circuit with inputs **A** and **B** and output **F**:



[0.5] (i) Which of the two *types* of simulation possible is being used?

ANSWER: TIMING

[1] (ii) What is the function of the logic gate being simulated?

ANSWER: OR

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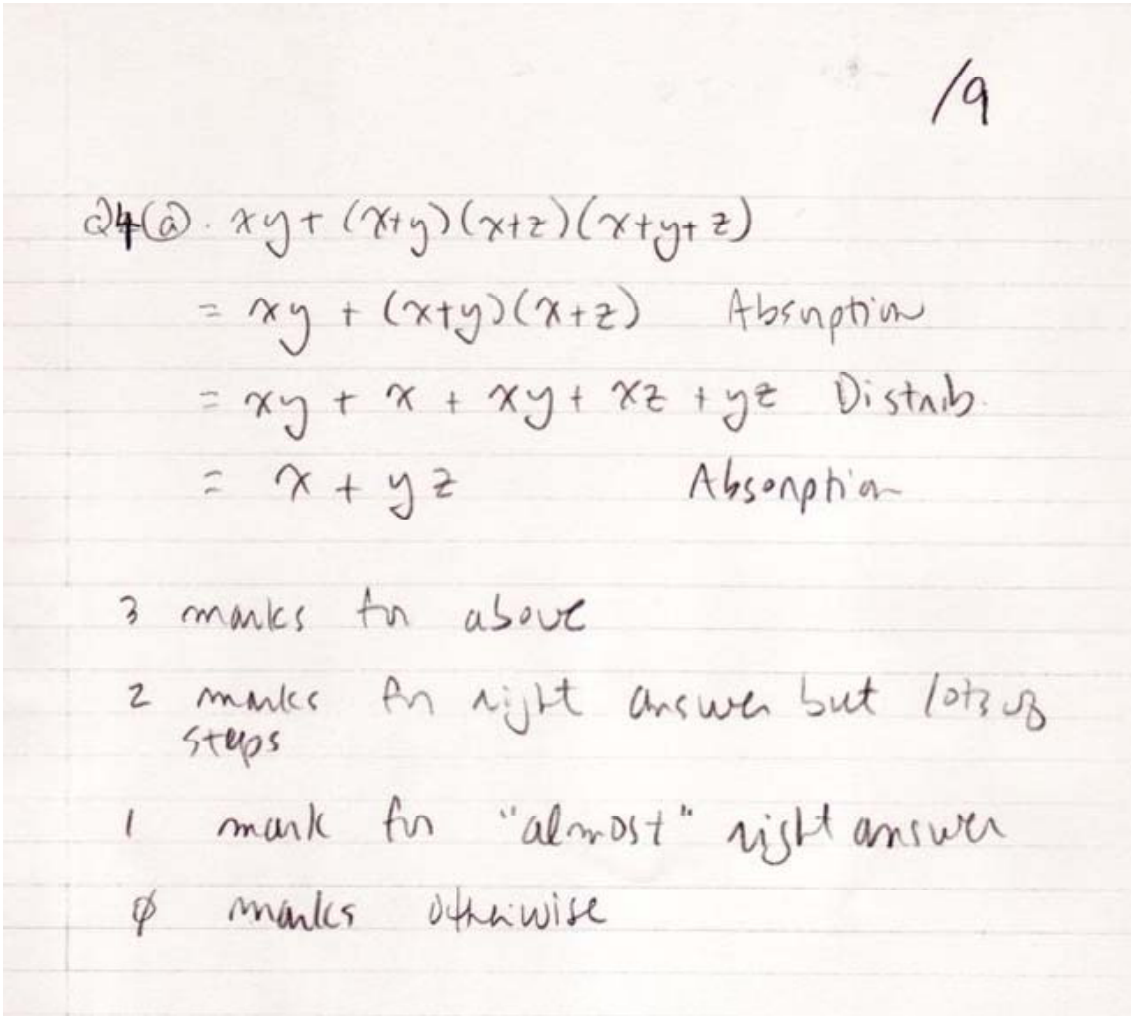
[9] Q4 For this question you are to use algebraic manipulation to produce minimum sum-of-products or product-of-sums expressions. You need to show your work and the steps that are being used in your solution. Higher marks will be given for solutions that apply the theorems and identities of Boolean algebra in as few steps as possible. So, you are to show all of your steps, but don't use more steps than needed.

[3] (a) Use Boolean algebra to minimize the following expression. Your final answer should be the minimal SOP form for this function.

$$f = xy + (x + y)(x + z)(x + y + z)$$

ANSWER:

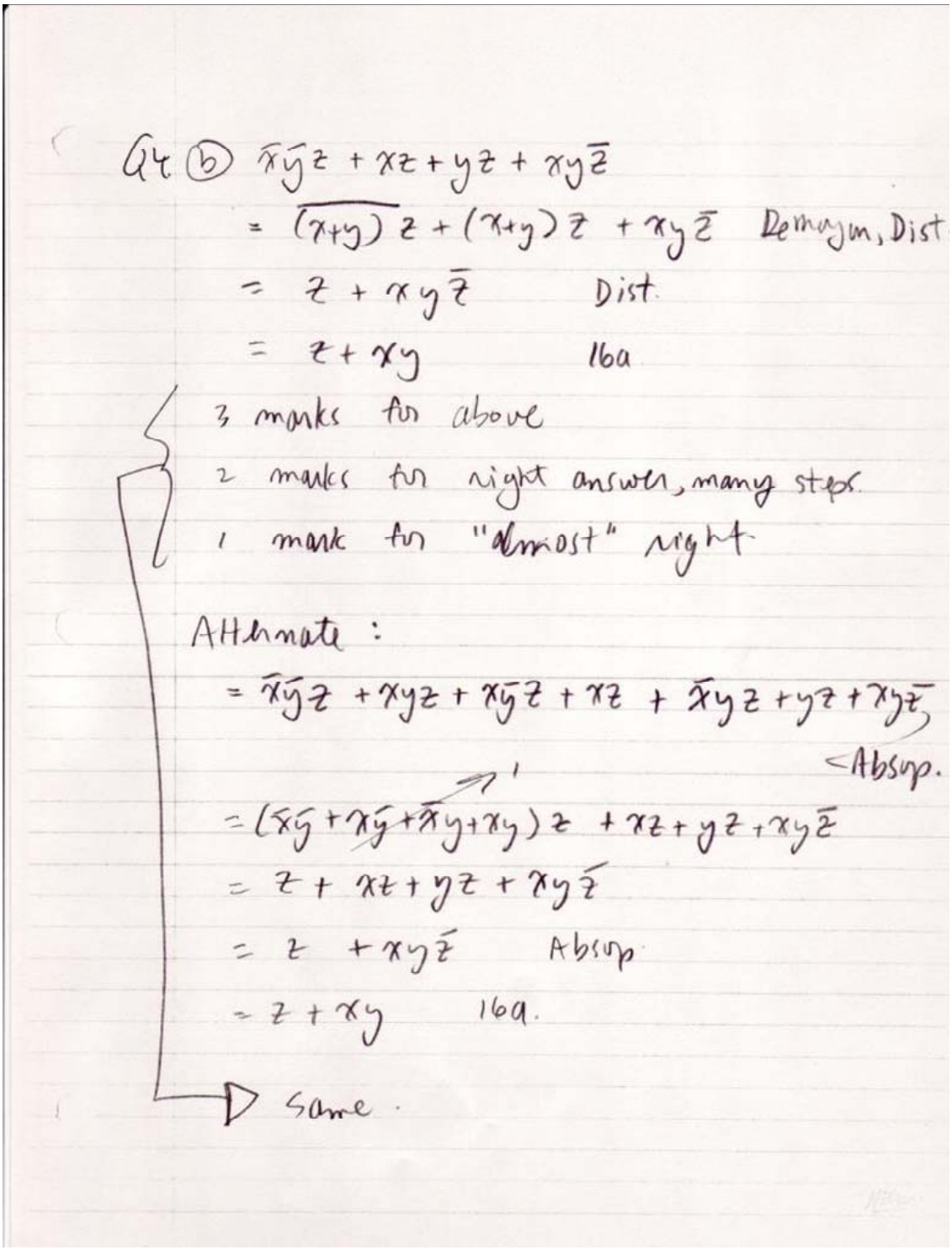


Question 4, continued

[3] (b) Use Boolean algebra to minimize the following expression. Your final answer should be the minimal sum of products (SOP) form for this function.

$$f = \bar{x} \cdot \bar{y} \cdot z + x \cdot z + y \cdot z + x \cdot y \cdot \bar{z}$$

ANSWER:

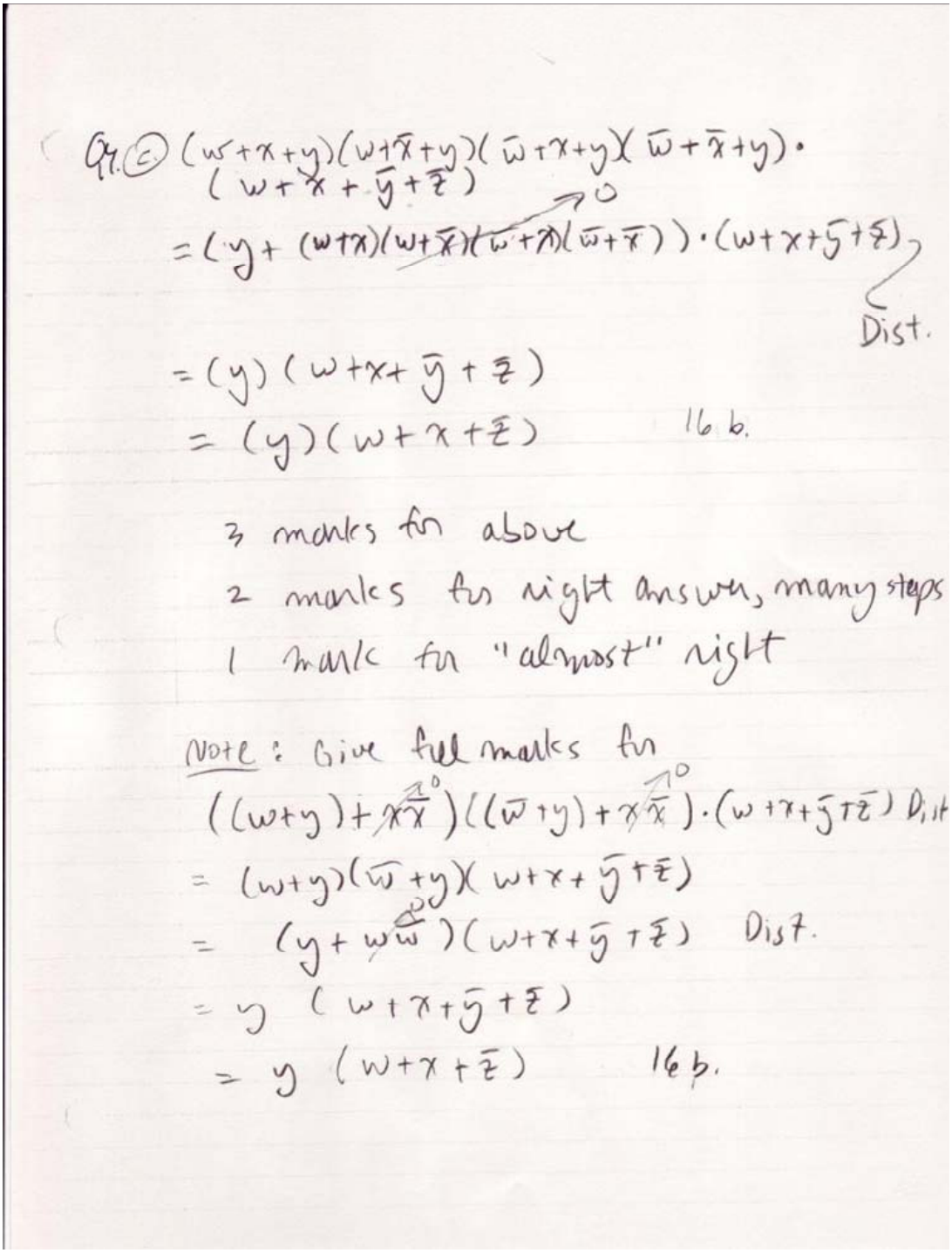


Question 4, continued

[3] (c) Use Boolean algebra to minimize the following expression. Your final answer should be the minimal product of sums (POS) form for this function.

$$f = (w + x + y)(w + \bar{x} + y)(\bar{w} + x + y)(\bar{w} + \bar{x} + y)(w + x + \bar{y} + z)$$

ANSWER:



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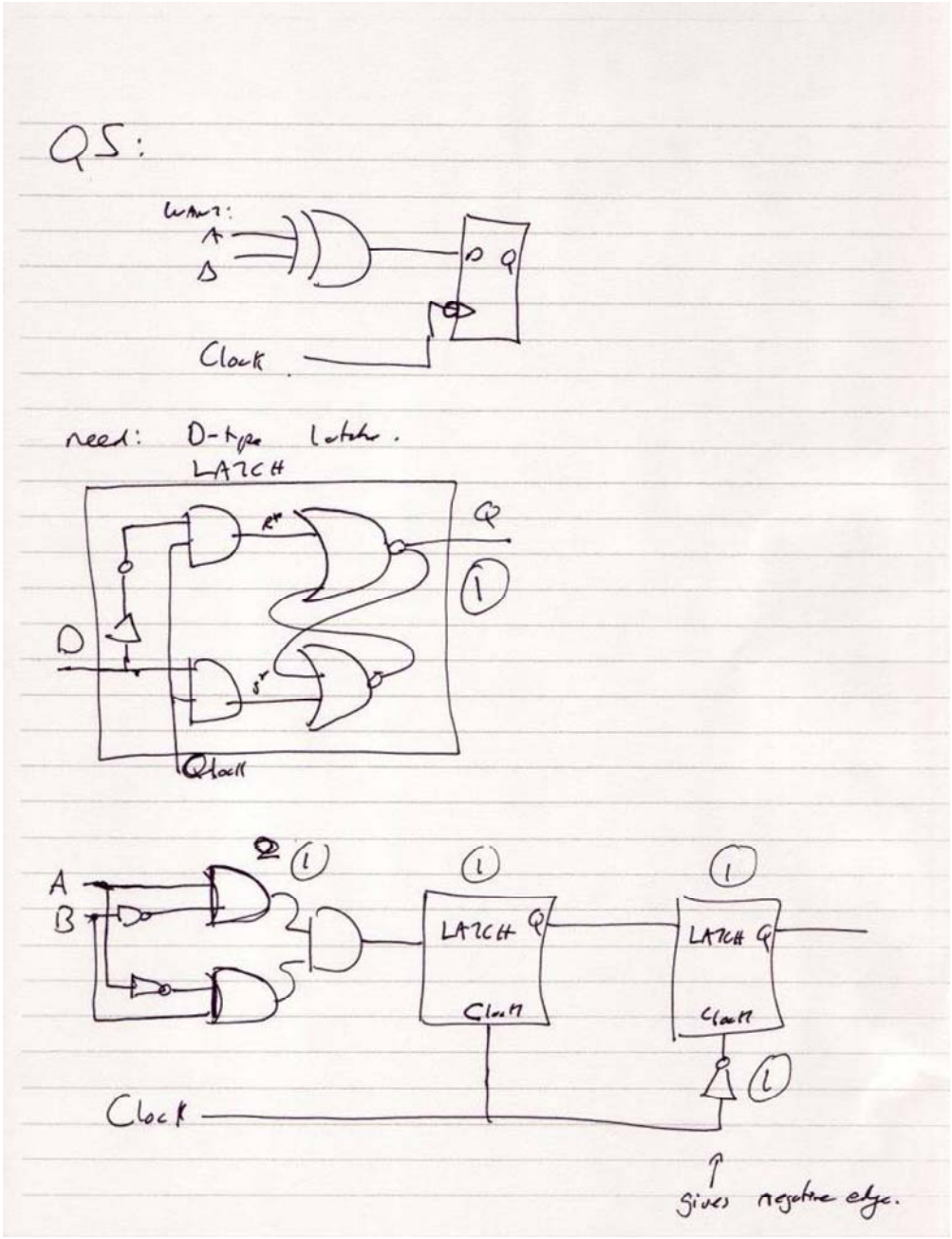
[5] Q5. Read this question carefully. You are to design a circuit that has 3 inputs, **A**, **B** and **Clock**, and one output, **F.** The output F should be the exclusive-OR function of the signals A and B captured just prior to the *falling* edge (i.e. the 1 to 0 transition) of the signal **Clock.** You may use only AND, OR, NAND, NOR or NOT gates in your design, but you should present your design "hierarchically" – meaning that you can show a repetitive part of your design as a separate group of gates enclosed by a box with a name, and then use that named box one or more times in the final design.

ANSWER:



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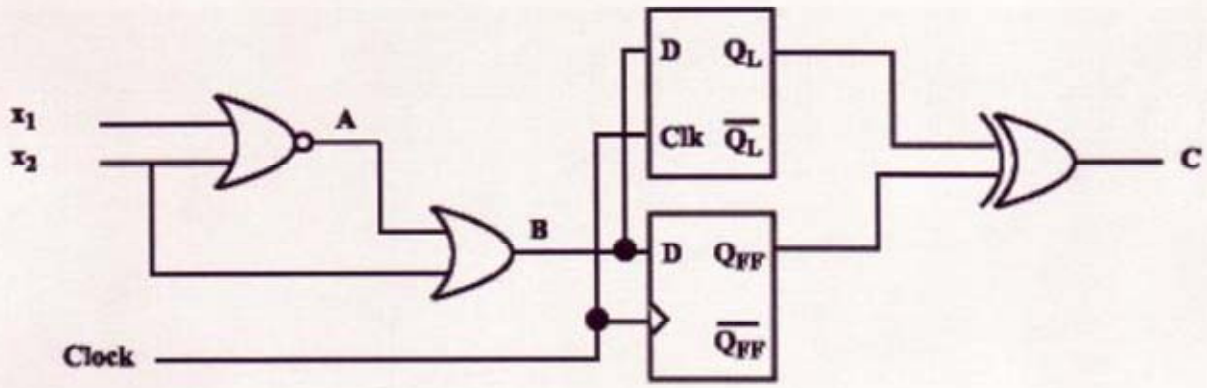
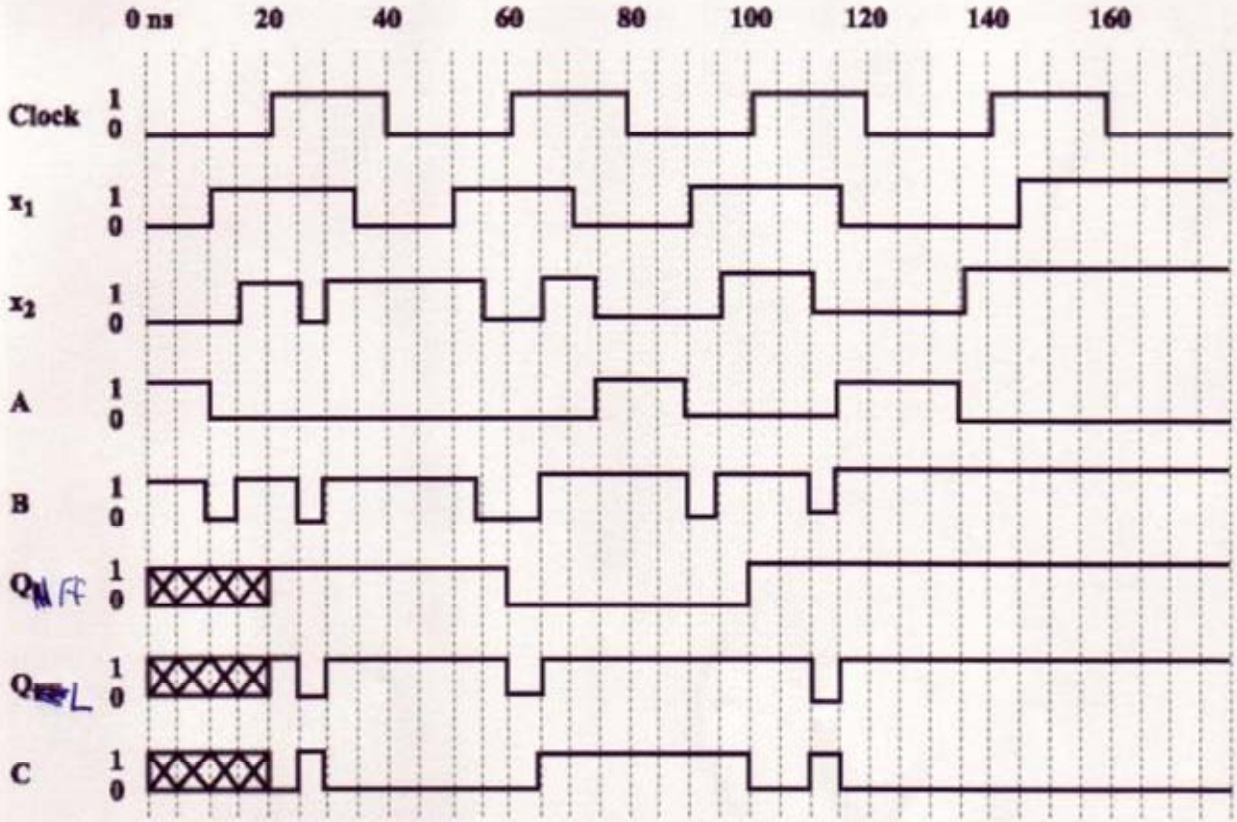
[10] Q6. Consider the circuit shown below. Assume there is no propagation or clock-to-Q delay in the latch, flipflop and gates. Draw the timing diagram showing A, B, Q_L(latch), Q_{FF}(flipflop) and C.





2 marks each for each correct line. Proportional marks for proportion of correct signals.

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[6] Q7. a) For the Karnaugh map shown below derive the minimum-cost sum-of-products (SOP) for the logic function f (a,b,c,d). [2]

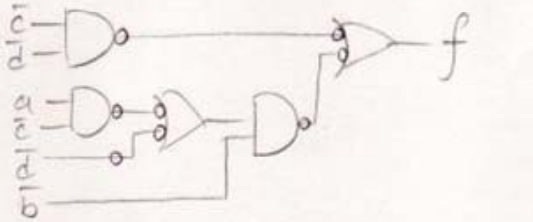
ab \ cd	00	01	11	10
00	1	1	1	1
01	0	0	0	1
11	0	0	0	0
10	1	0	0	1

$f = \bar{c}\bar{d} + \bar{b}\bar{d} + a\bar{b}\bar{c}$

each wrong term [-½]

b) Implement the function f (a,b,c,d) using only 2-input NAND gates (as few as possible), assuming that both the true and complemented variables are available as inputs. [4]

$f = \bar{c}\bar{d} + \bar{b}(\bar{d} + a\bar{c})$ factoring



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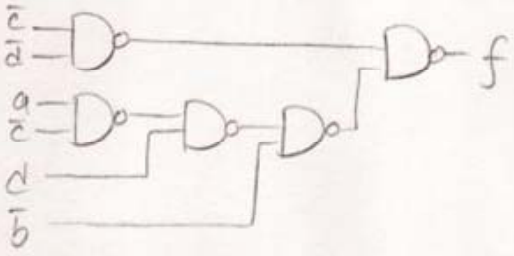
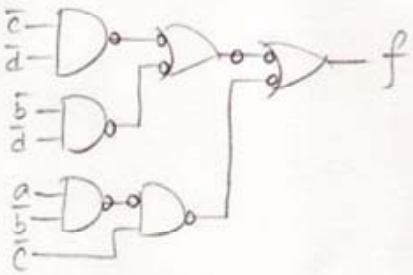


full mark!



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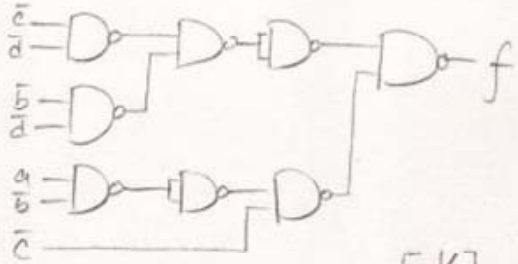

[-½]

keep ▷ in the cct. [-½]

each extra gate beyond 8 [-½]

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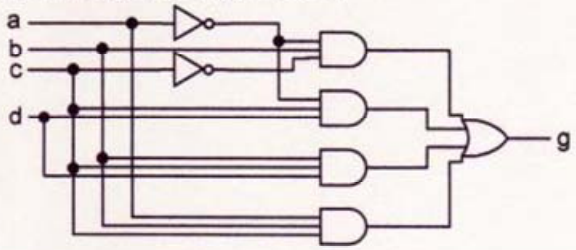
[5] Q8. For the 2-level logic circuit given below,



a) Write the logic expression g (a,b,c,d) in sum-of-products (SOP) form. [1]

$g = \bar{a}b\bar{c} + \bar{a}cd + bcd + abc$

partially correct [-½]

b) Represent the function g (a,b,c,d) in the following K-map. [2]

ab / cd	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	0

each wrong "1" entry [-½]

c) Derive the minimum-cost product-of-sums (POS) expression for g (a,b,c,d). [2]

$g = (b+c)(\bar{a}+c)(\bar{a}+b)(a+\bar{c}+d)$

each wrong term [-½]

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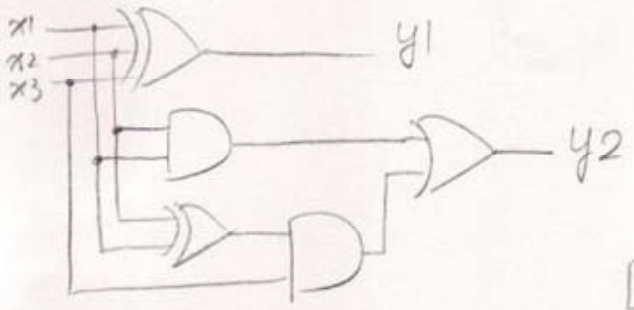
[4] Q9. Draw the schematic diagram and derive the logic expressions for the output functions for the Verilog code given below. Be sure to label all wires using the same symbols as in the code.

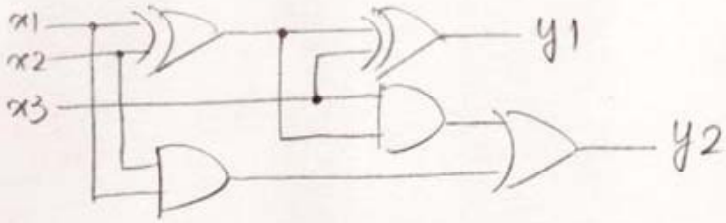
```
module simple_cct (x1, x2, x3, y1, y2);
    input  x1, x2, x3;
    output y1, y2;

    assign y1 = x1 ^ x2 ^ x3;
    assign y2 = (x1 & x2) | ((x1 ^ x2) & x3);
endmodule
```



[2½]

each gate is worth ½ mark

or



$y1 = x1 \oplus x2 \oplus x3$ [½]

$y2 = x1 \cdot x2 + (x1 \oplus x2) \cdot x3$ [1]

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