Last Name_____Student Number_____

University of Toronto

Faculty of Applied Science and Engineering

Department of Electrical and Computer Engineering

Midterm Examination

ECE 241F - Digital Systems
Tuesday October 11, 2005, 6:00 – 7:30 pm

Duration: 90 minutes
Examiners: S Brown, J. Rose, K. Truong and B. Wang

ANSWER ALL QUESTIONS ON THESE SHEETS, USING THE BACK SIDE IF NECESSARY.
1. No calculator and no cellphones are allowed.
2. The number of marks available for each question is indicated in the square brackets []; each portion of a question also shows how many marks are allocated to it.
3. There are two extra blank pages at the end of the test for rough work.

AID ALLOWED: The Course Textbook, **Fundamentals of Digital Logic with Verilog Design.**

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Last Name: _____

First Name: _____

Student Number: _____

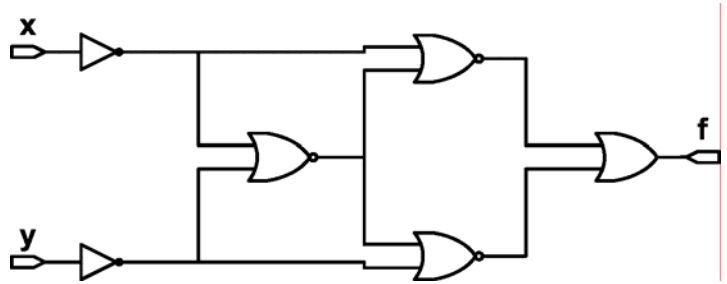
Lecture Section: **Section 01 (Rose) [ ]**
Section 02 (Wang) [ ]
Section 03 (Brown) [ ]
Section 04 (Truong) [ ]

Total Available Marks:

Question	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**Total**
Marks Available	**6**	**6**	**9**	**8**	**6**	**8**	**5**	**6**	**53**
Marks Achieved									

[5] Q1. Circuit analysis.

[2] **(a)** For the following circuit, give the truth table.



ANSWER:
(Marking scheme: 0.5 marks for each row)

x	y	f
0	0	0
0	1	1
1	0	1
1	1	0

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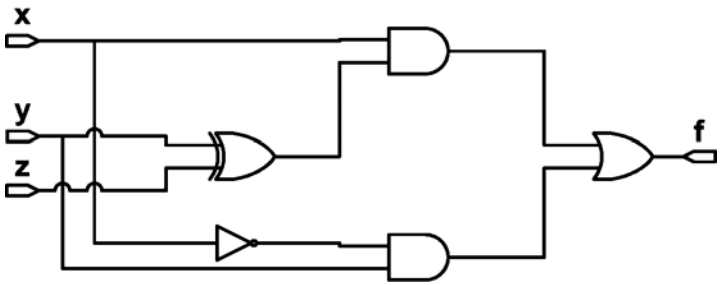
Q1, continued.

[3] **(b)** For the following circuit, give the truth table.



ANSWER:

(Marking scheme: -0.5 marks for each incorrect row)

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

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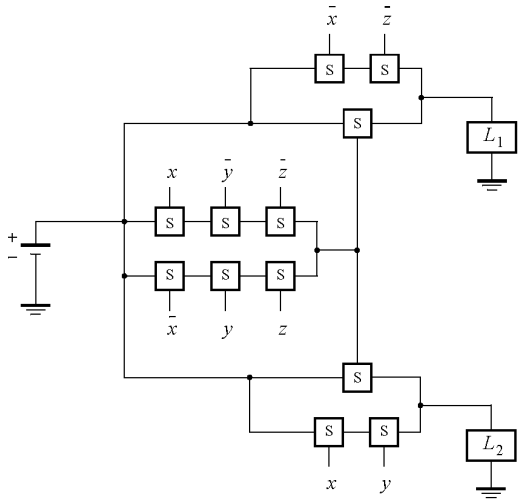
[6] Q2 In Section 2.1 of the textbook, circuits that turn a simple light, *L*, on or off are used to illustrate some basic logic functions. This questions involves some similar circuits with switches controlled by inputs *x*, *y*, or *z*.

[3] **(a)** Consider the circuit diagram shown below. You are to write logic expressions, in **sum-of-products** (SOP) form, for the functions L_1 and L_2 where each of these functions is 1 when the light is on and 0 when the light is off. Higher marks will be given for determining the simplest SOP expression possible.



ANSWER (it is **not necessary** to show the steps used to derive your answer):

L1 = !xy + !y!z (1.5 marks)
L2 = x!z + yz (1.5 marks)

If a consensus term is present (!x!z in L1 and xy in L2) then -0.5 for each consensus term.

Other accepted solutions:
L1 = x!y!z + !xyz + !x!z (0.5 marks)
L2 = x!y!z + !xyz + xy (0.5 marks)

-0.5 if the equation is not in Sum of Products form.

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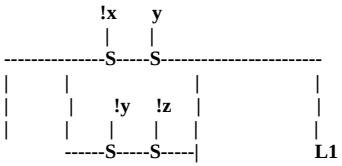
Q2, continued.

[3] **(b)** Assume now that we need to implement a circuit that drives only light L_1 from part (a). Draw the simplest circuit you can with switches like those shown in part (a) that implements only L_1. Higher marks will be given for a circuit that uses as few switches as possible.

ANSWER (it is **not necessary** to show the steps used to derive your answer):



3 marks when diagram shown here corresponds to equation for L1 in part a, even if part (a) is wrong. Subtract 0.5 for any unnecessary switches, or switches with more or fewer than 3 terminals.

0 marks are given when logic gates are used to represent the function, instead of switches.

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[9] Q3. For this question you are to use algebraic manipulation to produce minimal cost **sum-of-products** (SOP) or **product-of-sums** (POS) expressions. You need to show your work and the steps that are being used in your solution. Higher marks will be given for solutions that apply the theorems and identities of Boolean algebra in as few steps as possible. So, you are to show all of your steps, but don't use more steps than needed.

[3] **(a)** Use Boolean algebra to minimize the following expression. Your final answer should be the minimal cost **sum-of-products** (SOP) form for this function.

$$f = y\bar{z} + (\bar{x} + \bar{z})(x + y + \bar{z})$$

ANSWER:

f	= y !z + (!z + (!x)(x + y))	by Distribution
	= y !z + !z + !xy	by Distribution, and !x x = 0
	= !z + !x y	by Absorption

3 marks for correct solution using OR-based distribution (SOP)

2 marks for correct solution using AND-based distribution (POS)

1 mark for incorrect solution, but evidence of correct application of logic reduction rules is shown.

0 if reduction makes no sense, no work is shown except for the final answer, or a K-map is used to minimize the logic function.

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Q3, continued.

[3] **(b)** Use Boolean algebra to minimize the following expression. Your final answer should be the minimal cost **sum-of-products** (SOP) form for this function.

$$f = x \cdot \bar{z} + x \cdot y + \bar{x} \cdot \bar{y} + \bar{y} \cdot z$$

ANSWER:

f = x!z + !yz + x!y +xy + !x!y Consensus
= x(!y + y) + !y(x + !x) + x!z + !yz
= x + !y + x!z + !yz
= x + !y

3 marks for correct solution using logical progression of manipulations

2 marks for almost correct solution

1 mark for incorrect solution, but evidence of correct application of logic reduction rules is shown.

0 if reduction makes no sense, no work is shown except for the final answer, or a K-map is used to minimize the logic function.

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Q3, continued.

[3] **(c)** Use Boolean algebra to minimize the following expression. Your final answer should be the minimal cost **product-of-sums** (POS) form for this function.

$$f = y + xz + \overline{xz}$$

ANSWER:

!f = !(y + xz + !x!z)
= !y !(xz)!(!x!z) by deMorgan
= !y (!x + !z)(x + z) by deMorgan
= !y (!xz + !zx) by Distrbution
= !y!xz + !y!zx
f = !(!y!xz + !y!zx)
= !(!y!xz) !(!y!zx) by deMorgan
= (x + y + !z)(!x + y + z) by deMorgan

3 marks for correct solution using logical progression of manipulations

2 marks for correct solution, but not minimal

1 mark for incorrect solution, but evidence of correct application of logic reduction rules is shown. Solution not in POS form

0 if reduction makes no sense, no work is shown except for the final answer, or a K-map is used to minimize the logic function.

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[8] Q4. Karnaugh maps.

[2] **(a)** For the Karnaugh map shown below, derive the minimal cost **sum-of-products** (SOP) form for the logic function f (x,y,z).

	xy	00	01	11	10
z	0	1	0	1	0
	1	1	1	0	1

ANSWER: (Marking scheme: - 0.5 marks for each missing term)

f=x'y'+y'z+x'z+xyz'

[2] **(b)** Derive the minimal cost **product-of-sums** (POS) form for the logic function f (a,b,c,d).

	ab	00	01	11	10
cd	00	0	0	0	1
	01	1	0	0	1
	11	0	0	1	1
	10	0	1	0	0

ANSWER: (Marking scheme: - 0.5 marks for each missing term)

f=(b'+c)(a+c'+d')(a+b+d)(a'+c'+d)

[4] **(c)** Derive the minimal cost **sum-of-products** (SOP) form for the logic function f (a,b,c,d,e). Note that '**×**' is a don't care output.

E=0

	ab	00	01	11	10
cd	00	1	0	×	1
	01	0	×	0	0
	11	0	0	1	0
	10	×	0	0	1

e=1

	ab	00	01	11	10
cd	00	1	0	1	×
	01	1	×	0	×
	11	1	0	0	×
	10	1	1	1	×

ANSWER: (Marking scheme: +1 mark for each correct term)

f=b'd' + ac'd' + cd'e + abcde'+ b'e

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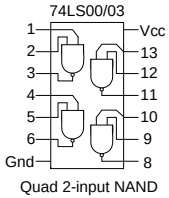
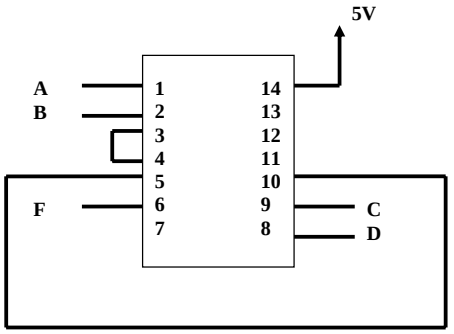
[6] Q5. A student in ECE 241 has been asked to wire up a single TTL 74LS00 QUAD 2-input NAND gate chip (the pin-out of which is given below) to implement the logic function **F = AB + CD**. Below you will see the wiring diagram that student has created. The circuit doesn't work because it has **exactly three** errors or omissions. Your answer, on the next page, should be the ***changes*** that need to be made to the circuit to make it function correctly. For example, a change could be "connect pin 3 to pin 12."

Pin-out Diagram for the 74LS00:



Quad 2-input NAND

Below is the wiring diagram of the student's circuit;



(question continues on next page)

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Q5, continued.

Working space:

Answers:

Circuit Error #1: Connect Ground to Pin 7 [2 marks]
Circuit Error #2: Connection from Pin 5 to 10 should be Pin 5 to Pin 8 [2 marks]
Circuit Error #3: Connection from D to pin 8 should be from D to Pin 10 [2 marks]

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[8] Q6. Word problem

[3] **(a)** A museum has three rooms, each with a motion sensor (m_1, m_2, and m_3) that outputs 1 when motion is detected. At night, the only person in the museum is one security guard who walks (i.e. no standing still, or sitting, or sleeping) from room to room. Give a truth table for the security system that sounds an alarm (by setting an output *A* to 1) if motion is ever detected in more than one room at a time. (*Hint: be sure to include any don't care in the output.*)

m_1	m_2	m_3	A
0	0	0	X
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Marking scheme: 1 mark for "x"
2 marks for the remaining entries

[5] **(b)** Now consider a museum with 7 rooms. A truth table is not a good choice (it has too many rows), nor is an equation describing when the alarm should sound (it has too many terms). However, the inverse of the alarm function can be straightforwardly captured as a logic equation, and then the desired circuit (*A*) can be achieved by adding an inverter to the inverse function ($\overline{A}$). Design the 7-room security system by expressing the inverse of the alarm function, $\overline{A}(m_1, m_2, m_3, m_4, m_5, m_6, m_7)$.

$$\overline{A} = m_1\overline{m}_2\overline{m}_3\overline{m}_4\overline{m}_5\overline{m}_6\overline{m}_7 + \overline{m}_1m_2\overline{m}_3\overline{m}_4\overline{m}_5\overline{m}_6\overline{m}_7 + \overline{m}_1\overline{m}_2m_3\overline{m}_4\overline{m}_5\overline{m}_6\overline{m}_7$$
$$+ \overline{m}_1\overline{m}_2\overline{m}_3m_4\overline{m}_5\overline{m}_6\overline{m}_7 + \overline{m}_1\overline{m}_2\overline{m}_3\overline{m}_4m_5\overline{m}_6\overline{m}_7 + \overline{m}_1\overline{m}_2\overline{m}_3\overline{m}_4\overline{m}_5m_6\overline{m}_7 + \overline{m}_1\overline{m}_2\overline{m}_3\overline{m}_4\overline{m}_5\overline{m}_6m_7$$

or

$$\overline{A} = \overline{(\overline{m_1} + m_2 + m_3 + m_4 + m_5 + m_6 + m_7)(m_1 + \overline{m_2} + m_3 + m_4 + m_5 + m_6 + m_7)}$$
$$\overline{(m_1 + m_2 + \overline{m_3} + m_4 + m_5 + m_6 + m_7)(m_1 + m_2 + m_3 + \overline{m_4} + m_5 + m_6 + m_7)}$$
$$\overline{(m_1 + m_2 + m_3 + m_4 + \overline{m_5} + m_6 + m_7)(m_1 + m_2 + m_3 + m_4 + m_5 + \overline{m_6} + m_7)}$$
$$\overline{(m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + \overline{m_7})}$$

Marking scheme: 5 marks for the correct answer
-0.5 mark for each wrong product / sum term
-1 mark for missing the "long" bar in the POS form

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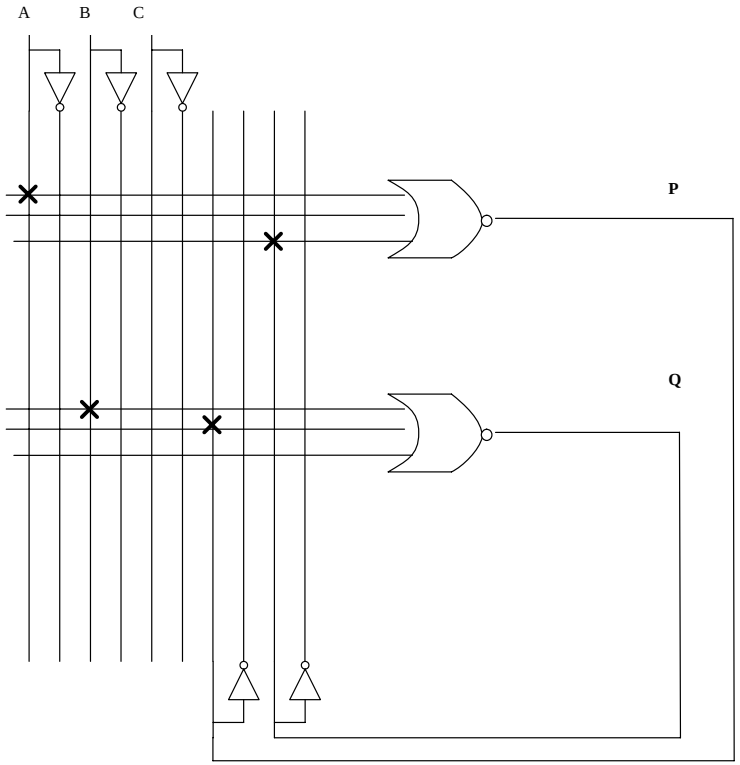
[5] Q7. The following schematic represents a programmable logic device that has been programmed. Assume that when two wires that cross are annotated as follows:

it means that the wires are connected, while wires that cross without the "X" are not connected. Also, assume that gates whose inputs are not connected to anything will take those inputs as a logical "0".



(*question continues on next page*)

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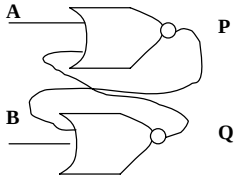
Q7, continued.

[2] **(a)** Redraw the circuit in the simplest form you can.



2 marks; part marks if something sensible.

-1 if mislabeled inputs/outputs
-0.5 for a careless mistake
-1 if unsimplified

[3] **(b)** What is this circuit?

Answer: A Set-Reset Latch (R-S) Latch (3 marks)

If give P = (A + Q)' and Q = (B + P)' only get 1 mark
If answer is just 'latch' then give 1.5 marks.

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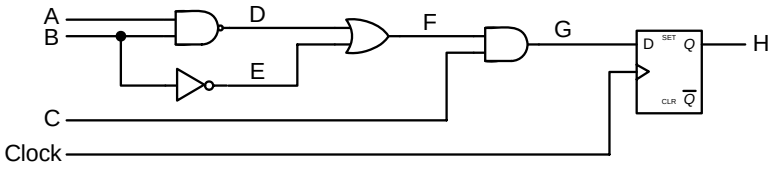
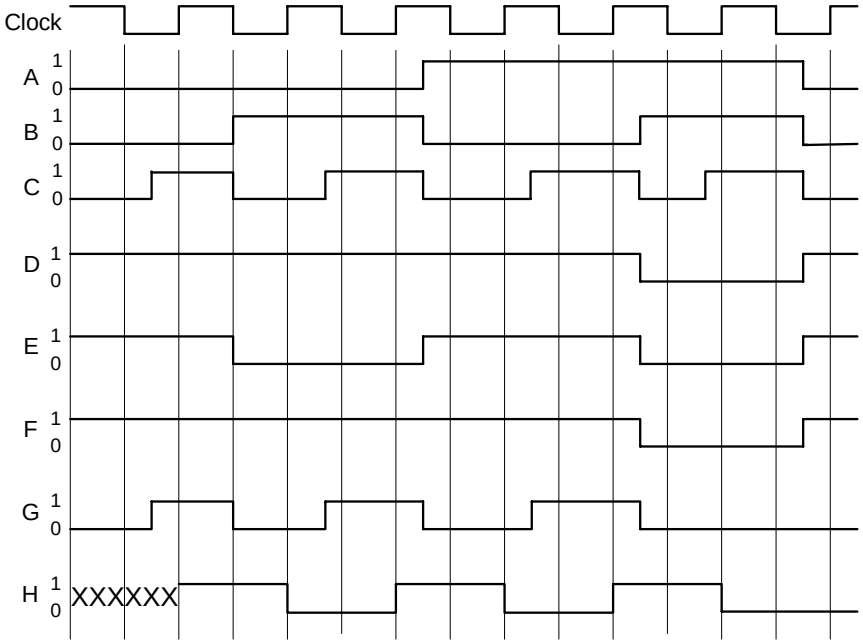
[6] Q8. Consider the circuit shown below. Assume there are no propagation delays in the gates and in the D flip-flop. Draw the timing diagram showing D, E, F, G and H.





Marking scheme: 1 mark each for the correct D, E, F and G
2 marks for the correct H (-0.5 mark for missing XXXXXX)