University of Toronto

Faculty of Applied Science and Engineering

Department of Electrical and Computer Engineering

Midterm Examination

ECE 241F - Digital Systems
Wednesday October 11, 2006, 6:00 – 7:30 pm

Duration: 90 minutes
Examiners: S Brown, J. Rose, K. Truong and B. Wang

ANSWER ALL QUESTIONS ON THESE SHEETS, USING THE BACK SIDE IF NECESSARY.
1. No calculator and no cellphones are allowed.
2. The number of marks available for each question is indicated in the square brackets [].
3. There are two extra blank pages at the end of the test for rough work.

AID ALLOWED: The Course Textbook, **Fundamentals of Digital Logic with Verilog Design.**

Last Name: _____

First Name: _____

Student Number: _____

Lecture Section:
Section 01 (Rose) [ ]
Section 02 (Wang) [ ]
Section 03 (Brown) [ ]
Section 04 (Truong) [ ]

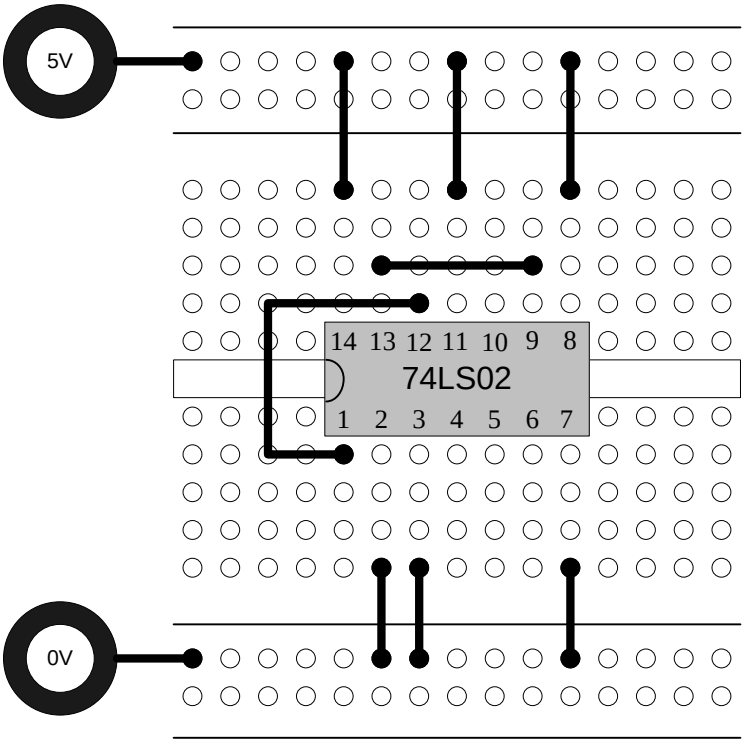
Total Available Marks:

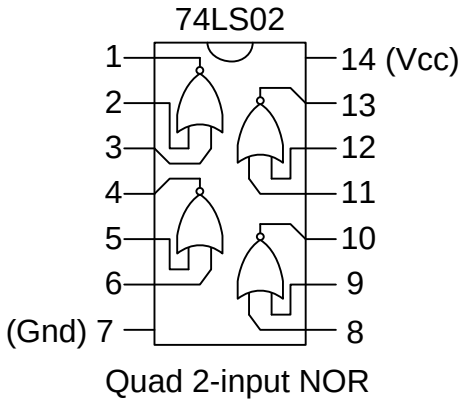
Question	1	2	3	4	5	6	7	8	Total
Marks Available	8	9	7	8	4	7	9	6	58
Marks Achieved									

Last Name_____Student Number_____

[8] Q1. Lab-Based Question.

The picture below shows the protoboard that you used in Laboratory #1. Its holes are connected as you learned in Lab #1. The board has a TTL 74LS02 Quad 2-input NOR gate chip on it, as shown. The pinout for that chip is given at the right of the picture. There are a number of wires placed on this circuit, as indicated by the black lines. The lines/wires connect only the holes on the protoboard at the ends of the wires, not any of the holes traversed in between. Note also that the inputs of the circuit are connected to either 0V or 5V as opposed to a switch.





(a) Draw the schematic of the digital circuit that is wired, using the value "1" to represent logic 1 and "0" to represent logic 0 where ever it appears.

(b) Assume that a logic probe, just like the one you used in the lab, is correctly powered and touched to the pins of the 74LS02 chip that are indicated in the table below (one at a time, once for each row of the table). In the right hand column of the table indicate what the "output" of the logic probe is when touched to each of the pins (i.e. what the indicator lights on the logic probe would show):

74LS02 PIN Number	**Logic Probe Visual "Output"**
1	
13	
10	
5	

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[9] Q2.

(a) Consider the logic function $f(x1, x2, x3, x4) = \sum m(0,2,5,8,9,10,12,13,14,15)$. (Note for the minterm numerical labeling that the order of the variables is *x1 x2 x3 x4*, such that minterm 13 would be written 1101).

Each of the logic expressions below may or may not implement all of the minterms of this function. Indicate which minterms (using their base 10 numerical number) of the function are not covered (if any) in the space provided. If all minterms *are* covered, then your answer should be "NONE".

Working Space:

i. $f = x1 \cdot \overline{x3} + x1 \cdot x2 + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4$

Minterms not covered: _____

ii. $f = x1 \cdot \overline{x3} + x1 \cdot x2 \cdot x3 + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4$

Minterms not covered: _____

Q2(a), cont'd

iii. $f = x1 \cdot \overline{x3} + x1 \cdot x2 \cdot \overline{x3} + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4 + x1 \cdot \overline{x4}$

Minterms not covered: _____

iv. $f = x1 \cdot \overline{x4} + x1 \cdot x2 + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4 + x1 \cdot \overline{x2} \cdot \overline{x3}$

Minterms not covered: _____

Q2, cont'd

(b) Using your knowledge of Boolean algebra simplify the following English statements. Assume that the normal rules of Boolean logic precedence apply to the English. Your answer should be in English.

i. **Statement:** The party will be fun if Mark is there or if Nancy is there and Mark is not.

ANSWER:

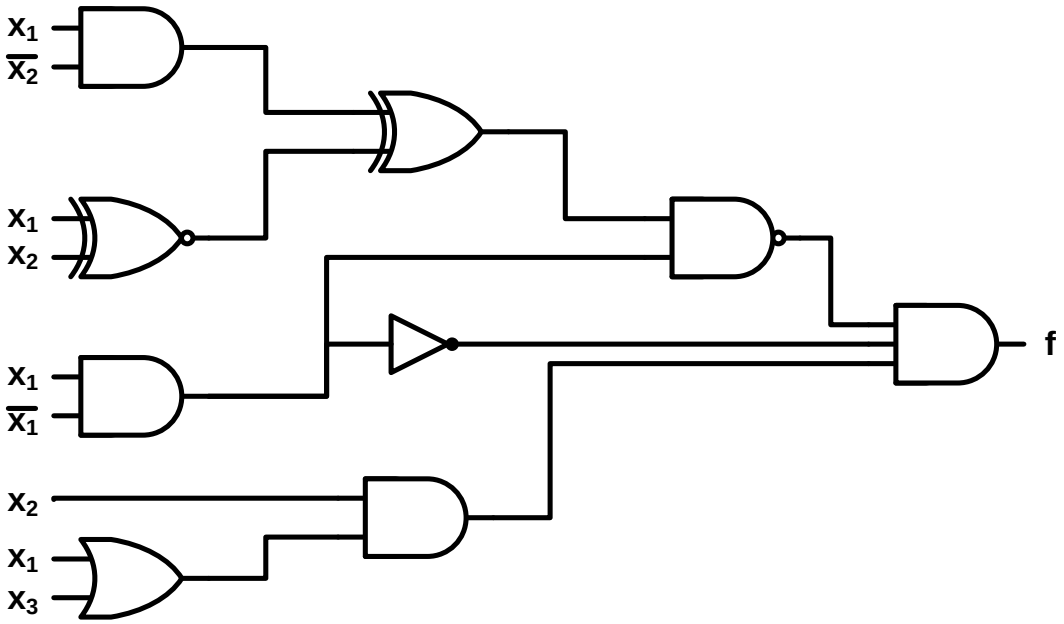
ii. **Statement:** The party will be fun if both Jim and Frank are there or if Lisa is there but Frank is not or if both Jim and Lisa are there.

ANSWER:

Last Name_____Student Number_____

[7] Q3.

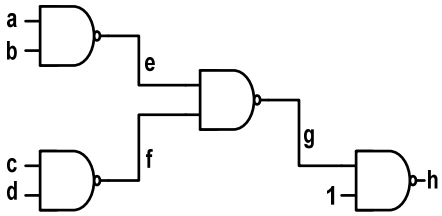
(a) Give the logic function of the circuit below in the **minimal** sum of products form.



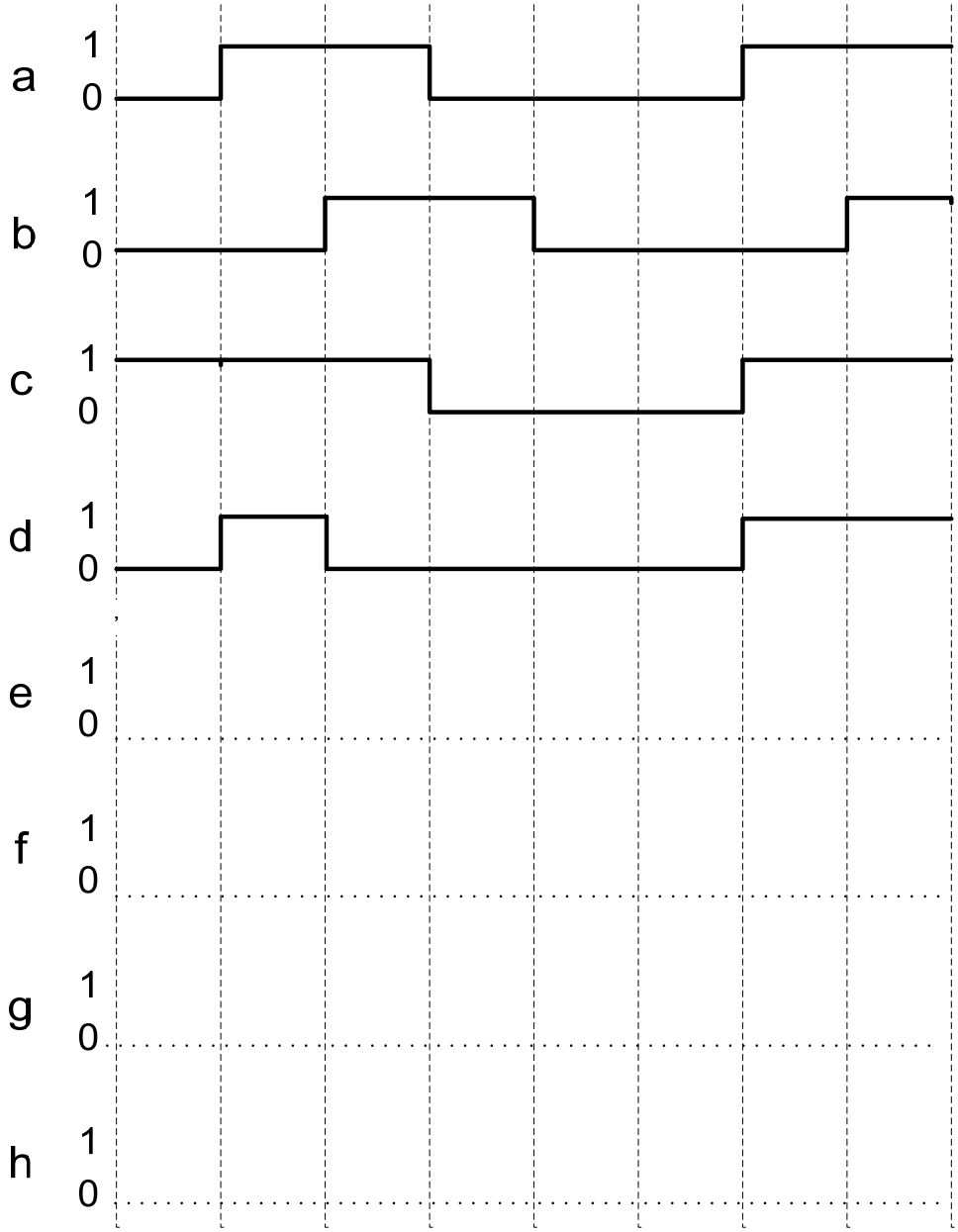
ANSWER:

Q3, continued.

(b) Give the **functional** simulation of the circuit below, using the input waveforms given.



ANSWER:



[8] Q4.

The device that you used in Labs #2 and #3 are called Field-Programmable Gate Arrays (FPGAs) and you created circuits by "downloading" bits into the device from a computer. The FPGA contains a large number of *programmable switches* that permit two wires to be connected. These switches are configured by the download process, after which some connect their related wires and some do not.

The FPGA shown in part (b) below, **uses a 2-input NAND gate as its logic block,** and in part (b) you will be asked to "program" it to implement the following Verilog-described logic circuit:

```
module FPGALogic(A,B,C,F);

input A,B,C;

output F;

assign F = (A & B) | (~C);

endmodule
```

(a) Since the FPGA below uses NAND gate logic blocks, give the simplest schematic (using the fewest NAND gates) of the circuit that implements the above Verilog logic function:

Answer:

(b) Figure 4-2 below illustrates the FPGA to be programmed. Assume that every crossing of two wires can be programmably connected with a programmable switch. Determine which switches in the FPGA must be turned on (programmed to connect the crossed wires) to implement your NAND-gate circuit above. In your answer, to show that a programmed switch should be "connected" draw an X at the intersection of the two wires, as illustrated below in Figure 4-1. **NOTE:** You must use the input/output pads of the chip that are labeled on the outside of the array, and that correspond to the inputs and outputs in the Verilog above. For example the top left pad is F, and so the output of your function must connect to that pad.

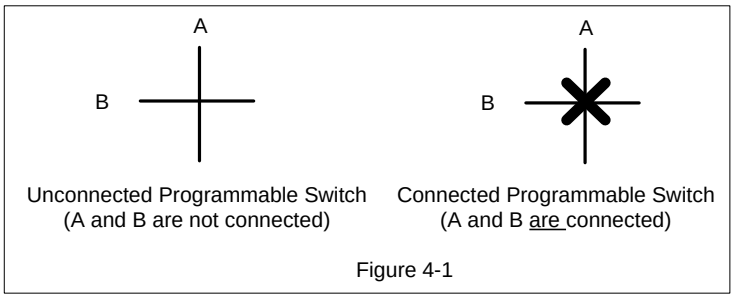


Figure 4-1

Answer:

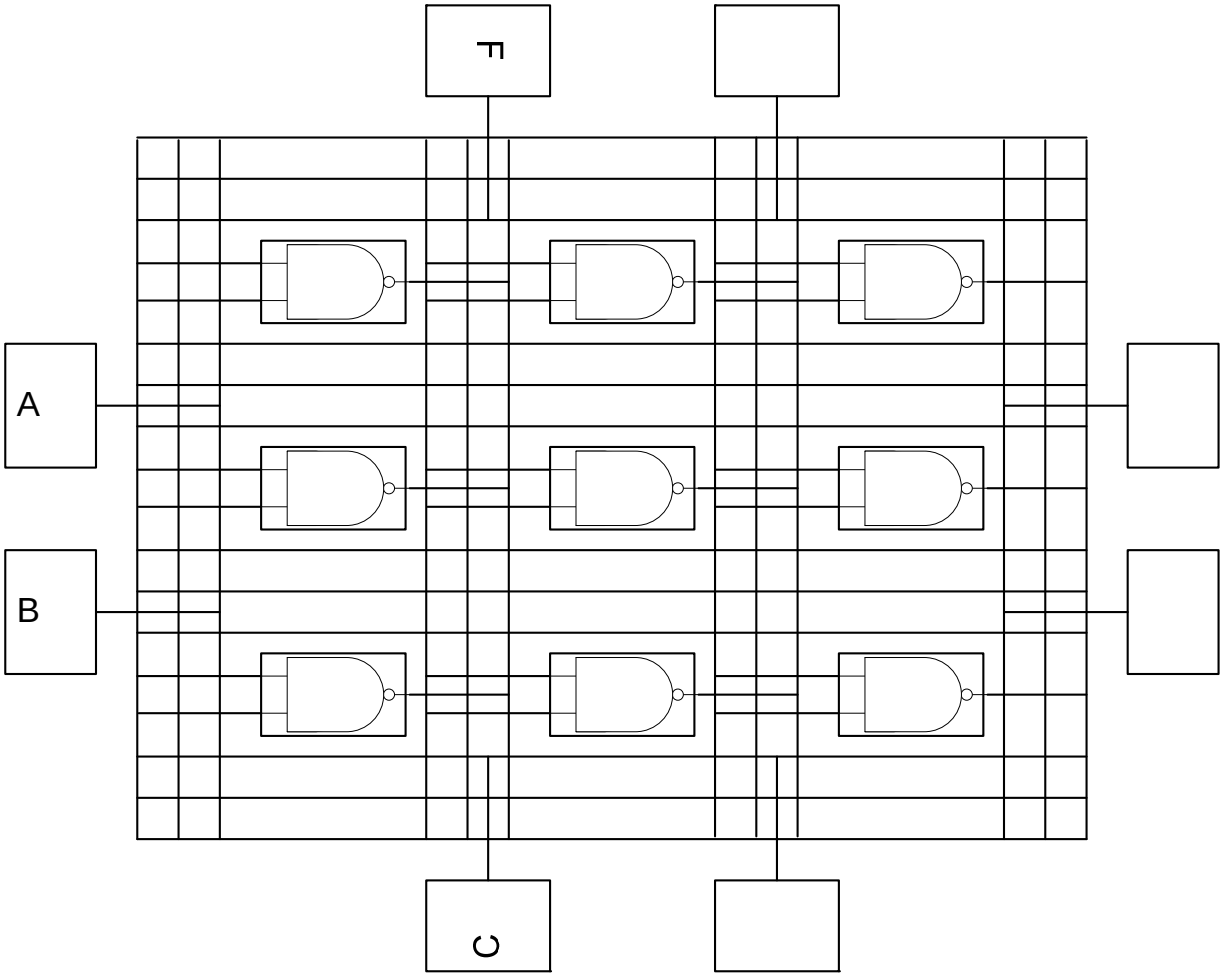


Figure 4-2

[4] Q5.

A car has a low-tire pressure sensor that outputs the current tire pressure as a 4-digit binary number (N_3 N_2 N_1 N_0). The table below shows the 4-digit binary number conversion to the (base 10) tire pressure. Create a circuit that illuminates a "low tire pressure" indicator light (by setting an output **L** to 1) when the tire pressure drops below 8. Full marks will be given to the solution that uses the fewest gates.

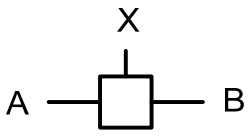
N_3	N_2	N_1	N_0	Tire Pressure
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

ANSWER:

Last Name_____Student Number_____

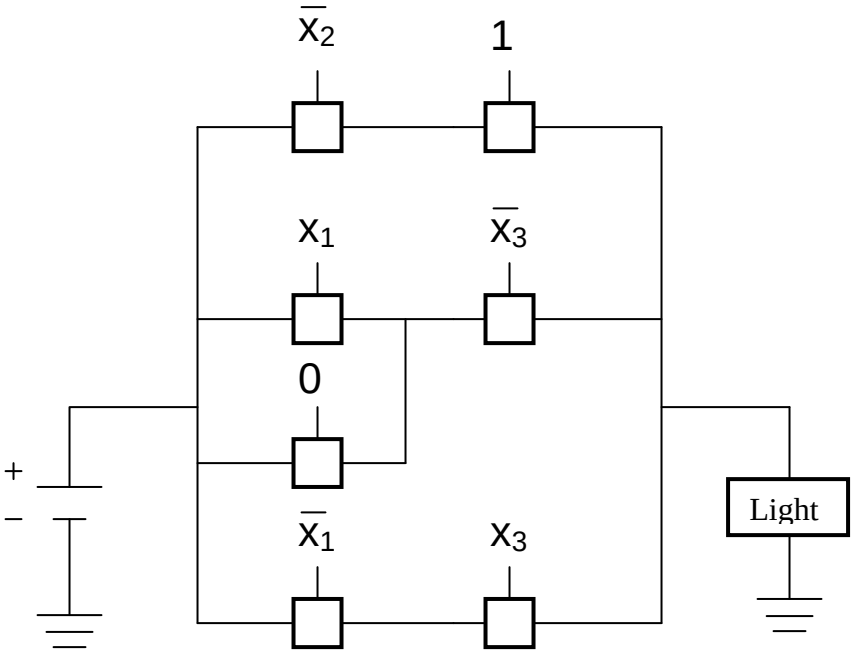
[7] Q6.

Consider the connection of switches shown below. Write a logic expression that corresponds to this circuit and indicates when the light is on (for which the logic expression should evaluate to 1), and off by evaluating to 0. Give the simplest expression sum-of-products form that you can.

Recall that a switch: 

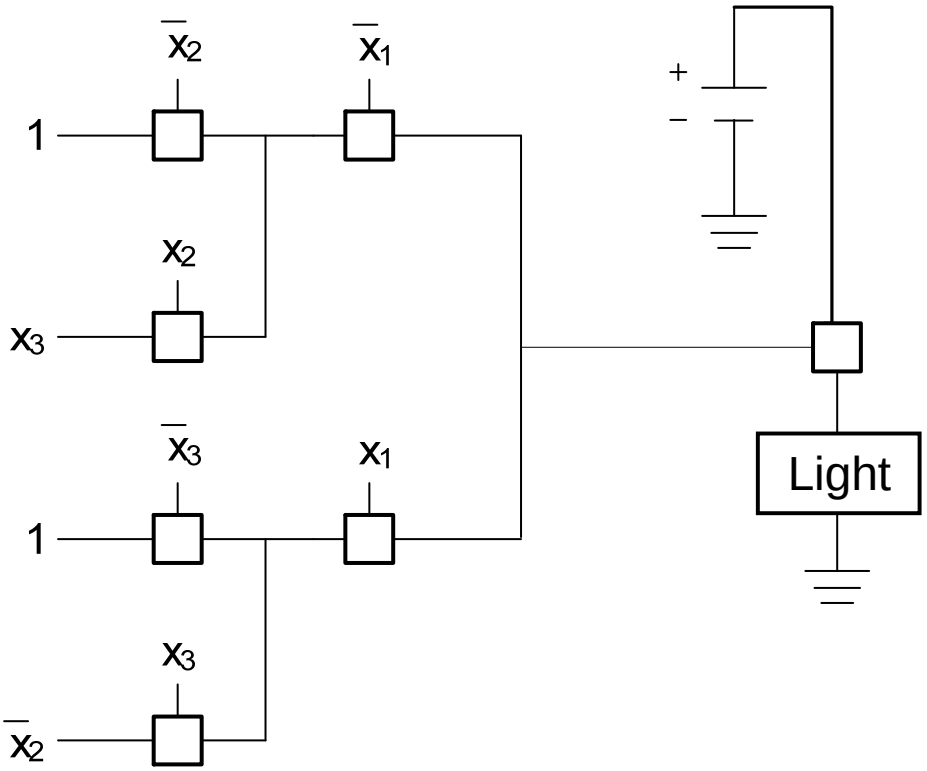
with logical input X, connects the wires A and B when X=1 and leaves them disconnected when X=0.

(a) Circuit:



Logic expression: _____

Q6, continued.
(b) Circuit:



Logic expression: _____

Last Name_____Student Number_____

[9] Q7 For the logic function $f = (x_1 + x_0)(\overline{x_3} + \overline{x_2} + x_1)(\overline{x_3} + \overline{x_1})(x_3 + \overline{x_1} + x_0)$

(a) Fill in the Karnaugh map given below.

x_1x_0 \ x_3x_2	**0 0**	**0 1**	**1 1**	**1 0**
0 0				
0 1				
1 1				
1 0				

(b) Determine the logic expression for the output (f) in the **minimal** (simplest**)** sum-of-product (SOP) form and draw the circuit diagram using only NAND gates to implement the logic. Assume that the inputs are available only in the un-complemented (un-inverted) form.

(c) Determine the logic expression for the output (f) in the **minimal** (simplest) product-of-sum (POS) form.

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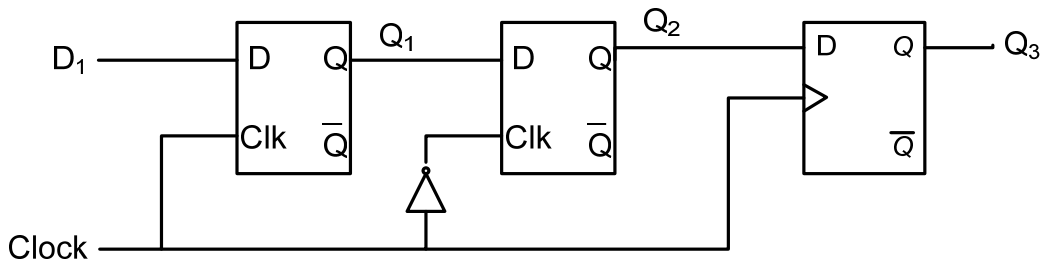
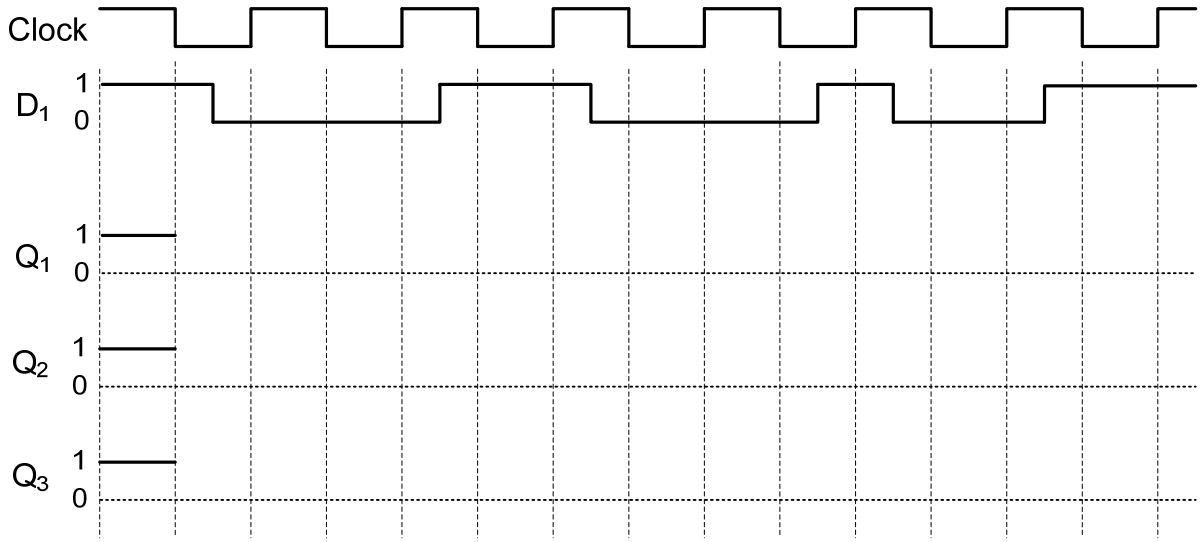
[6] Q8. For the following circuit, complete the functional simulation for outputs Q_1, Q_2 and Q_3 shown below.



Answer:



Last Name_____Student Number_____

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