University of Toronto

Faculty of Applied Science and Engineering

Department of Electrical and Computer Engineering

Midterm Examination

ECE 241F - Digital Systems
Wednesday October 11, 2006, 6:00 – 7:30 pm

Duration: 90 minutes
Examiners: S Brown, J. Rose, K. Truong and B. Wang

ANSWER ALL QUESTIONS ON THESE SHEETS, USING THE BACK SIDE IF NECESSARY.
1. No calculator and no cellphones are allowed.
2. The number of marks available for each question is indicated in the square brackets [].
3. There are two extra blank pages at the end of the test for rough work.

AID ALLOWED: The Course Textbook, **Fundamentals of Digital Logic with Verilog Design.**

Last Name: **SOLUTIONS**

First Name: _____

Student Number: _____

Lecture Section: **Section 01 (Rose) [ ]**
Section 02 (Wang) [ ]
Section 03 (Brown) [ ]
Section 04 (Truong) [ ]

Total Available Marks:

Question	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**Total**
Marks Available	**8**	**9**	**7**	**8**	**4**	**7**	**9**	**6**	**58**
Marks Achieved									

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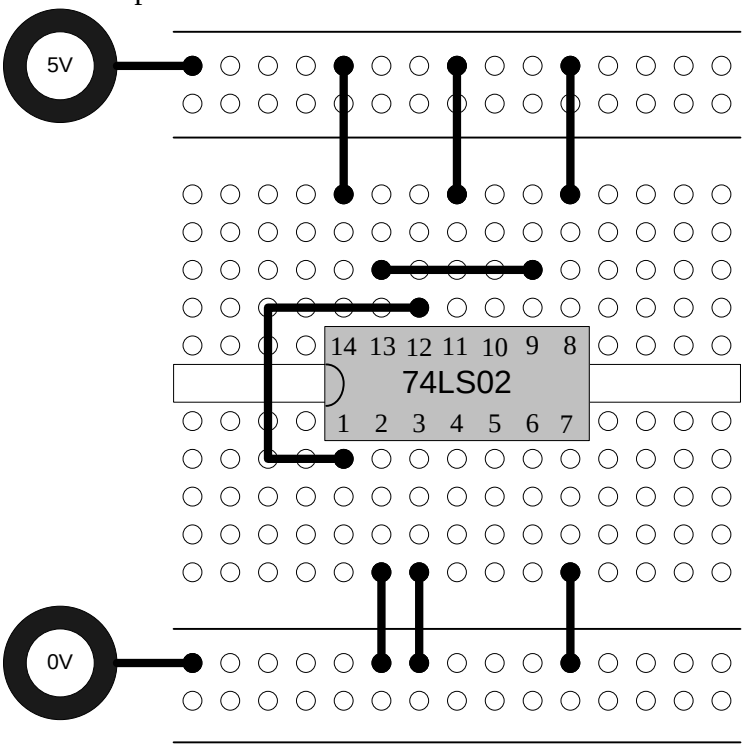
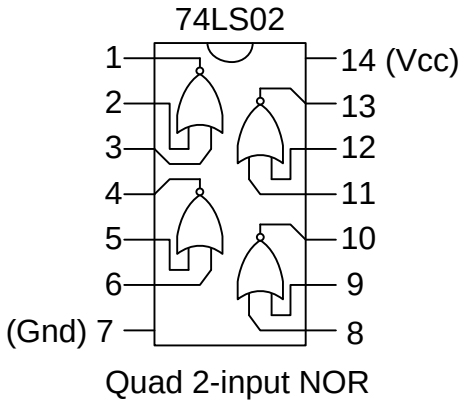
[8] Q1. Lab-Based Question.

The picture below shows the protoboard that you used in Laboratory #1. Its holes are connected as you learned in Lab #1. The board has a TTL 74LS02 Quad 2-input NOR gate chip on it, as shown. The pinout for that chip is given at the right of the picture. There are a number of wires placed on this circuit, as indicated by the black lines. The lines/wires connect only the holes on the protoboard at the ends of the wires, not any of the holes traversed in between. Note also that the inputs of the circuit are connected to either 0V or 5V as opposed to a switch.

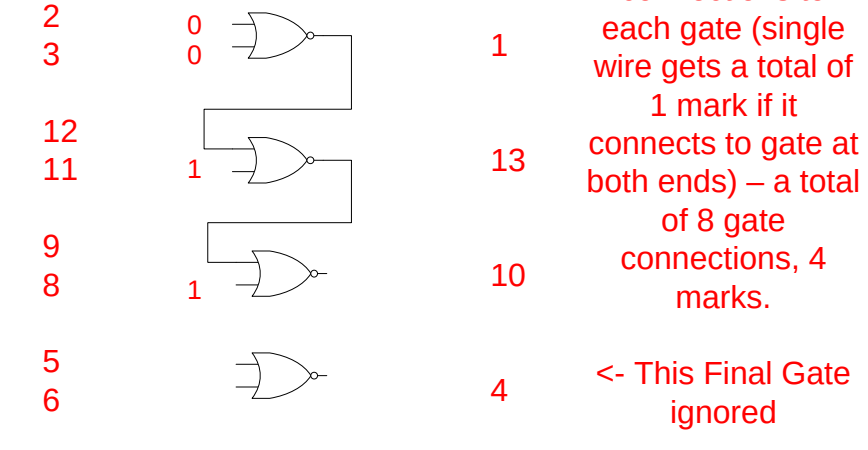




(a) Draw the schematic of the digital circuit that is wired, using the value "1" to represent logic 1 and "0" to represent logic 0 where ever it appears.

Gate with inputs pins 5,6 and output 4 was ignored.

SOLUTION to 1(a)



(b) Assume that a logic probe, just like the one you used in the lab, is correctly powered and touched to the pins of the 74LS02 chip that are indicated in the table below (one at a time, once for each row of the table). In the right hand column of the table indicate what the "output" of the logic probe is when touched to each of the pins (i.e. what the indicator lights on the logic probe would show):

SOLUTION TO 1(B)		
PIN Number	**Logic Probe "Output"**	**Marks**
1	Answer: "High" or "green" or "1"	1
13	Answer: "Low" or "red" or "0"	1
10	Answer: "Low" or "red" or "0"	1
5	Answer: Nothing (no lights light up,)	1 Total 4 marks

For Logic Probe Visual Output:

- if assumptions were stated give full marks if the result is consistent with the assumptions, otherwise part marks
- If the output was specified with both logic state (0s and 1s) and colours, gave marks for correct logic state if colours were either wrong or ambiguous

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[9] Q2.

(a) Consider the logic function $f(x1, x2, x3, x4) = \sum m(0,2,5,8,9,10,12,13,14,15)$. (Note for the minterm numerical labeling that the order of the variables is *x1 x2 x3 x4*). Each of the logic expressions below may or may not implement all of the minterms of this function. Indicate which minterms of the function are not covered (if any) in the space provided. If all minterms *are* covered, then your answer should be "NONE".

Working Space:

i. $f = x1 \cdot \overline{x3} + x1 \cdot x2 + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4$

Minterms not covered: _____

SOLUTION: NONE, worth 1 mark, no part marks

ii. $f = x1 \cdot \overline{x3} + x1 \cdot x2 \cdot x3 + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4$

Minterms not covered: _____

SOLUTION: NONE, worth 1 mark, no part marks

Q2, cont'd

iii. $f = x1 \cdot \overline{x3} + x1 \cdot x2 \cdot \overline{x3} + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4 + x1 \cdot \overline{x4}$

Minterms not covered: _____

SOLUTION: minterm 15 is not covered, worth 1; -0.5 for every additional one not covered

iv. $f = x1 \cdot \overline{x4} + x1 \cdot x2 + \overline{x2} \cdot \overline{x4} + x2 \cdot \overline{x3} \cdot x4 + x1 \cdot \overline{x2} \cdot \overline{x3}$

Minterms not covered: _____

SOLUTION: NONE, worth 1 mark, no part marks

Q2, cont'd

(b) Using your knowledge of Boolean algebra simplify the following English statements. Assume that the normal rules of Boolean logic precedence apply to the English. Your answer should be in English. Write your simplified statement in the answer space.

i. **Statement:** The party will be fun if Mark is there or if Nancy is there and Mark is not.

ANSWER:

Solution: The party will be fun if Mark is there or if Nancy is. 2 marks (No part marks)

ii. **Statement:** The party will be fun if both Jim and Frank are there or if Lisa is there but Frank is not or if both Jim and Lisa are there.

ANSWER:

Solution: The party will be fun if both Jim and Frank are there or if Lisa is there but Frank is not. Worth 3 marks (no part marks)

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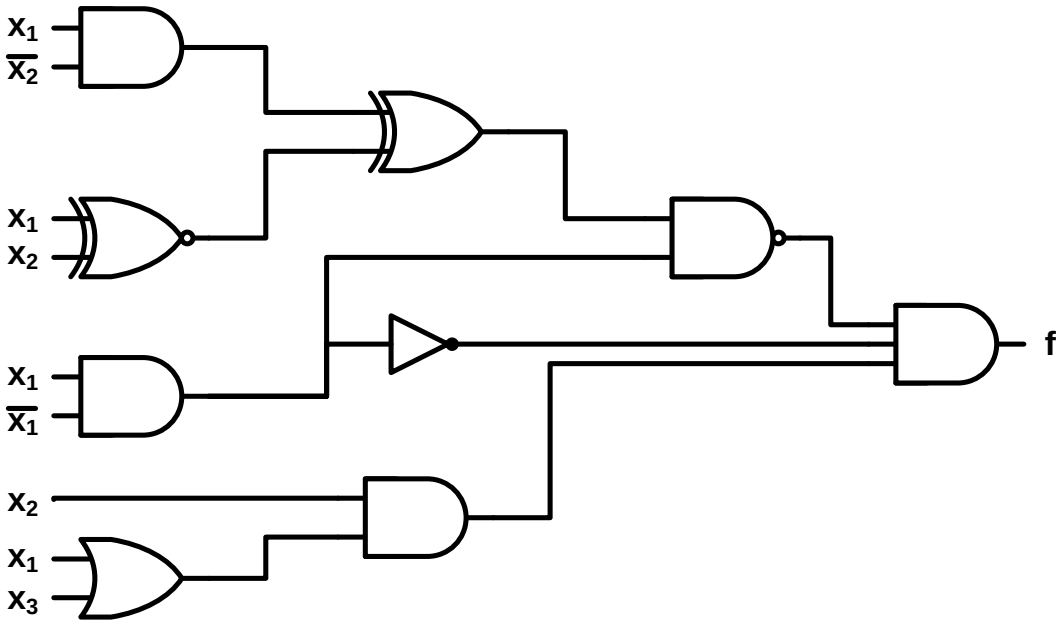
[7] Q3.

(a) Give the logic function of the circuit below in the **minimal** sum of products form.



ANSWER:

SOLUTION to Q3(a):

$f= (x_2)(x_1+x_3)=x_1x_2+x_2x_3$

MARKING SCHEME:

3 marks for the correct minimal SOP form.
2 marks for the correct but not mimimal SOP form.
0-1 marks for varying degrees of a partially correct solution

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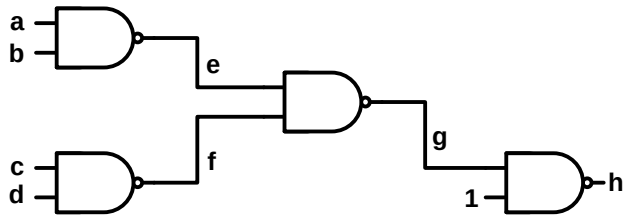
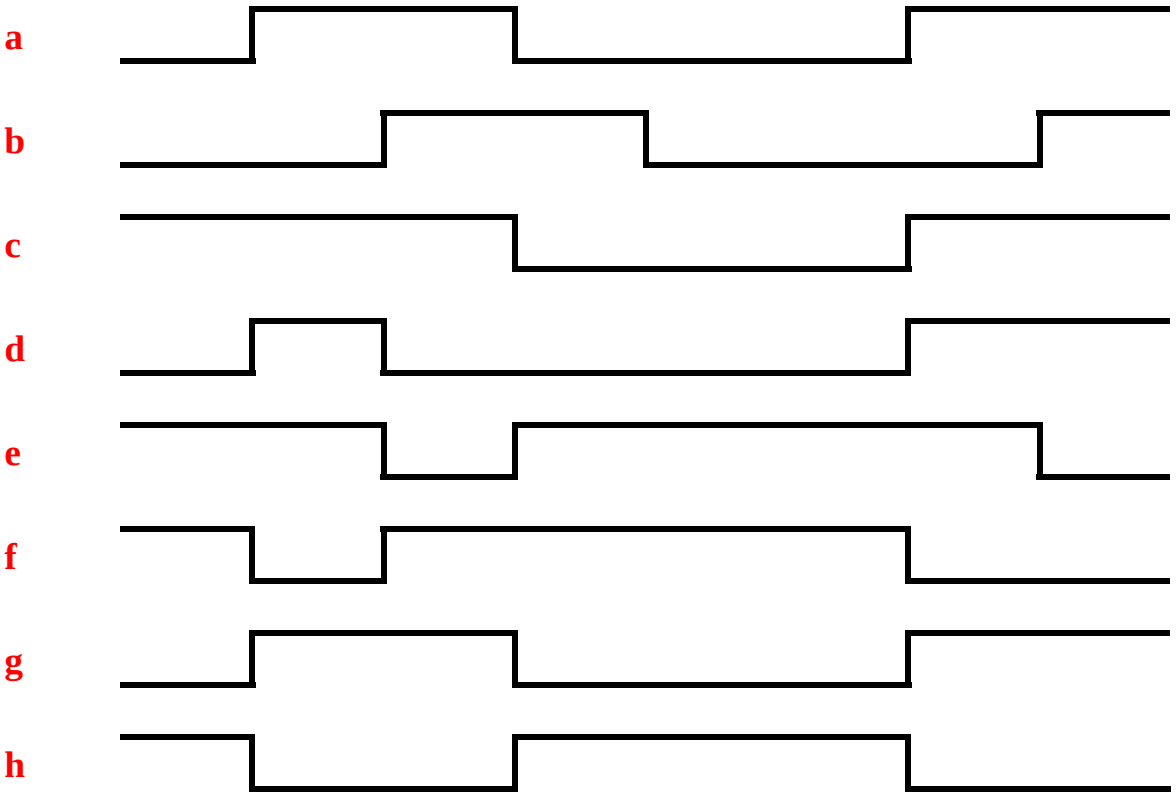
Q3, continued.

(b) Give the **functional** simulation of the circuit below, using the input waveforms given.



ANSWER:

SOLUTION:



MARKING SCHEME:

1 mark for each correct waveform, for a total of 4 marks

In each waveform, -0.5 for each different error, up to a maximum of 1.

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[8] Q4.

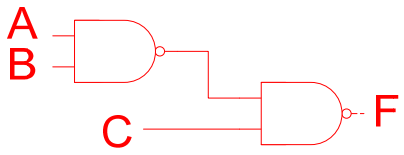
The device that you used in Labs #2 and #3 are called Field-Programmable Gate Arrays (FPGAs) and you implemented circuits by "downloading" bits into the device from a computer. The FPGA contains a large number of *programmable switches*, that permit two wires to be connected. These switches are configured by the download process, after which some connect their related wires and some do not.

The FPGA shown in part (b) below, **uses a 2-input NAND gates as its logic block,** and in part (b) you will be asked to "program" it to implement the following Verilog-described logic circuit:

```
module FPGALogic(A,B,C,F);

input A,B,C;

output F;

assign F = (A & B) | (~C);

endmodule
```

(a) Since the FPGA below uses NAND gate logic blocks, give the simplest schematic (using the fewest NAND gates)of the circuit that implements the above Verilog logic function:

Answer:



Cases:

1. Wrong function without NAND gates =>
   Part a) 0
   Part b) 0
2. Wrong function with NAND gates =>
   Part a) 0
   Part b) -1 for each wrong connection up to 4
3. Correct function without NAND gates =>
   Part a) -1 for each extra gate
   Part b) -1 for each wrong connection
4. Correct function without NAND gates, but optimized
   Part a) 3
   Part b) -1 for each wrong connection
5. Correct function with NAND gates => Part a) 3 Part b) 5
6. Correct function without NAND gates => Part a) 1, Part b) 0

(b) Figure 4-2 below illustrates the FPGA to be programmed. Assume that every crossing of two wires can be programmably connected with a programmable switch. Determine which switches in the FPGA must be turned on (programmed to connect the crossed wires) to implement the circuit above. In your answer, to show that a programmed switch should be "connected" draw an X at the intersection of the two wires, as illustrated below in Figure 4-1. You must use the inputs and outputs of the chip that are labeled on the outside of the array, and that correspond to the inputs and outputs in the Verilog above.

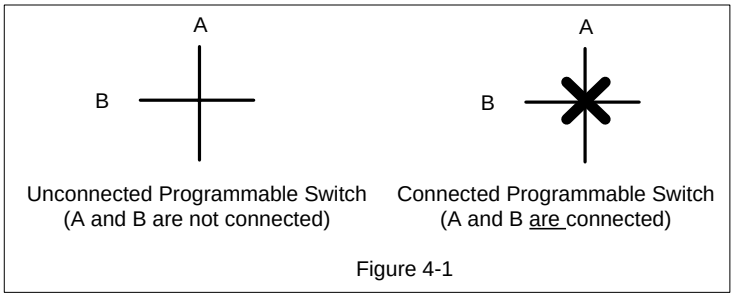
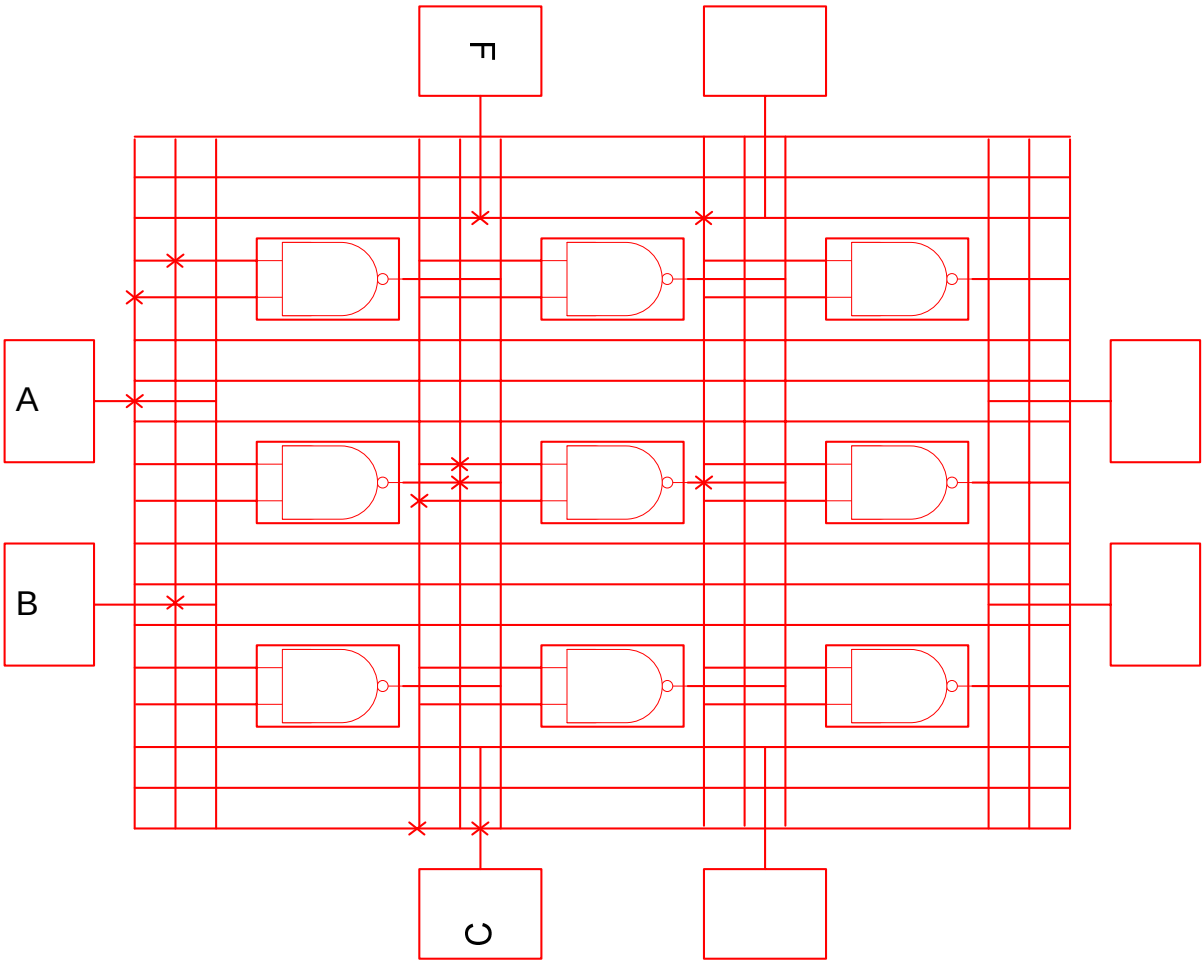


Figure 4-1

Answer:

Solution:



SOLUTION FOR QUESTION 4(b)

Total of 5 marks, minus one for each error, up to a maximum of 5. Marker will have to check each solution to see if it is correct, and if it corresponds to the answer given in part (a).

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[4] Q5.

A car has a low-tire pressure sensor that outputs the current tire pressure as a 4-digit binary number (N_3 N_2 N_1 N_0). The table below shows the 4-digit binary number conversion to the (base 10) tire pressure. Create a circuit that illuminates a "low tire pressure" indicator light (by setting an output **L** to 1) when the tire pressure drops below 8. Full marks will be given to the solution that uses the fewest gates.

N_3	N_2	N_1	N_0	Tire Pressure
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

ANSWER:

SOLUTION to Question 5:

- One solution: A SOP circuit that has 8 products consisting of all the minterms less than 8.
- Best solution: An inverter for the N_3 signal.

MARKING SCHEME:

4 marks for a correct and minimal solution
3 marks for a correct but not minimal solution
-1 for every error in solution, up to the maximum of 4.

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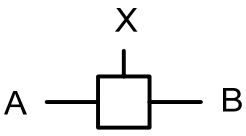
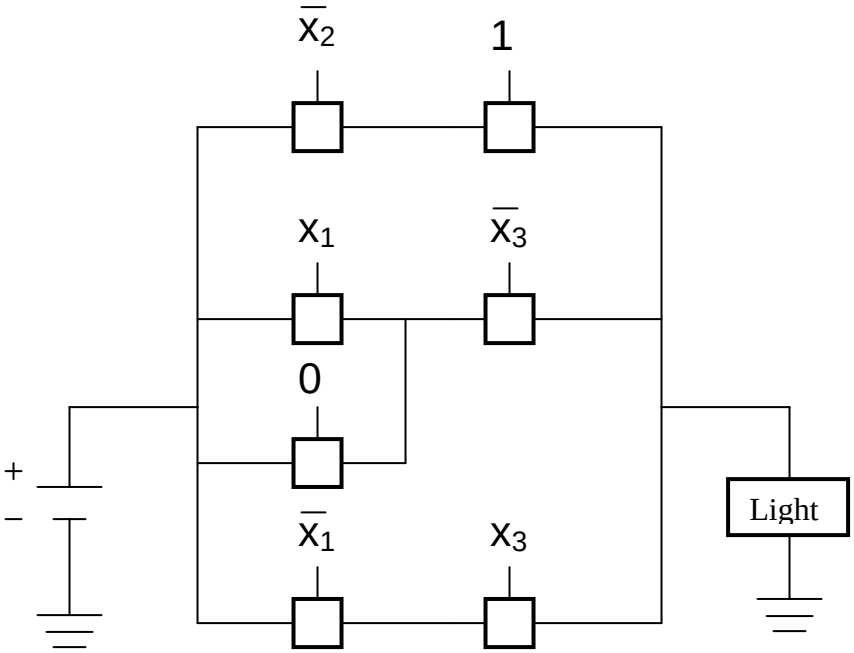
[7] Q6.

Consider the connection of switches shown below. Write a logic expression that that corresponds to this circuit and indicates when the light is on (for which the logic expression should evaluate to 1), and off by evaluating to 0. Give the simplest expression sum-of-products form that you can.

Recall that a switch: 

with input X connects the wires A and B when X=1 and leaves them disconnected when X=0.

(a) Circuit:

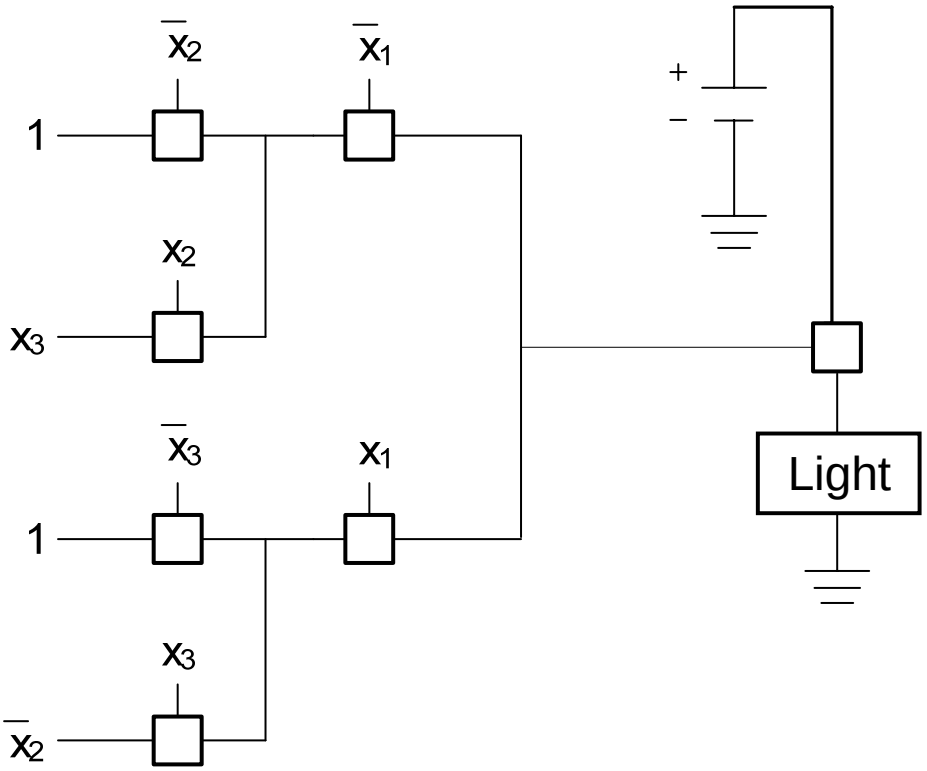


Logic expression: _____

Solution:

1. Logic expression: ____L = ! X2 + X1 !X3 + !X1 X3 (worth 3 marks)
2. Also correct, but not SOP (worth 2 marks) : L = !X2 + (X1 ^ X3). Full marks if solution in point 1 was also present.
3. If correct intermediate step in SOP form, but final solution incorrect, give 1.5 marks.
4. For non-minimal SOP, but correct give 1 mark. E.g. !X2 & 1 + (X1 + 0) !X3 + !X1 X3

Q6, continued.
(b) Circuit:



Logic expression: _____

Logic expression: ____L = ! X2 + X1 !X3 + !X1 X3 (worth 4 marks)

Also correct, but not SOP (worth 3 marks) : L = !X2 + (X1 ^ X3)

For non-minimal SOP, but correct give 1 mark

Give 1 mark if correct but non-SOP.

Subtract 0.5 marks from any of the above in case of any minor typos (missed inversion)

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[9] Q7 For the logic function $f = (x_1 + x_0)(\overline{x_3} + \overline{x_2} + x_1)(\overline{x_3} + \overline{x_1})(x_3 + \overline{x_1} + x_0)$

(a) Fill in the Karnaugh map given below.

x_1x_0 \ x_3x_2	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

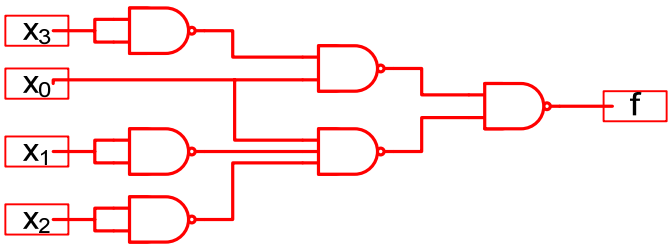
Ans.

x_1x_0 \ x_3x_2	0 0	0 1	1 1	1 0
0 0	0	0	0	0
0 1	1	1	0	1
1 1	1	1	0	0
1 0	0	0	0	0

[3] Marking scheme: -0.5 mark for each wrong "1" entry up to maximum of 3.

(b) Determine the logic expression for the output (f) in the **minimal** (simplest**)** sum-of-product (SOP) form and draw the circuit diagram using only NAND gates to implement the logic. Assume that the inputs are available only in the un-complemented (un-inverted) form.

Ans. $f = \overline{x_3}x_0 + \overline{x_2}\,\overline{x_1}x_0$



Ans.

[4] Marking scheme: 2 marks for the correct expression (-1 for every error up to maximum of 2).
2 marks for the correct circuit diagram (-1 for every error up to maximum of 2). Subtract 0.5 marks if used NAND & NOT gates. Subtract 1 if used NAND and some other gates, subtract 2 if NAND not used. -0.5 if more than 6 NAND gates were used.

(c) Determine the logic expression for the output (f) in the **minimal** (simplest) product-of-sum (POS) form.

Ans. $f = x_0(\overline{x_3} + \overline{x_2})(\overline{x_3} + \overline{x_1})$

[2] Marking scheme: 2 marks for the correct answer.
1 mark for partially correct answer. If SOP = 0 marks. If POS and 0s and 1s are inverted then -1.

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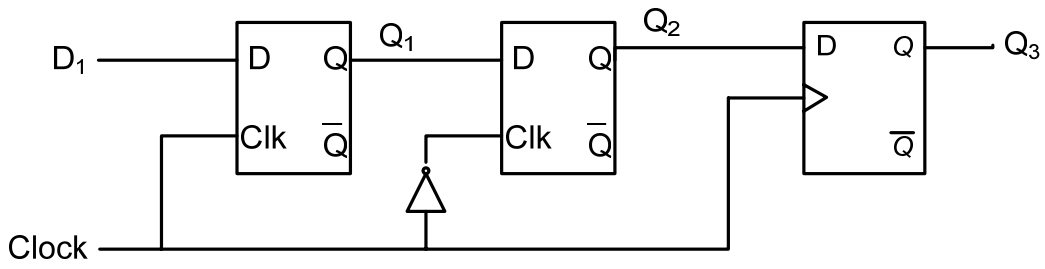
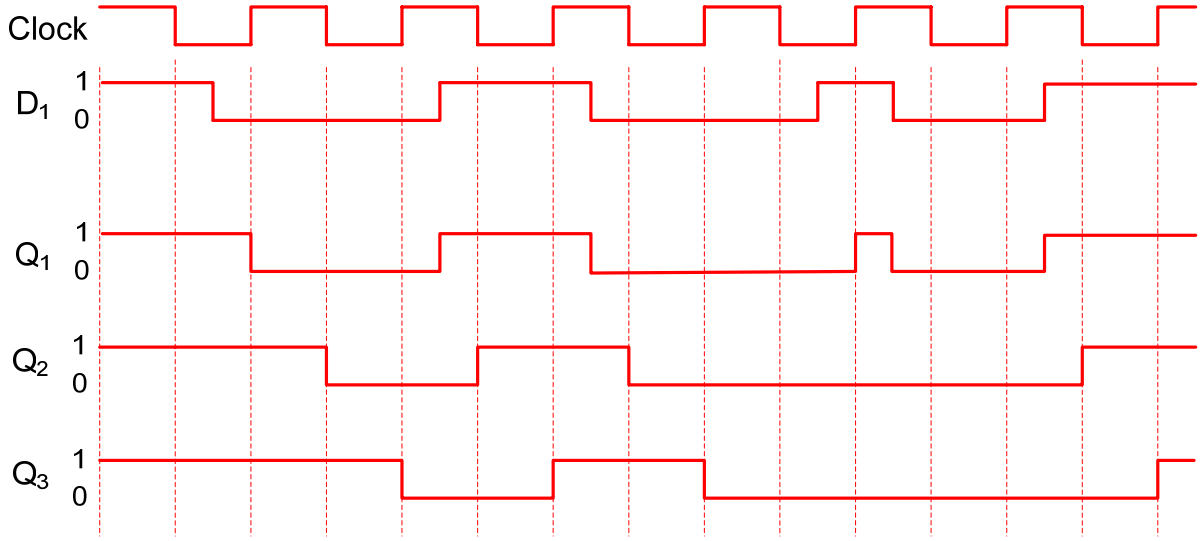
[6] Q8. For the following circuit, complete the functional simulation for outputs Q_1, Q_2 and Q_3 shown below.



Answer:

Solution to Question 9:



Marking scheme: 2 marks each for the correct Q_1, Q_2 and Q_3.
1 mark each for partially correct Q_1, Q_2 and Q_3.