### University of Toronto

## Department of Electrical and Computer Engineering

### ECE241- Digital Systems

#### Midterm Examination

### October 1999

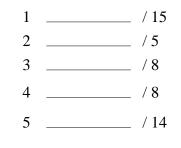
Last Name:	
First Name:	
Student Number:	
Signature:	

Duration: 1.5 Hours

No aids permitted.

Answer ALL questions on this test paper. There is extra space at the end if you need it.

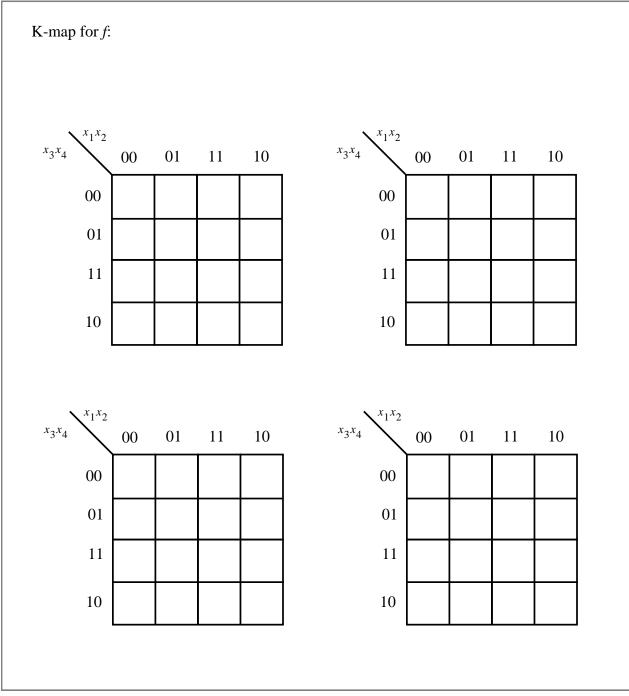
### **EXAMINER's REPORT**

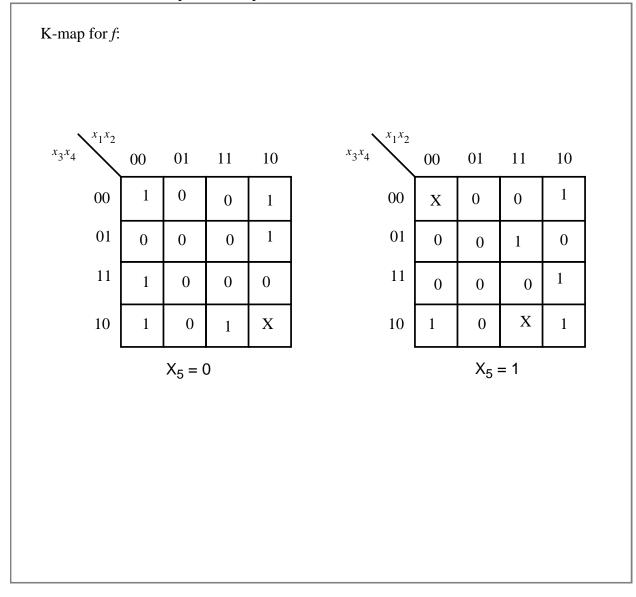


TOTAL: \_\_\_\_\_ / 50

## Question 1 — [15 marks]

**a** Derive the truth table for the following 6-input 1-output function. The six inputs are the variables  $X_1, X_2, X_3, X_4, X_5$ , and  $X_6$ . The output, *f*, should be a 1 when the majority of the inputs (i.e. **more** than half) are a 1. You must put your answer into the K-maps provided below.





**b** For the five-input logic function specified in the below Karnaugh map, determine the minimal cost two-level sum-of-products expression.

Give the minum cost sum-of-products expression for f:

Give the cost, as defined in class, **counting the NOT gates and their inputs**, of this expression:

Cost = \_\_\_\_\_

## Question 2 — [5 marks]

**a** A timing diagram from an Altera maxplus2 timing simulation is shown below. What function was implemented? **Give your answer only as a sum of minterms**.

[1] × [1] y [1] z [0]f	140.0ns 16
[] z	
[0]f	
	3i
NSWER:	

**b** Write the single line of VHDL code necessary to implement the function  $f = xyz + x\bar{y}\bar{z}$ .

ANSWER: \_\_\_\_\_

# Question 3 — [8 marks]

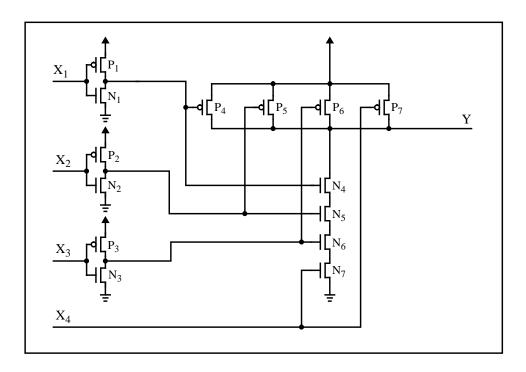
**a** Prove the following theorem:  $xy + yz + \bar{x}z = xy + \bar{x}z$ . Use only boolean logic axioms and identities to simplify the right-hand side into the left-hand side. Show all your steps.

**b** Implement the function  $f = x\bar{y} + \bar{x}z + \bar{y}z$ , using only NOT and AND gates. Give the schematic diagram.

## Question 4 — [8 marks]

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**a** Consider the circuit shown below with the following logic inputs:  $X_1 = X_2 = 1$ ,  $X_3 = X_4 = 0$ . Write the state of each transistor (i.e. ON or OFF) in the table below. Also, give the logic level at the output, Y



Transistor	State (i.e. ON or OFF)	Transistor	State (i.e. ON or OFF)
P <sub>1</sub>		N <sub>1</sub>	
P <sub>2</sub>		N <sub>2</sub>	
P <sub>3</sub>		N <sub>3</sub>	
P <sub>4</sub>		N <sub>4</sub>	
P <sub>5</sub>		N <sub>5</sub>	
P <sub>6</sub>		N <sub>6</sub>	
P <sub>7</sub>		N <sub>7</sub>	

Logic level at Y: \_\_\_\_

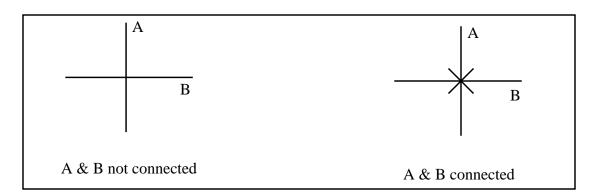
**b** For circuit above, write a logic expression for Y in terms of  $X_1$ ,  $X_2$ ,  $X_3$  and  $X_4$ .

ANSWER:		

**c** Draw the transistor-level schematic of another **CMOS logic** network which implements the same truth table as the circuit above using the fewest possible transistors.

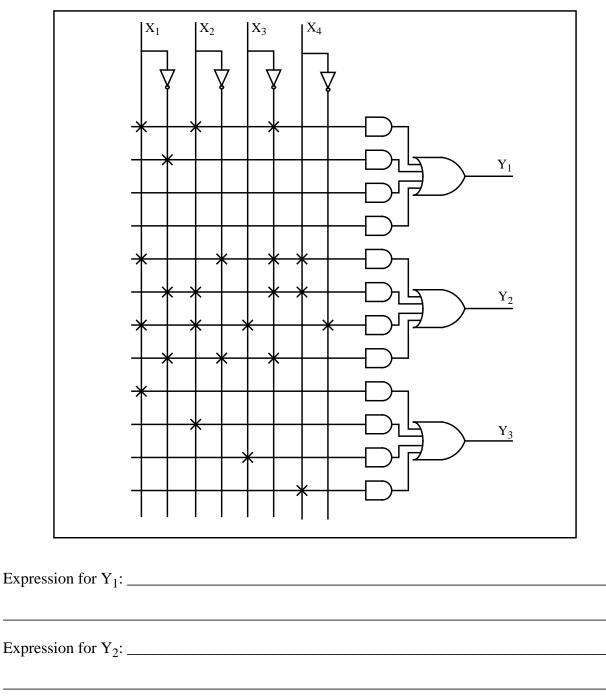
## Question 5 — [14 marks]

**READ THIS CAREFULLY:** Throughout this question, the following convention will be used to represent the state of programmable switches in a Programmable Logic Device (PLD):



That is, in both cases there is a programmable switch attached between wire A and wire B.

**a** Write a simple **sum-of-products** expression for each output in the following PLD (no simplification is necessary).



Expression for Y<sub>3</sub>: \_\_\_\_\_

- **b** Using the convention stated above, fill in the schematic diagram on the next page to iimplement the following logic specifications (**NOTE: the PLD has a NOR-NOR structure**):
  - $Y_1$  should be low (0) when all four inputs (i.e.  $X_1$ ,  $X_2$ ,  $X_3$ , and  $X_4$ ) are the same. Otherwise,  $Y_1$  should be high (1).
  - $Y_2 = \overline{(\overline{X_1}X_4 + X_2\overline{X_3})}$
  - Y<sub>3</sub> is specified by the following truth table:

X <sub>1</sub>	X <sub>2</sub>	X <sub>3</sub>	X <sub>4</sub>	Y <sub>3</sub>
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

