S7 Software Configurable Processor

RISC Processor
367 MHz
32-bit RISC

Wide Registers
32 x 128b Wide Registers + Flexible Wide Load/Store Instructions

ISEF
Programmable Logic Datapath Inside the Processor

ISEF Resources
- 1024 4-bit ALUs
- 32 16-bit Multipliers
- 64 KBytes IRAM
- 6 Kbits Registers

ISEF Reconfig
- 20usec

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C-Based Design Entry

APPLICATION C/C++

ANNOTATED C/C++

main ( ) {
    ...
}

kernel1( x,y,z)

kernel2( )

kernel2(......) {
    ...
}

UNIT DESIGNER

COMPILER

EXECUTABLE

MEMORY SYSTEM

CONTROL

32-BIT RF

ISEF BIT STREAM

ALU

FPU

Xtensa-LX 367 MHz 32-bit RISC Processor

ISEF Programmable Logic Datapath *Inside* the Processor

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S7000 For All Surveillance Needs

D1 Multi-Stream Video Servers
- 2x S7100: 32 Channel
- S7100: 16 Channel
- S7110: 12 Channel
- S7120: 6 Channel

D1 Multi-Stream Hybrid DVRs
- S7100: 16 Channel
- S7110: 12 Channel
- S7120: 8 Channel
- S7120: 4 Channel

Multi-Stream WDR IP Cameras
- 2x S7100: 5Mpixel @ 30fps
- S7100: 1080p60
- S7100: 1080p30

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