Prof. David A. Johns

CV Date	December 29, 2020
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Research Interests	Analog Integrated Circuits, Analog-to-Digital Converters, Digital-to-Analog Converters, Filters, Low Power Electronics, High-Speed Serial Links

Education

University of Toronto, Toronto, Ontario, Canada

Ph.D., Electrical Engineering, 1989

- Thesis: *Analog and Digital State-Space Adaptive IIR Filters*
- Advisors: Martin Snelgrove and Adel Sedra

M.A.Sc., Electrical Engineering, 1983

- Topic: *State-Space Filters Based on LC Ladder Simulation*
- Advisor: Adel Sedra

B.A.Sc., Engineering Science, 1980

Academic Experience

Professor 1998 to present
Dept of Elec and Comp Eng,
University of Toronto

Associate Professor 1994 to 1998
Dept of Elec and Comp Eng,
University of Toronto

Assistant Professor 1989 to 1994
Dept of Elec and Comp Eng,
University of Toronto

Lecturer 1988 to 1989
Dept of Elec and Comp Eng,
University of Toronto

Industrial Experience

Vice-President IP Division 2007 to 2008
Gennum Corp, Ontario
(on leave from UofT)

Vice-President 2003 to 2007
Snowbush Corp, Ontario,
(part-time)

Vice-President 2002 to 2003
Snowbush Corp, Ontario
(1 year research leave)

Vice-President 1998 to 2002
Snowbush Corp, Ontario
(part-time)

Visiting Researcher 1995 to 1996
Brooktree Corp, San Diego
(1 year research leave)

IC Design Engineer 1983 to 1985
Pacific Microcircuits, Vancouver

Applications Engineer 1980 to 1981
Mitel Corp, Ottawa

Awards and Honours

- Elected to **Fellow of the Canadian Academy of Engineering** (CAE), 2012.
- I. Ahmed and D.A. Johns, "An 11-bit 45MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage", European Solid-State Circuits Conference, Munich, Germany, Sept. 2007. *This paper was recipient of the 'Young Scientist Award' (best student paper for works published at ESSCIRC 2007)
- First place award for student design contest for DAC/ISSCC, 2005 for paper entitled "A 50MS/s (35mW) to 1kS/s (15uW) power scaleable 10b pipelined ADC with minimal bias current variation" by Imran Ahmed and D.A. Johns.
- Evening session award for "Are startups killing innovation" at ISSCC, 2002. Panel moderator.
- Elected to **IEEE Fellow** in 2001 "For contributions to the theory and design of analog integrated circuits used in digital communications".
- Co-recipient of the **1999 IEEE Darlington Best Paper Award** for the paper entitled "BiCMOS circuits for analog Viterbi decoders",

Trans on CAS, Dec. 1998. Co-authors were H. Shakiba and K. Martin.

- Recipient of the 1999 Gordon Slemon Teaching Award (A departmental award)
- Co-recipient of 1999 ISCAS student competition paper award (3rd place) for paper entitled "A multilevel modulation scheme for high-speed wireless infrared communications". Co-author was S. Hranilovic.
- Co-recipient of 1993 CMC Design Award (with A. Shoval and M. Snelgrove)

Textbooks

[1] T. Chan Carusone, D. A. Johns, and K. Martin, *Analog Integrated Circuit Design*. NY, NY: Wiley, 2 ed., 2011

[2] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. NY, NY: Wiley, 1 ed., 1997 **Adopted by over 40 universities. More than 40,000 copies sold.**

Chapters in Textbooks

[3] A. Carusone and D. A. Johns, "Design of high frequency integrated analogue filters," *Analogue adaptive filters, London, United Kingdom: The Institute of Electrical Engineers, Circuits, Devices and Systems, Series*, vol. 14, pp. 161–195, 2002

Journal Publications

[4] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A third-order integrated passive switched-capacitor filter obtained with a continuous-time design approach," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 10, pp. 3643–3652, 2019

[5] S. Amini and D. A. Johns, "A normalized figure of merit for capacitive accelerometer interface circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2019

[6] S. Ahsanuzzaman, A. Parayandeh, A. Prodić, and D. A. Johns, "A building block ic for designing emerging hybrid and multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 500–514, 2018

[7] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A simplified model for passive-switched-capacitor filters with complex poles.," *IEEE Trans. on Circuits and Systems*, vol. 63, no. 6, pp. 513–517, 2016

[8] S. Ahsanuzzaman, A. Prodić, and D. A. Johns, "An integrated high-density power management solution for portable applications based on a multioutput switched-capacitor circuit," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4305–4323, 2016

[9] S. Amini and D. A. Johns, "A flexible charge-balanced ratiometric open-loop readout system for capacitive inertial sensors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 4, pp. 317–321, 2015

[10] A. Nilchi and D. A. Johns, "A low-power delta-sigma modulator using a charge-pump integrator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1310–1321, 2013

[11] I. Ahmed, J. Mulder, and D. A. Johns, "A low-power capacitive charge pump based pipelined adc," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1016–1027, 2010

[12] A. Nilchi and D. Johns, "Charge-pump based switched-capacitor integrator for delta sigma modulators," *Electronics letters*, vol. 46, no. 6, pp. 400–401, 2010

[13] T. C. Caldwell and D. A. Johns, "Incremental data converters at low oversampling ratios," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1525–1537, 2010

[14] A. Gharbiya and D. A. Johns, "A 12-bit 3.125 mhz bandwidth 0–3 mash delta-sigma modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 2010–2018, 2009

[15] A. Gharbiya and D. A. Johns, "Combining multipath and single-path time-interleaved delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 12, pp. 1224–1228, 2008

[16] K. Farzan and D. A. Johns, "A robust 4-pam signaling scheme for inter-chip links using coding in space," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 16, no. 11, pp. 1535–1544, 2008

[17] I. Ahmed and D. A. Johns, "An 11-bit 45 ms/s pipelined adc with rapid calibration of dac errors in a multibit pipeline stage," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1626–1637, 2008

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[19] T. C. Caldwell and D. A. Johns, "A time-interleaved continuous-time/spl delta//spl sigma/modulator with 20-mhz signal bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1578–1588, 2006

[20] A. Gharbiya and D. A. Johns, "On the implementation of input-feedforward delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 6, pp. 453–457, 2006

[21] K. Farzan and D. A. Johns, "Coding schemes for chip-to-chip interconnect applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 4, pp. 393–406, 2006

[22] I. Ahmed and D. A. Johns, "A 50-ms/s (35 mw) to 1-ks/s (15/spl mu/w) power scaleable 10-bit pipelined adc using rapid power-on opamps and minimal bias current variation," *IEEE journal of solid-state circuits*, vol. 40, no. 12, pp. 2446–2455, 2005

[23] A. Gharbiya, T. C. Caldwell, and D. Johns, "High-speed oversampling analog-to-digital converters," *International journal of high speed Electronics and systems*, vol. 15, no. 02, pp. 297–317, 2005

[24] K. Farzan and D. A. Johns, "A cmos 10-gb/s power-efficient 4-pam transmitter," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, pp. 529–532, 2004

[25] A. C. Carusone and D. A. Johns, "Digital lms adaptation of analog filters without gradient information," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 9, pp. 539–552, 2003

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[30] A. Carusone and D. A. Johns, "Analogue adaptive filters: past and present," *IEE Proceedings-Circuits, Devices and Systems*, vol. 147, no. 1, pp. 82–90, 2000

[31] K. Phang and D. A. Johns, "A cmos optical preamplifier for wireless infrared communications," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 7, pp. 852–859, 1999

[32] M. Shakiba, D. A. Johns, and K. W. Martin, "Bicmos circuits for analog viterbi decoders," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 12, pp. 1527–1537, 1998. **This paper won the IEEE Darlington Best Paper Award for IEEE Trans. on Circuits and Systems.**

[33] M. H. Shakiba, D. A. Johns, and K. W. Martin, "An integrated 200-mhz 3.3-v bicmos class-iv partial-response analog viterbi decoder," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 61–75, 1998

[34] D. A. Johns and D. Essig, "Integrated circuits for data transmission over twisted-pair channels," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 398–406, 1997

[35] R. Khoini-Poorfard, L. B. Lim, and D. A. Johns, "Time-interleaved oversampling a/d converters: Theory and practice," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 8, pp. 634–645, 1997

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[44] K. A. Kozma, D. A. Johns, and A. S. Sedra, "Tuning of continuous-time filters in the presence of parasitic poles," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 40, no. 1, pp. 13–20, 1993

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[46] D. Johns and D. Lewis, "Iir filtering on sigma-delta modulated signals," *Electronics letters*, vol. 27, no. 4, pp. 307–308, 1991

[47] K. A. Kozma, D. A. Johns, and A. S. Sedra, "Automatic tuning of continuous-time integrated filters using an adaptive filter technique," *IEEE Transactions on Circuits and Systems*, vol. 38, no. 11, pp. 1241–1248, 1991. **This paper is included in an IEEE Press Book entitled "Integrated Continuous-Time Filters"**

[48] D. A. Johns, W. M. Snelgrove, and A. S. Sedra, "Continuous-time lms adaptive recursive filters," *IEEE Transactions on Circuits and Systems*, vol. 38, no. 7, pp. 769–778, 1991

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CONFERENCE PUBLICATIONS

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[54] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A 150-μw 3 rd-order butterworth passive-switched-capacitor filter with 92 db sfdr," in *VLSI Circuits, 2017 Symposium on*, pp. C142–C143, IEEE, 2017

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[59] A. Nilchi and D. A. Johns, "Charge-pump based switched-capacitor gain stage," in *Circuits and Systems (MWSCAS), 2012 IEEE 55th International Midwest Symposium on*, pp. 306–309, IEEE, 2012

[60] J. Liang and D. A. Johns, "A frequency-scalable 15-bit incremental adc for low power sensor applications," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pp. 2418–2421, IEEE, 2010

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[65] A. O. Nafee and D. A. Johns, "A 14-bit micro-watt power scalable automotive mems pressure sensor interface," in *Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European*, pp. 450–453, IEEE, 2008

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[68] T. C. Caldwell and D. A. Johns, "An incremental data converter with an oversampling ratio of 3," in *Research in Microelectronics and Electronics 2006, Ph. D.*, pp. 125–128, IEEE, 2006

[69] T. C. Caldwell and D. A. Johns, "A high-speed technique for time-interleaving continuous-time delta-sigma modulators," in *Research in Microelectronics and Electronics, 2005 PhD*, vol. 1, pp. 101–104, IEEE, 2005

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[71] A. Gharbiya and D. Johns, "Mixed-mode input feedforward delta-sigma modulator," in *Circuits and Systems, 2005. 48th Midwest Symposium on*, pp. 688–691, IEEE, 2005

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[74] I. Ahmed and D. Johns, "A 50 ms/s (35 mw) to 1 ks/s (15/spl mu/w) power scaleable 10b pipelined adc with minimal bias current variation," in *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, pp. 280–598, IEEE, 2005

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[111] A. Shoval, D. Johns, and W. Snelgrove, "A wide-range tunable bicmos transconductor," in *CCVLSI*, (Halifax, Nova Scotia), pp. 81–88, 1992

[112] D. Johns and D. Lewis, "Sigma-delta based iir filters," in *Circuits and Systems, 1991., Proceedings of the 34th Midwest Symposium on*, pp. 210–213, IEEE, 1991

[113] D. Johns, W. Snelgrove, and A. Sedra, "Performance improvements for fine-tuned adaptive recursive filters," in *IEEE International Symposium on Circuits and Systems*, pp. 1951–1954, 1990

[114] K. Kozma, D. A. Johns, and A. Sera, "An adaptive tuning circuit for integrated continuous-time filters," in *Circuits and Systems, 1990., IEEE International Symposium on*, pp. 1163–1166, IEEE, 1990

[115] X. F. Wania, D. Johns, and A. Sedra, "Programmable multiplexed switched-capacitor filters," in *Circuits and Systems, 1990., Proceedings of the 33rd Midwest Symposium on*, pp. 973–976, IEEE, 1990

[116] X. Gao, W. Snelgrove, and D. Johns, "Nonlinear iir adaptive filtering using a bilinear structure," in *Circuits and Systems, 1989., IEEE International Symposium on*, pp. 1740–1743, IEEE, 1989

[117] D. Johns, W. Snelgrove, and A. Sedra, "Continuous-time analog adaptive recursive filters," in *Circuits and Systems, 1989., IEEE International Symposium on*, pp. 667–670, IEEE, 1989

[118] D. Johns, W. Snelgrove, and A. Sedra, "Dc offsets in analogue adaptive iir filters," in *Circuit Theory and Design, 1989., European Conference on*, pp. 137–141, IET, 1989

[119] D. Johns, W. Snelgrove, and A. Sedra, "Nonideal effects in continuous-time adaptive recursive filters," in *Circuits and Systems, 1989., Proceedings of the 32nd Midwest Symposium on*, pp. 594–597, IEEE, 1989

[120] D. Johns, W. Snelgrove, and A. Sedra, "State-space adaptive recursive filters," in *Circuits and Systems, 1988., IEEE International Symposium on*, (Helsinki, Finland), pp. 2153–2156, IEEE, 1988

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Ph.D. Graduate Students Supervised

1. Zeynep Lulec, "in progress". Jointly supervised with Prof. Liscidini.
2. Saber Amini, "A Variable Gain Direct Digital Readout System for Capacitive Inertial Sensors", 2017
3. S.M. Ahsanuzzaman, "High-density Power Management Architecture for Portable Applications," 2015. Jointly supervised with Prof. Prodic
4. Alireza Nilchi, "Low-power charge-pump based switched-capacitor circuits," 2013.

5. Trevor Caldwell, "Delta-sigma modulators with low oversampling ratios," 2010.

6. A. Gharbiya, "Architecture alternatives for time-interleaved and input-feedforward delta-sigma modulators," 2008.

7. I. Ahmed, "Pipelined ADC enhancment techniques," 2008.

8. Kamran Farzan, "Space coding applied to high-speed chip-to-chip interconnects", 2005.

9. Amir Hadji-Abdolhamid, "Partial analog equalization and ADC requirements in wired communications", 2004.

10. Takis Zourntos, "Compensation of delta-sigma modulators: Stabilization, signal restoration, and integrated circuits," 2003.

11. Anthony Chan Carusone, "Digital algorithms for analog adaptive filters," 2002.

12. Bahram Zand, "High-speed optical wireless communications using reduced-state sequence detection," 2002

13. Khoman Phang, "CMOS optical preamplifier design using graphical circuit analysis," 2001.

14. Hossein Shakiba, "Analog Viterbi detection for partial-response signalling", 1997.
Jointly supervised with Prof. K. Martin.

15. Karen Kozma, "Theory and application for the adaptive tuning of continuous-time integrated filters," 1996.
Jointly supervised with Prof. A.S Sedra.

16. Ayal Shoval, "Analog adaptive filtering techniques for high-speed data communications," 1995.
Jointly supervised with Prof. W.M. Snelgrove.

17. Ramin Khoini-Poorfard, "Analysis methods and time-interleaved architectures for oversampling modulators," 1994.

M.A.Sc. Graduate Students Supervised

18. Aggarwal, Mayank, "Power reduction for 112Gb/s serdes", 2018 (start date)

19. Zhong Hong Jiang, "A low-power sub-GHz RF receiver front-end with enhanced blocker tolerance", 2017. Jointly supervised with Prof. Liscidini.

20. Kei-Ming Kwong, "MEMS Accelerometer Specifications and Their Impact in Inertial Applications", 2017.

21. Hao Yan, "An Open Source Inertial Sensor Network with Bluetooth Smart", 2014

22. Rene Rail-Ip, "Evaluation of low cost MEMS accelerometers and investigation of inertial algorithms for dead reckoning in railway enviroments", 2014

23. Colin Tse, "Design of a power scalable capacitive MEMS accelerometer front end", 2013.

24. Guangzhao (Andy) Zhang, "A low-power pipeline ADC with front-end capacitor-sharing", 2012.

25. Joshua Liang, "A frequency-scalable 14-bit ADC for low power sensor applications", 2009.

26. Akram Nafee, "Design of a high accuracy power scalable MEMS sensor interface", 2008.

27. Robert Wang, "A low voltage low power 10-bit pipeline ADC in 90nm digital CMOS technology", 2004. Jointly supervised with Prof. KW Martin

28. Navid Yaghini, "Design of a wideband quadrature continuous-time delta-sigma ADC", 2004.

29. Imran Ahmed, "A power scaleable and low power pipeline ADC using power resettable opamps", 2004.

30. Trevor C. Caldwell, "Time-interleaved continuous-time delta-sigma modulators", 2004.

31. Samira Naraghi, "A 4-bit analog-to-digital converter for high-speed serial links", 2004.

32. Paul-Hugo Lamarche, "Field-programmable analog array implemented using delta-sigma based digital signal processing", 2003.

33. Sherif Abdalla, "A 7.2 Gb/s/pin 8-bit parallel bus transmitter using incremental signaling in 0.18um CMOS," 2002.

34. Rajeevan Mahadevan, "Front-end circuit for full-duplex transmission over coaxial cable", 1999.

35. Steve Hranilovic, "Modulation and contrained coding techniques for wireless infrared communications channels", 1999.
Jointly supervised with F. Kschischang.

36. Cameron Lacy, "Design of a programmable switched-capacitor analog FIR filter", 1999.

37. Kasra Ardalan, "Fractional-N clock synthesis", 1998.

38. Jasmine Cheng, "Adaptive equalization system for data transmission over coaxial cables", 1998.

39. Rod Zavari, "A high-speed CMOS A/D converter employing variable nonuniform quantization", 1998.

40. Kapil Kamra, "Cable equalization using adaptive analog filters", 1996.

41. John Sandhu, "Digitally control of switch mode power supplies using delta-sigma modulation", 1996.

42. Salvatore Crapanzano, "A 2V fully-differential switched-capacitor integrator technique in standard CMOS," 1995.

43. Khiem Nguyen, "Delta-sigma signal processing: Applications and implementations," 1995. Jointly supervised with Prof. D.M. Lewis.

44. Lysander Lim, "Design and implementation of time-interleaved delta-sigma A/D converters," 1994.

45. Tony Poon, "Implementation of a pipelined delta-sigma filter," 1994. Jointly supervised with Prof. D.M. Lewis.

46. Bryn Owen, "The design of delta-sigma modulator based IIR filters," 1993.

47. Dennis Au, "An integrated delta-sigma based IIR filter," 1993. Jointly supervised with Prof. D.M. Lewis.

48. Khoman Phang, "Adaptive microphone arrays using FIR and IIR filters", 1992.

49. Jane Xin, "A high-resolution digital-to-analog converter for tuning applications", 1992.
Jointly supervised with Prof. A.S. Sedra.

50. Karen A. Kozma, "Tuning integrated continuous-time filters using an adaptive technique", 1990.
Jointly supervised with Prof. A.S. Sedra.

51. Ayal Shoval, "Median-based offset cancellation circuits for integrated analog circuits", 1991.
Jointly supervised with Prof. W.M. Snelgrove.

52. Xerxes F. Wania, "Programmable multiplexed switched-capacitor filters", 1990.
Jointly supervised with Prof. A.S. Sedra.

Research Grants

NSERC - Discovery Grant - $28,000/yr 2017-2022
Digital assistance for nanoscale analog circuits

NSERC - Discovery Grant - $22,000/yr 2016
Long-Range Low-Energy Systems for the Internet of Things

NSERC - CRD with Thales - $53,000/yr 2014-2015
Next generation train localization system
(held with T. Barfoot)

NSERC - Discovery Grant - $50,000/yr 2010-2015
Advanced interface circuits for MEMS

NSERC - CRD with Gennum - $50,167/yr 2007-2009
Alternative architectures for 200MS/s data converters

BOSCH Corp - $30,000/yr 2005-2010
Scalable low power data converters

NSERC - Discovery Grant - $43,000/yr 2005-2010
Advanced oversampling converters in nanometer technologies

MICRONET - $24,000/yr 2004-2005
High speed communication circuits

NSERC - Discovery Grant - $39,000/yr 2001-2005
Programmable delta-sigma signal processing

Communications and Information Technology Ontario (CITO) - $30,000/yr 2001-2002
High speed free space optical communication

MICRONET - $35,000/yr 2001-2003
High speed communication circuits

Semiconductor Research Corp (SRC) - $64,534/yr 2000-2002
Integrated circuit and systems sciences

MICRONET - $136,000/yr 1998-2000
High speed digital communication

(held with K. Martin)

NSERC Discovery Grant - $21,000/yr 1997-2001
High speed digital comm over wireless channels

NSERC Equipment Grant - $90,330/yr 1997
Server for compute and data intensive research
(with 7 other professors)

MICRONET - $160,000/yr 1997
High speed digital communication
(held with K. Martin)

MICRONET - $100,000/yr 1995-1997
High speed data communication
(held with A. Sedra)

Information Technology Research Centre (ITRC) - $100,000,000/yr 1995-1997
Rapid analogue and mixed system design
(held with K. Martin, and G. Gulak)

MICRONET - $72,250,000/yr 1994
High speed analog circuits
(held with A. Sedra)

NSERC Discovery Grant - $13,000/yr 1993-1997
Signal processing integrated circuits

ITRC - $100,000,000/yr 1993-1995
Rapid analogue and mixed system design
(held with K. Martin, A. Sedra and G. Gulak)

ITRC - $85,000,000/yr 1991-1993
Algorithms and hardware for digital audio
(held with M. Snelgrove, P. Chow and A. Sedra)

NSERC Discovery Grant - $13,285/yr 1990-1993
Analog adaptive recursive filtering

MICRONET - $80,000,000/yr 1990-1994
Programmable and current-mode filters
(held with A. Sedra and E. El-Masry)

ITRC - $80,000,000/yr 1989-1991

Integrated filter and equalizer design
(held with A. Sedra and M. Snelgrove)

Admin Duties

- Eng. Sci. option chair for Elec/Comp Eng. 2012-2014
- Electronics Group Chairman 2003-2006
- Admissions committee representative for Elec. and Comp. Engineering 2003-2006
- Eng. Sci. option chair for Elec. Eng. 1997-2002
- Director of Elec. Eng. 1997-199
- First-year admission director for Elec. Eng. 1997-199
- Electronics Group Chairman 1996-1999
- Electronics Group Graduate Coordinator 1996-1999
- Member of various committees such as undergrad curriculum, search committees, advisory committees, etc.

Professional Activities

- Member of technical program committee 2017
  MWSCAS, Boston
- Member of technical program committee 2006
  ESSCIRC, Switzerland
- **One of three keynote speakers at NORCHIP held in Oslo, Norway** 2006
- Elected member of Advisory Committee 2001-2004
  IEEE Solid-State Circuits Society
- Elected member of Advisory Committee 2005-2008
  IEEE Solid-State Circuits Society
- Member of Technical program committee 2001-2005
  ISSCC
- **Guest editor for December 2002 issue** 2002
  IEEE Journal of Solid-State Circuits (Special ISSCC issue)
- Moderator for evening panel session 2001
  IEEE ISSCC (won best panel award)
- **Associate Editor** 1995-1997
  IEEE Trans. on Circuits and Systems
  Part I: Fundamental Theory and Applications
- **Associate Editor** 1993-1995
  IEEE Trans. on Circuits and Systems
  Part II: Analog and Digital Signal Processing
- Member of Technical program committee 1995
  ISCAS, Seattle
- Member of Technical program committee 1993
  ISCAS, Chicago
- Member of the Analog Signal Processing Committee 1994-2000
- Session Chairman 1992

Canadian Conference on Elec and Comp Engineering

Industrial Short Courses

- 12 hour short course (Mixed-Signal IC Design) 2019
  MEAD, Limerick, Ireland
- 6 hour short course (Oversampling Data Converters) 2018, 2019
  MEAD, Lausanne, Switzerland
- 6 hour short course (Low Power Circuit Design) 2018, 2019
  MEAD, Santa Cruz, CA
- 5 Day short course (Analog Circuit Design) 2003
  Qualcomm, San Diego
- 3 hour lecture (Analog Filters) 1999
  MEAD, Lausanne, Switzerland
- 1.5 hour lecture (Passband HDSL and ADSL) 1998
  ISSCC, San Francisco, CA (short course with 350 participants)
- 6 hour lecture (Digital Communications) 1996
  MEAD, Monterey, CA (40 participants)
- 3 day short course (Digital Communications) 1997
  Lucent, PA (formerly Bell Labs) (repeated in 1998)
- 3 day short course (Analog Integrated Circuits) 1998
  Lucent, PA (formerly Bell Labs)
- 3 day short course (Analog Integrated Circuits) 1997
  Cadence, North Carolina
- 1 day short course (Digital Communications) 1995
  MEAD Austin, TX (repeated in 1996 and 1997)
- 3 hour lecture (Analog Circuit Design) 1997
  Portland, OR (100 participants)
  (other lecturers included E. Vittoz, B. Gilbers, G. Temes, P. Brokaw)
- 3 graduate level courses while on research leave 1995
  Brooktree Corp, San Diego, CA
  (Signal Processing, Analog Circuits, Digital Communications)
- 3 day short course (Analog Circuits) 1994
  IBM, Vermont

Addendum

Comments on Selected Publications

- Textbook [2]**(Citations:4242)** has sold over 40,000 copies for the first edition published in 1997. A second-edition was published in 2011. At one time, it was the leading textbook for senior and graduate level courses in the area of analog circuit design. This textbook is used mostly at the graduate level although some schools are adopting it for 4'th year courses. It also has a large number of sales to working engineers who are upgrading their knowledge. Some of the adopting Universities were/are: Alfred U Main Campus, Auburn University, Brigham Young University, Carnegie Mellon University, Columbia University, Cornell University, Iowa State University, New Jersey Institute of Technology,

North Carolina State University, Northern Arizona University, Northern Illinois University, Ohio State University, Oklahoma State University, Oregon State University, Penn State University, Purdue University, Rochester Institute of Technology, Rochester St. Jr. College, Simmons College, Southern Methodist University, Tufts University, University of Arkansas - Fayetteville, University of California - Irvine, University of Colorado - Denver, University of Colorado - Boulder, University of Colorado - Colorado Springs, University of Illinois - Champaign, University of Maryland, University of Miami, University of Michigan, University of Minnesota, University of New Hampshire, University of New Mexico, University of Texas - Austin, University of Texas - Arlington, University of Washington, University of California - La Jolla, Stanford University.

- [34]**(Citations:122)** is a tutorial paper that is a result of a sabbatical leave in California with Brooktree Corp. The co-author, D. Essig, is a Brooktree fellow. Although tutorial in nature, the paper describes state-of- the-art techniques for realizing high-speed digital communications over wired channels. It has been well received and resulted in Prof. Johns being invited to ISSCC, 1998 to give a tutorial talk on passband schemes for HDSL and ADSL.
- [36]**(Citations:14)** presents a method for realizing a 100Mb/s pulse-shaping transmit filter in a 0.8um BiCMOS process. The filter is automatically tuned and experimental results are included. At the time of this publication, this work demonstrated the fastest integrated analog adaptive filter. The student involved with this work (Ayal Shoval) joined Lucent where he applied these concepts to a 100Mb/s Fast Ethernet transceiver. This chip sold at high volume and showed considerable performance advantages over other existing integrated ethernet transceivers.
- [38]**(Citations:89)** presents an extensive analysis into the dc offset effects of four variants of the LMS algorithm as applied to adaptive analog filters. This work was part of Ayal Shoval's Ph.D. study where Dr. Johns was the primary supervisor in this part of his work. This paper has numerous citations as it has helped researchers understand dc offset effects in various LMS algorithms.
- [40]**(Citations:108)** made use of the oversampling techniques in [43] **(Citations:106)** to present a method for realizing a high quality analog sinusoidal signal using only 4 digital adders together with some minor logic, a 1- bit D/A converter and a low-pass filter. This work was jointly performed with Prof. Roberts at McGill University. Experimental results were performed at UofT. This work grew out of [43] which described an approach for performing IIR filtering directly on oversampled modulated signals without the use of multibit multipliers. This technique saves considerable amounts of hardware where multiple analog inputs (or outputs) are needed compared to processing at the Nyquist-rate

through the use of decimation and/or interpolation filters. It also reduces the amount of latency and thus has a significant advantage for use in systems with feedback such as control loops. This work was jointly developed with Prof. Lewis who contributed mostly on the digital hardware aspects with Dr. Johns contributing mostly on the signal-processing aspects. Industry and academics are have shown a considerable amount of interest in this work.

- [47] **(Citations:55)** described a tuning approach for continuous-time integrated filters based on adaptive filter theory. This approach is the first method that can tune both the poles and zeros of a transfer function. This work was part of Karen Kozma's M.A.Sc. thesis where Dr. Johns was the primary supervisor. This work is strongly based on Dr. Johns' Ph.D. results on continuous-time adaptive filters. This paper is included in an IEEE Press Book entitled "Integrated Continuous-Time Filters".
- [51] **(Citations:87)** introduced a new filter structure for continuous-time filters referred to as "orthonormal ladder filters". This structure is particularly well suited for programmable applications (such as adaptive filtering) as it is unique for a given transfer-function (within scaling factors of -1), inherently scaled for optimum dynamic range, has a simple stability check and a performance comparable to an optimum cascade-of-biquads. This work was part of Dr. Johns' Ph.D. thesis. A firm in Pickering, Ont. (Adamson Acoustics) made use of these orthonormal filters for their audio equalizers while PhD graduate students at CMU have made use of this structure for their research into analog equalization.