A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling

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***Abstract*—A sigma–delta digital/analog converter implemented in 0.6-μ CMOS uses a 6-bit modulator together with a segmented noise-shaped scrambling scheme to achieve 113-dB A-weighted dynamic range over a 20-kHz bandwidth. A continuous-time output stage is used to achieve high signal-to-noise ratio in a 9.1-mm^2 die area. The output stage uses a dual return-to-zero circuit that eliminates errors caused by intersymbol interference.**

***Index Terms*—Digital–analog conversion, sigma–delta modulation.**

I. Introduction

NEW CONSUMER formats such as digital video disc are pushing the performance of audio digital/analog (D/A) converters to higher and higher levels. D/A converters (DAC's) with very high dynamic range and very low cost are now in demand.

Previous sigma–delta D/A converters shown in Fig. 1 have used 1-bit digital modulators with switched-capacitor analog filters. The noise of switched-capacitor filters is limited by thermal kT/C noise, and thus, achieving very high dynamic range requires an impractical amount of on-chip capacitance. For example, consider the design of a sigma–delta audio D/A converter with a simple first-order switched-capacitor output filter operating at an oversampling ratio of 128 (about a 6-MHz clock rate) and a signal-to-noise ratio (SNR) of 120 dB. A simple calculation of kT/C noise shows that the value of input and feedback capacitance of the output filter must be at least 100 pF. In addition, to achieve a 100-kHz cutoff frequency would require 1 nF of capacitance for the integrating capacitor, which results in a total capacitance of 1.2 nF. Typically, second- or third-order switched-capacitor filters are used; hence, the actual amount of on-chip capacitance may be higher.

The kT/C noise of switched-capacitor filters may be avoided by using a continuous-time output stage [3], as shown in Fig. 2. Several examples of continuous-time output stages are shown in Fig. 3. In Fig. 3(a), the 1-bit digital data from the modulator are applied to a CMOS inverter powered from "clean" analog supplies. The inverter output is then fed to a filter consisting of a passive pole followed by an active filter. Only a single-pole active filter is shown, but there are many variations that can be used to achieve high-order analog filtering in a single op-amp stage. The purpose of the passive pole is to prevent the op-amp from seeing full-scale steps at the modulator clock rate. These steps, if unfiltered, may cause foldovers of noise and tones due to the nonlinear settling behavior of an op-amp when presented with a fast transient. Unlike many switched-capacitor circuits where only the settled value is important, the dynamic behavior of a DAC output stage must be linear at all times.

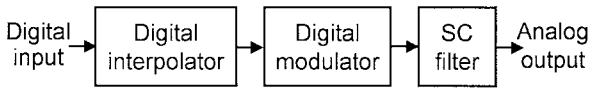

Fig. 1. Conventional SC sigma–delta DAC.

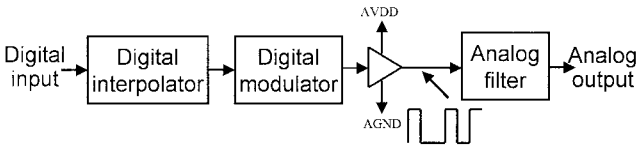

Fig. 2. Sigma–delta DAC with continuous-time output stage.

The simple inverter output stage suffers from many potential problems. Any noise on the positive analog supply (VDD) will couple into the output, and since the gain of this circuit is proportional to VDD, high-frequency supply noise can mix with the high-frequency sigma–delta spectral components to cause in-band tones and excess noise. Another problem with this simple output stage is sensitivity to clock jitter. If the clock edges are contaminated by random jitter, then the area under each output voltage pulse will be incorrect. This random error in the pulse area causes noise to appear in the baseband spectrum. Fig. 4 shows the results of a simulation carried out to determine the sensitivity to clock jitter. A conventional second-order loop was coded in software and its output passed through a software infinite impulse response low-pass filter. To simulate the effect of jitter, a random Gaussian number was generated with an rms amplitude equal to the desired clock jitter. For each clock cycle, the error in the pulse area due to clock jitter is computed by altering the amplitude of the 1-bit signal rather than changing the edge timing. The amplitude alteration only takes place on those clock cycles where a transition from 0 to 1 or 1 to 0 occurs, as clock jitter can only affect the pulse area when the 1-bit signal changes. This simplification allows a conventional difference-equation simulation to be carried out at the modulator clock rate rather than trying to slice time into 1-ps increments, which would result in extremely lengthy simulation times. This approach results in an accurate estimate of the baseband noise contamination.

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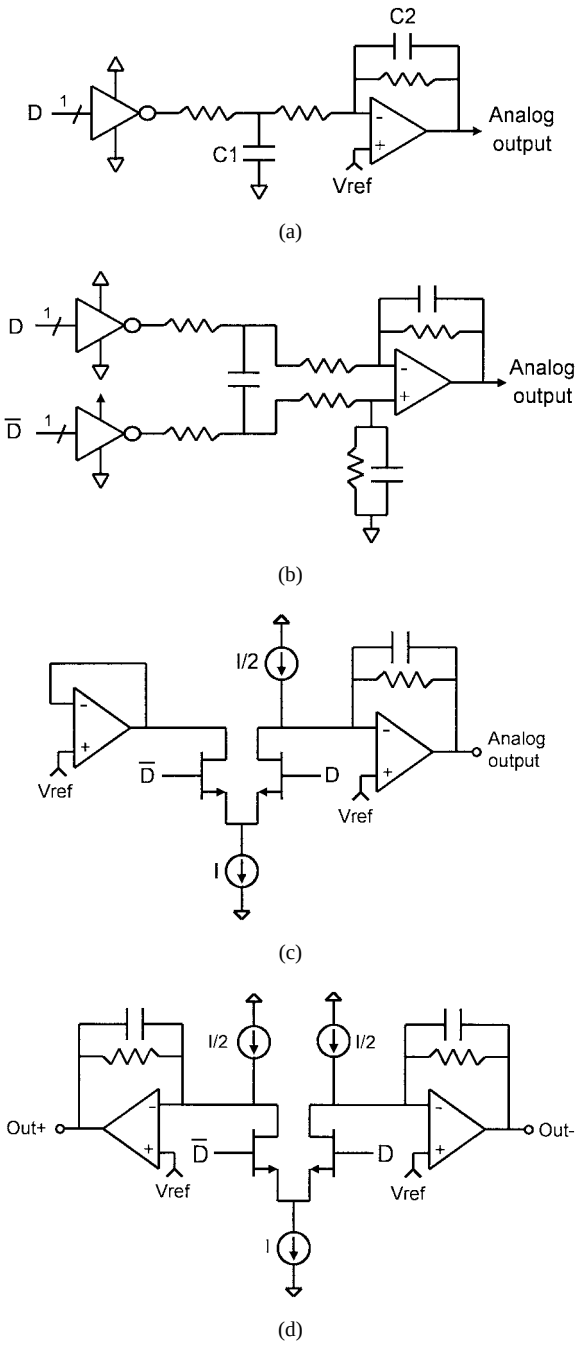

Fig. 3. Options for 1-bit DAC. (a) Voltage-out inverter with passive and active filter. (b) Differential voltage-out inverter with passive and active filter. (c) Current-output 1-bit DAC. (d) Differential current-output 1-bit DAC.

The graph shows that there are two components to the output noise: one due to clock jitter and one due to the filtered quantization noise. For the 128x-oversampled system shown, the 1-bit quantization noise is 95 dB below the peak signal, assuming the peak signal completely uses up the available range of the converter. The noise due to clock jitter is linear with the amplitude of the jitter. For low values of jitter where the noise is dominated by quantization noise, we have extrapolated the jitter-noise line below that of the quantization noise so that we can estimate the jitter requirements for higher performance, higher order designs. The graph shows that 10-

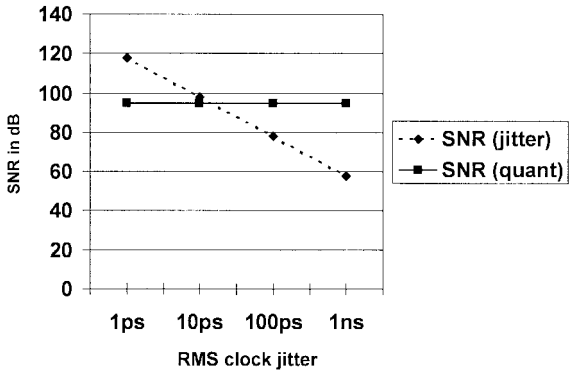

Fig. 4. Jitter sensitivity from simulation for a second-order 1-bit 128x oversampling delta–sigma modulator with white Gaussian clock jitter.

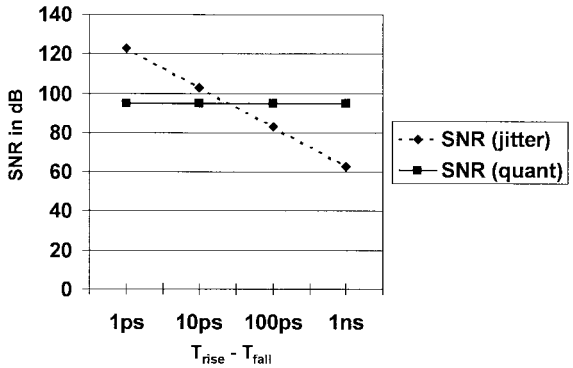

Fig. 5. Sensitivity to mismatch in rise and fall time of the 1-bit signal from simulation of a second-order 1-bit 128x oversampling delta–sigma modulator.

ps rms white Gaussian jitter will limit the performance of a 128x-oversampled 1-bit design to 98 dB.

It is possible to design crystal oscillators that meet this jitter specification. However, a commercial D/A converter intended for inexpensive consumer-electronics equipment must be able to tolerate clock jitter as high as 100-ps rms. Often the clock source is not a crystal oscillator but rather an inexpensive phase-locked loop used in a clock-recovery circuit. This sensitivity to clock jitter thus presents a serious problem to the chip designer and is the primary reason why switched-capacitor designs have been used in the majority of successful commercial D/A designs.

Another problem with 1-bit continuous-time outputs is the sensitivity to the difference in rise and fall time of the 1-bit signal. If the rise and fall times of the 1-bit signal are matched, then the area error under a sequence of bits does not depend on the order of the bits. However, if the rise and fall times are mismatched, the area under a sequence of bits does depend on the order of the bits. This nonlinearity causes noise and tones in the high-frequency region of the 1-bit spectrum to fold into the baseband. Fig. 5 shows the results of a simulation carried out to determine the sensitivity to this mechanism. The simulation is done in the same way as the previous simulation for jitter sensitivity, where the amplitude of each output bit is adjusted to give the same area as a real pulse that is contaminated by finite rise/fall times. The results are very similar to the case for jitter; a mismatch of 10 ps in the rise and fall times of the

1-bit waveform limits the performance of a 128x-oversampled design to 103 dB.

Differential structures may be used to obtain some relief from the rise/fall-time matching requirement. Fig. 3(b) shows a differential structure with two inverters fed from out-of-phase data signals. These two inverters feed a differential passive filter, followed by a differential-to-single-ended stage with additional filtering. In this scheme, as long as the rise times of the two inverters are the same, and the fall times of the two inverters are also the same, then cancellation of the rise/fall errors will occur. Thus, it is only important that the two inverters match each other rather than relying on the matching between an NMOS and a PMOS device. The jitter sensitivity is unfortunately not improved by using a differential circuit, and the sensitivity to noise on the VDD supply line is still a problem.

Fig. 3(c) shows a single-ended current-switching scheme where a CMOS differential pair is used to steer currents into an I–V converter. This circuit still suffers from rise/fall matching and jitter errors, but it offers improved rejection of supply noise, as the gain is only affected by the magnitude of the current source and not the magnitude of the VDD supply. Another advantage is that the input-referred noise voltage of the op-amp appears at the output with a gain of one, assuming the current-source output impedance is much larger than the value of the feedback resistor. The circuits shown in Fig. 3(a) and (b) both have at least 6 dB of noise gain and thus require a lower noise op-amp to achieve the same SNR.

Fig. 3(d) shows a differential current-steering output circuit that offers some rejection of the rise/fall mismatch noise. The degree of rise/fall error reduction depends on the symmetry of the gate drive signals applied to the differential pair. The gate drive signals should ideally cross at the midpoint in order to minimize the "glitch" seen on the drain of the current-source device.

None of the circuits above can solve the most serious problem: the extreme sensitivity to clock jitter. This jitter sensitivity is caused by the large steps in the 1-bit waveform, which converts a timing error into an area error. Thus, the only way to reduce jitter sensitivity is to reduce the size of the steps in the output waveform. This can be accomplished by replacing the 1-bit quantizer in the sigma–delta loop with a multibit quantizer.

Fig. 6 shows waveforms for both a 1-bit sigma–delta converter and a multibit converter. Clearly, the step sizes in the multibit case are far lower than in the 1-bit case, and thus the jitter sensitivity is reduced proportionally. Fig. 7 shows the simulation results for the multibit case where a 6-bit (64-level) quantizer is used. The jitter sensitivity is now vastly improved; 100-ps rms of white Gaussian clock jitter degrades the SNR to 109 dB. Many clock-recovery circuits used in consumer-electronics equipment have a combination of random jitter and low-frequency jitter due to $1/f$ noise. Sigma–delta continuous-time outputs are primarily sensitive to the random portion of the jitter and not the $1/f$ portion of the jitter. In most consumer equipment, the random jitter component is less than 100 ps. Therefore, it was decided that a 6-bit quantizer was required to meet the target specification of 112 dB with typical clock jitter.

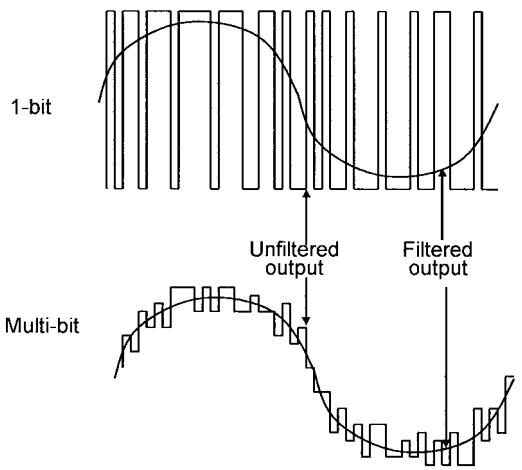

Fig. 6. One-bit and multibit waveforms.

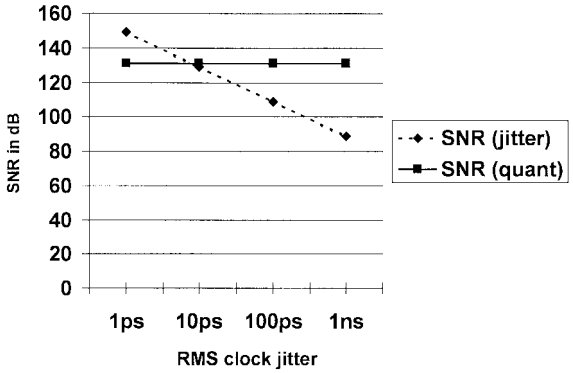

Fig. 7. Jitter sensitivity from simulation for a second-order 6-bit 128x oversampling delta–sigma modulator with white Gaussian clock jitter.

Using a multibit modulator introduces another problem, namely, distortion caused by element mismatch. In previous works [1], [2], the authors disclosed a method for dynamically reassigning the connection between thermometer-decoded modulator bits and analog elements in such a way as to turn the mismatch errors into shaped noise. This approach used a network of interconnected "swapper" circuits where each swapper cell is controlled by the data itself. This technique could not be used in the present design due to the large number of modulator levels (64), which would cause an increase in chip area and power consumption. To circumvent this problem, a new technique called segmented scrambling is used, where the 6-bit word is split into two smaller subwords that are each individually noise shaped. These two smaller words are then individually scrambled using the noise-shaped scrambling technique in [1] and applied to two separate DAC's.

The problem of nonlinear intersymbol interference is solved by using another new technique called "dual return-to-zero." These new techniques will be described in more detail in the next sections.

II. Chip Architecture

Fig. 8 shows the overview of the design. The input is presented through a serial port to a digital interpolation filter

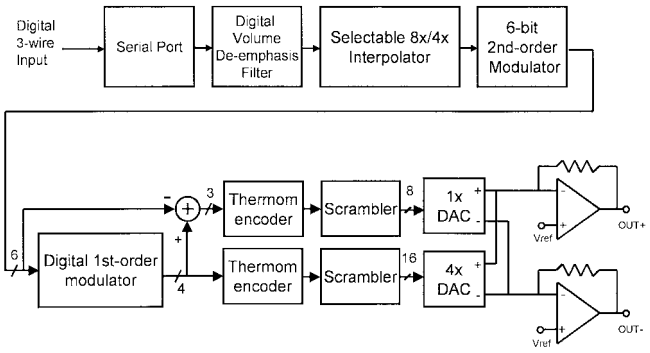

Fig. 8. Chip implementation.

with an interpolation ratio of 4 or 8x, depending on the input sample rate. This signal is then upsampled by a factor of 16 to the modulator rate using a zero-order-hold register. The interpolated data are then passed to a second-order digital modulator with 6-bit quantization. The modulator is of conventional design, with a theoretical SNR of 125 dB. The use of a 6-bit modulator reduces the output step size compared to a 1-bit system by a factor of 64, which dramatically lowers the sensitivity to jitter and presents an output waveform that resembles a sine wave without any filtering, as shown in Fig. 6.

The 6-bit modulator output is then split into two subwords, one of length 4 bits and the other of length 3 bits, using a noise-shaped splitter circuit, described in more detail later. The weighted sum of these two subwords (4*B + C) equals the original 6-bit modulator output word A.

Each subword is then applied to a thermometer decoder circuit. The 4-bit signal B is decoded into 16 equally weighted lines, and the 3-bit signal C is decoded into 8 equally weighted lines. The thermometer-decoded outputs are then applied to two data-directed scrambler circuits that are identical to those used in a previous design presented in [1]. The scrambler preserves the number of lines that are at a logic "1," and therefore, the digital sum is not changed by the scrambling operation. The outputs of the two scrambler circuits are then applied to two current-steering DAC's with weights of 4 : 1 relative to each other. Each of these DAC's uses a dual return-to-zero architecture to be described later. The DAC outputs are differentially summed in current mode into two active I–V converters, yielding a differential voltage output.

A. Segmented Scrambling

To meet the desired 112-dB design goal with 100 ps of clock jitter, a 6-bit modulator was required. Unfortunately, the scrambler design presented in (1) could not be easily extended to the 6-bit case without growing the digital complexity and area to unacceptable levels.

Fig. 9 shows a normal segmentation circuit where the 6-bit word is split into the upper 3 bits and lower 3 bits, with each subword then individually thermometer decoded and scrambled. The spectra for the original 6-bit word and the two subwords are shown in the figure. Clearly, while the original modulator output A contains shaped noise, the two subwords will each contain nonshaped noise as well as distortion. These components cancel if the two words are added together with

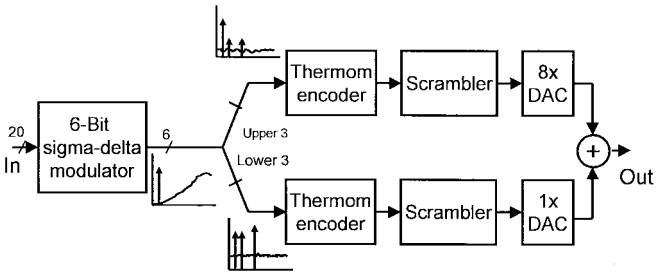

Fig. 9. Segmentation.

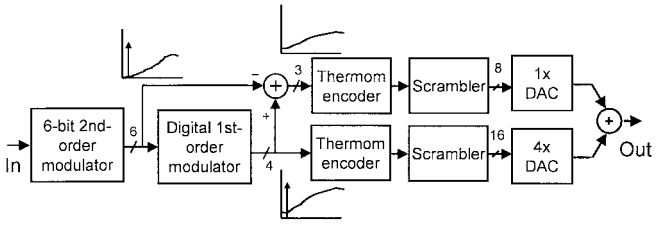

Fig. 10. Noise-shaped segmentation.

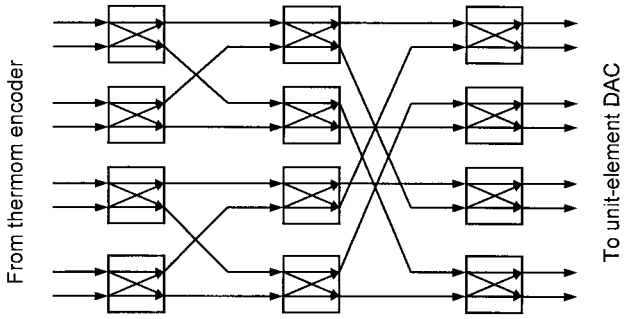

Fig. 11. A 3-bit example of the noise-shaped scrambler.

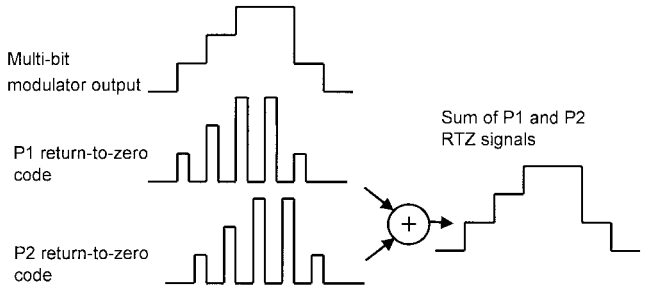

Fig. 12. Dual return to zero.

a gain ratio that is exactly 8 : 1, but in the presence of a gain error between the two DAC's, the spectra from each individual subword will "leak" into the output spectrum and cause degraded performance.

Fig. 10 shows the new noise-shaped segmented scrambling technique. A second-order digital modulator with a 6-bit output is applied to a simple first-order digital modulator of conventional design that reduces the 6-bit word length to 4 bits. This 4-bit signal B is subtracted from the original 6-bit signal A (with most significant bits aligned) to produce a 3-bit signal C. Since signal C is the difference between the input and output of a noise shaper, it represents only the shaped quantization noise of the first-order digital modulator and does not contain any signal components. The signal B is

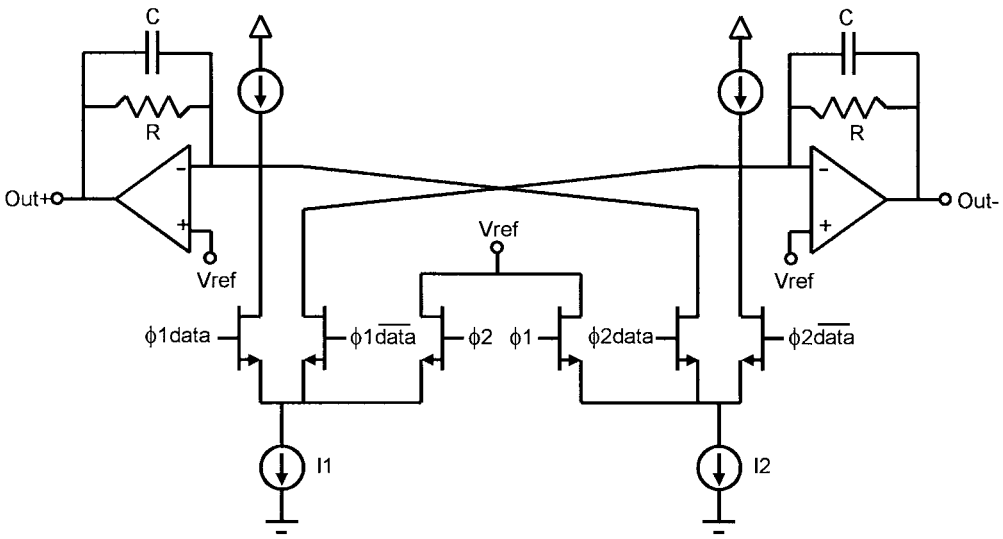

Fig. 13. A dual-RTZ bit-cell circuit.

then thermometer encoded and applied through a noise-shaped scrambler to a 16-level DAC with weight 4x, and signal C is likewise applied to an 8-level DAC with weight 1x. The sum of B and C must equal the original signal A, as the signal C was derived by subtracting B from A. Since each of the signals B and C passes through a noise-shaped scrambler circuit, any errors within each DAC result in shaped noise.

Now consider the case where the gain of DAC B does not match the gain of DAC C. Since signal C contains only shaped noise, the result of a gain mismatch must also be a noise-shaped signal that contributes little energy to the in-band spectrum. Thus the "spectral leakage" problem encountered earlier only causes out-of-band noise. Simulations show that gain errors of up to 1% may be tolerated while still achieving 110-dB SNR.

It is possible to design splitter circuits that use higher order shaping than the first-order noise shape used here. However, one problem with using higher order shaping is that the maximum difference between input and output of a higher order noise shaper is not bounded by ± 1 least significant bit of the loop quantizer, as it is in the first-order case. This causes the word width of signal C to grow and hence increases in the number of elements needed in the design of the 1x DAC.

Fig. 11 shows a 3-bit example of the scrambler described in [1]. The scrambler consists of a number of "swapper" cells, each with two inputs and two outputs. On each clock cycle, the swapper cell may either pass the two inputs unchanged to the two outputs or reverse the order of the input bits at the output. A control circuit will decide whether or not to "swap" the inputs on any given modulator clock cycle. This control logic circuit is designed to distribute the input bits as evenly as possible to the two output nodes. One bit of "state" is used to remember which output node has received the largest number of "1's." The output that is "behind" in its allotment of "1's" will receive the next "1" when the input pattern is a "0 1" or "1 0." It has been shown that each swapper output represents the "average" of the two inputs plus a first-order high-pass filtered mismatch error term [4]. By connecting the swapper cells in a fast Fourier transform (FFT)-like butterfly arrangement [5], the mismatch error between the unit elements of the entire DAC system will become first-order high-passed [4]. Thus, analog weight errors between the DAC elements will cause first-order highpass-shaped noise to appear at the output. This noise is largely above the audio band and therefore does not contribute significantly to the in-band noise.

The combination of noise-shaped segmentation and noise-shaped scrambling achieves a dramatic decrease in the sensitivity to analog weight mismatch errors. Random errors across the entire current-source array of up to 1% may be tolerated while still achieving 110 dB of SNR.

B. Dual Return-to-Zero Switching Scheme

It is well known that the intersymbol interference problem can be solved by using a return-to-zero (RTZ) code, where each bit cell is turned off during half of the clock period. However, this approach introduces large steps in the DAC output voltage, which again causes problems with jitter sensitivity and linearity in the output stage.

To overcome this problem, a new dual RTZ scheme shown in Fig. 12 is used. In this scheme, two independent return-to-zero signals are generated, with a time offset of 1/2 clock period. These signals are then linearly added together to form an output signal that is continuous over the full clock period. The theory of superposition may be used to state that if each RTZ signal is spectrally pure due to the absence of any intersymbol interference, then the linear sum of two RTZ signals must also be spectrally pure. This can also be explained in the time domain by noting that if the fall of the phase-1 RTZ signal does not match the rise of the phase-2 RTZ signal, the small "glitch" will occur in the summed output. This glitch contains just the right amount of area to cancel the error caused by intersymbol interference. Note that the falling edge of the phase-1 RTZ waveform is controlled by the same clock edge as the rising edge of the phase-2 RTZ waveform. If this edge of the clock is corrupted by jitter, there is little effect on the summed waveform, as both edges of the two RTZ waveforms move together. On the other hand, if the rising edge of phase-1

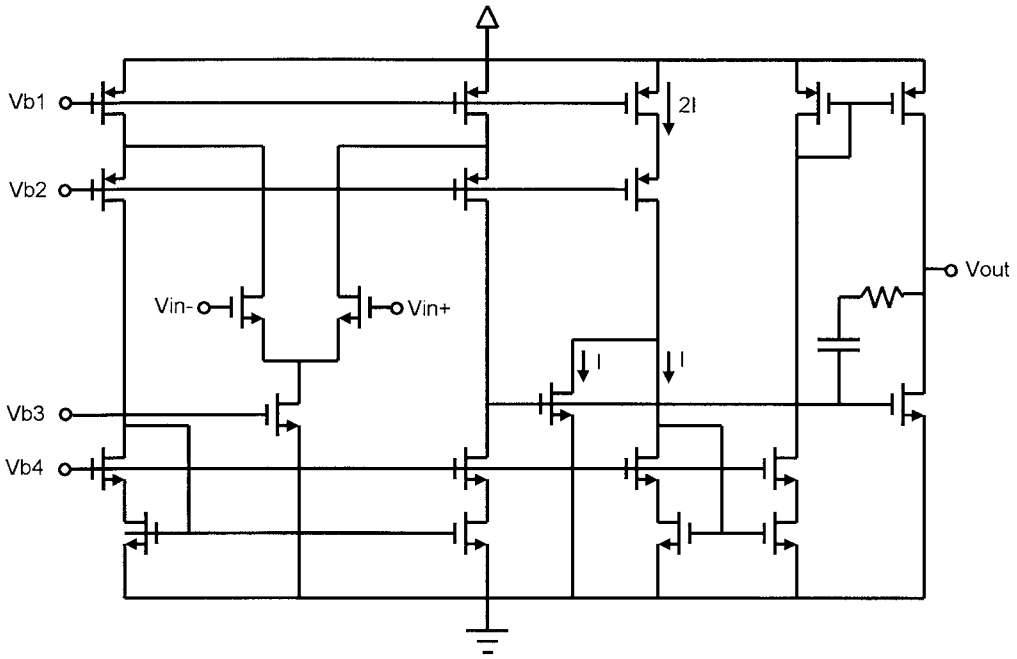

Fig. 14. Low-distortion op-amp.

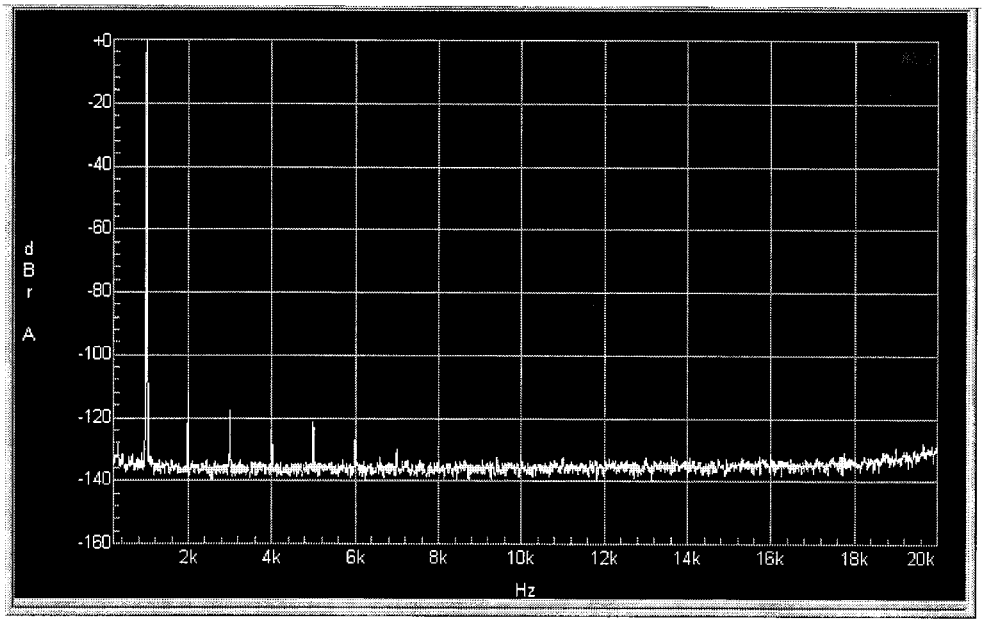

Fig. 15. 8-K FFT with full-scale 1-kHz input.

or falling edge of phase-2 RTZ is corrupted by jitter, it will result in in-band noise as the area under the current pulse is no longer constant.

The schematic diagram of a dual-RTZ DAC cell is shown in Fig. 13. The cell consists of two identical subcells I1 and I2 of equal magnitude. On phase 1, current cell I1 is steered to either op-amp A or op-amp B by a simple current-steering differential pair, depending on the input bit. At the end of phase 1, the current cell I1 is diverted to a throwaway point. During phase 2, a current cell I2 is steered to the same op-amp as was used in phase 1. At the end of phase 2, it is steered to a throwaway point. Since the same current is delivered on

TABLE I
MEASURED PERFORMANCE

SNR, 20-20kHz, un-weighted	111dB
SNR, 20-20kHz, A-weighted	113dB
D-range, -60dBFS, A-weighted	113dB
THD+N, 0dBFS	<-100dB
Digital filter frequency response	+/-0.04dB, DC-20kHz
Power consumption	250mW
PSRR @ 1kHz	60dB
Channel separation	100+dB

□

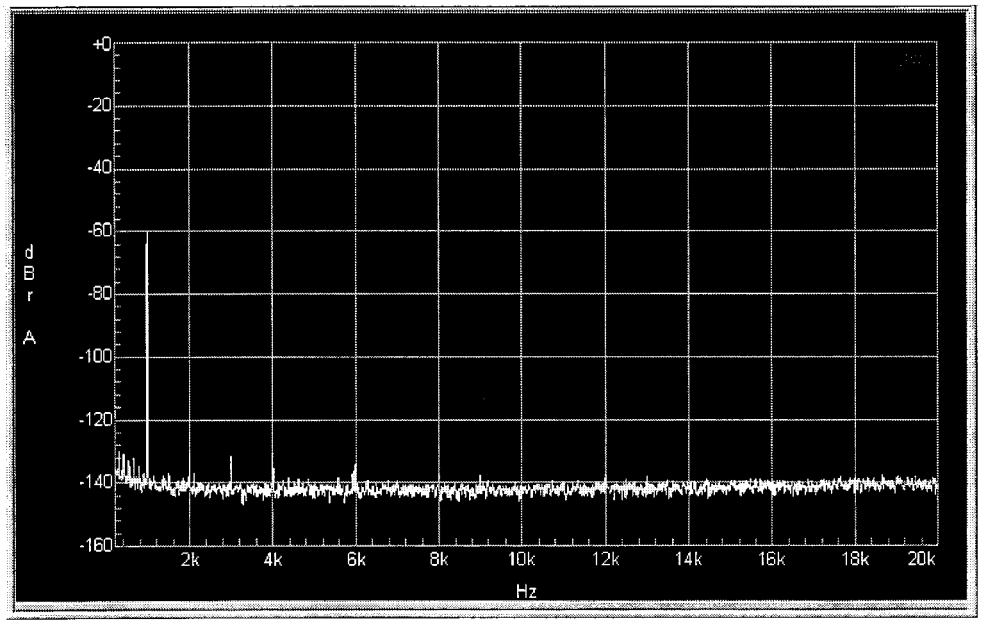

Fig. 16. 8-K FFT with −60 dBFS input.

both phases of the clock, the total current is approximately constant over the clock period.

The outputs of the dual RTZ current switches are fed to two single-ended I–V converters each using a 1.9-K feedback resistor. The op-amp in the I–V converter shown in Fig. 13 is designed for low noise and distortion. To enhance the resistive driving capability of the op-amp, a transconductance stabilizing circuit is added. The output stage senses the current in the NMOS output driver and subtracts this current from a reference current. The difference is then mirrored to the PMOS output device. Thus, the output stage works in a push–pull fashion and results in significantly improved distortion performance when driving a resistive load. The op-amp was measured separately and achieved a total harmonic distortion (THD) of −108 dB with a 1-$V_{\rm rms}$ output into a 1-K load.

As mentioned earlier, in a DAC design, it is essential that the output remain linear at all times and not just settle to the correct final value. In practice, this requirement can be translated to a slew-rate requirement on the op-amp. A step in the current applied to the I–V converters initially flows through feedback capacitor C in parallel with the feedback resistor R, causing an initial slope of I/C. The slew rate of the op-amp should be greater than this value by an amount large enough to avoid significant nonlinearity during this charging phase. This value can be determined through simulation by integrating the area under a sequence of up and down steps of various heights and measuring the error of this area relative to a simulation that uses ideal op-amps. In this design, the area using real op-amps was accurate to 1 ppm. Fig. 14 shows a low-distortion op-amp.

III. Measured Results

The performance of the converter is summarized in Table I. The converter achieves a 111-dB unweighted SNR (113-dB "A-weighted") and 100+ dB in THD + N. Figs. 15 and 16 show the FFT plots of an input sine wave with 0 and −60 dBFS amplitude, respectively. The power-supply rejection ratio was measured to be 60 dB at 1 kHz, and the interchannel separation is 100+ dB at 1 kHz.

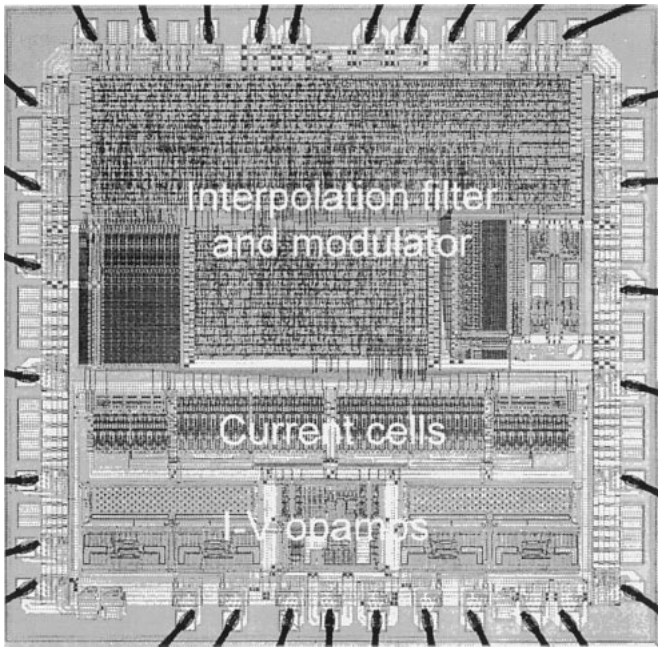

Fig. 17. Chip microphotograph.

The limiting factor in the SNR is the analog noise of the onboard op-amps and feedback resistor. A SPICE noise simulation of the biasing network and op-amp I–V converter gave a predicted SNR of 112 dB (unweighted). This means that the quantization noise of the sigma–delta modulator and the noise due to switching dynamics and intersymbol interference are far lower than the noise contributed by the op-amps and biasing network.

Fig. 17 shows a chip microphotograph. The IC was fabricated in a 0.6-μm double-poly double-metal CMOS process. The die area is 3.2 $\times$ 3.1 mm.

IV. Conclusion

Two new techniques have been proposed and successfully used to solve the problems that normally would plague continuous-time sigma–delta converters. The sensitivity to clock jitter has been reduced by using a 6-bit modulator. The element-matching problem of multibit modulators has been solved by using a noise-shaped segmentation and scrambling technique. The problem of intersymbol interference has been solved by using a dual return-to-zero circuit. Together, these techniques allow a 113-dB SNR to be achieved in a 9.1-mm^2 die area without the usual kT/C noise limitations of on-chip switched-capacitor filters.

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