16.7 A 110dB SNR and 0.5mW Current-Steering Audio DAC Implemented in 45nm CMOS

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Mobile consumer audio applications are demanding higher performance, longer battery life and lower cost. Achieving low out–of-band noise (OBN) is one of the key elements in designing inexpensive, low-power and robust audio DACs. Lowering OBN reduces the sensitivity to circuit mismatch, glitch energy and clock jitter. The need for an expensive analog post filter that requires high bias currents can be eliminated altogether. Requirements on the application clock are relaxed and low-cost PLLs can be used in the system. To reduce OBN, one needs to increase modulator resolution. The popular method is to increase the number of unit weighted elements in an oversampled DAC. This results in high digital complexity, inter-symbol-interference (ISI) and tonal problems when shaping mismatch errors. Reported multi-bit oversampling audio DACs [1, 2] use noise-shaped segmentation to split a main modulator output into binary weighted sub-DACs. This segmentation increases the resolution that can be used in the main modulator with relatively simple digital signal processing to shape mismatch errors outside the audio band.

This paper presents a cascaded-modulator architecture with parallel DACs that can be weighted arbitrarily to attain high effective resolution levels with greater flexibility. Figure 16.7.1 shows the high-level block diagram of the cascaded modulator architecture. The error signal across the primary modulator is scaled up by a factor of "*K*" and passed to the secondary modulator. The scaling down happens on the analog side by sizing secondary elements as "1/*K*th" of the primary ones. Therefore, cost of the secondary path is significantly lower for large values of *K*. For a simple 2-level cascaded system, the combined output transfer function can be written as

$$Y(z) = X(z) + \frac{1}{K} \cdot NTF(z) \cdot E_2(z)$$

If the secondary modulator has *M*-levels, then the final output will effectively have *K*•*M* level resolution at combined output. Mismatch changes the transfer function as

$$Y(z) = X(z) + \left(1 - \frac{K_d}{K_a}\right) \cdot NTF(z) \cdot E_1(z) + \frac{1}{K_a} \cdot NTF(z) \cdot E_2(z)$$

where K_d, K_a are the digital and analog coefficients, respectively. Any mismatch between the primary and secondary DACs is simply a deviation in K_a. This mismatch is shaped by the secondary noise transfer function (NTF) and has almost no impact on the in-band signal when compared to the in-band quantization noise contributed by the secondary modulator. In theory, a 1% mismatch allows to set *K* as high as 100 before starting to get limited by mismatch.

In this architecture, there is no reason that primary and secondary modulators must be identical. Each path can be optimized individually to maximize the overall resolution. The quantization noise of the primary modulator loads the secondary one which is providing finer resolution steps. Therefore, in the overall optimization scheme, one can put the emphasis on reducing the quantization noise when picking the primary modulator, and the stability when picking the secondary modulator. This method also maximizes *K*-factor which in turn increases the effective resolution. Cascading operation can be further repeated and OBN can be completely buried under the thermal noise floor. This operation is bounded with minimum device size and sensitivity to mismatch within one modulator path. An *N*-deep cascade with *K*-scaling at each level will result in K^{N-1}•*M* levels at the output. Previous noise-shaped segmentation method [1, 2] can still be applied on each modulator path depending on the quantizer levels chosen per path and mismatch shaping operation.

Digital pulse-width modulation (PWM) followed by an analog FIR (AFIR) filter has been shown to be very robust against circuit mismatch and ISI [3, 4]. PWM operation does not inject any new quantization noise into the system but creates replicas of the input spectrum into the higher frequencies centered around the carrier harmonics with additional nonlinear components as harmonic sidebands. The following AFIR DAC filters majority of this energy by aligning the notch locations to the image locations. Because filtering operation relies on the notch locations and not on the absolute value of the stop-band ripple, a slight shift in notching frequencies caused by circuit mismatch will have no impact on noise and distortion. An inexpensive analog filter can then be used to filter the remaining high-frequency contents in the spectrum. Another advantage is that the switching rate of the DAC elements is dominated by the PWM carrier frequency. Therefore, glitch energy is a function of the out-of-band carrier and is not strongly correlated to the audio signal frequency. This leads to reduced ISI-induced noise and distortion in a continuous-time current-mode DAC.

The system shown in Fig. 16.7.2 is implemented in this paper using a standard 45nm CMOS process. A 3rd-order noise-shaping transfer function is used for the modulators with two zeros placed at DC and one zero placed at Fs/2. It is important to note that while the additional zero at Fs/2 is suboptimal and does not help in reducing the out of band noise, it is useful in creating a clean notch location to implement 1/f noise cancellation in a subsequent amplifier that is planned for this circuit. Both quantizers have 33-levels. This allows *K*-factor to be as high as 10 and sets the output resolution to 330-levels. The input signal is oversampled by 64 to 3.072MHz. Each modulator output in the cascade is encoded to a 1b PWM sequence. Switching rate, when using double-sided PWM, for the DAC current sources is 3.072×33×2=202.752MHz. The 32-tap AFIR filtering is implemented in both primary and secondary current-steering DACs as shown in Fig. 16.7.3. Continuous-time current-mode DACs are perfectly suited for dense CMOS processes. They scale nicely from node to node, have very low layout overhead and can be clocked at very high speeds. The overall area of analog blocks including the primary and the secondary DACs is less than 0.04mm^2. To increase the area efficiency in the layout, secondary DAC elements are interleaved within the primary DAC.

Figure 16.7.4 shows measured OBN of the combined output and the simulated OBN of primary only and the combined outputs. Measurement and simulation results match very closely. With a very small area penalty of the secondary DAC, the cascaded architecture achieves a 20dB suppression of OBN. This level of filtering would have been extremely costly in terms of power as well as area if a standard analog filtering approach was used. As expected, audio-band FFT measurements in show a virtually distortion-free DAC operation in both large and idle channel signal swing conditions (Fig. 16.7.5). The tones seen at the DC and around the signal frequency are 60Hz and are harmonics of the board supply. The measured performance summary is shown in Fig. 16.7.6 and a die micrograph is included in Fig. 16.7.7.

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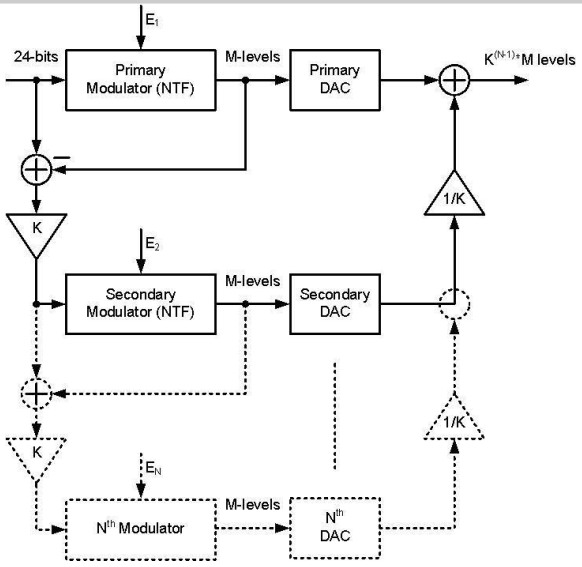

Figure 16.7.1: Cascaded modulator architecture.

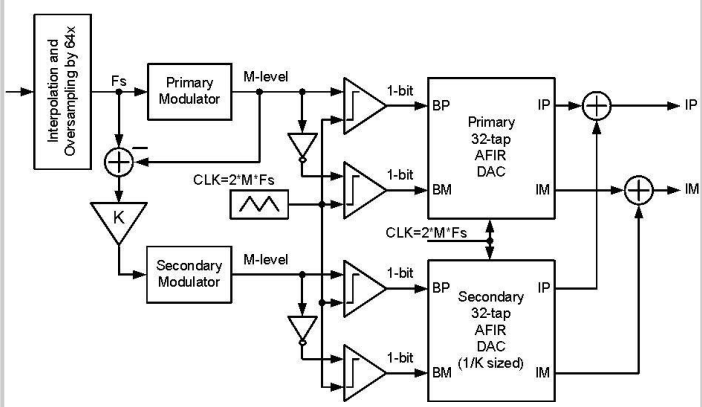

Figure 16.7.2: Implemented cascaded architecture with PWM and AFIR.

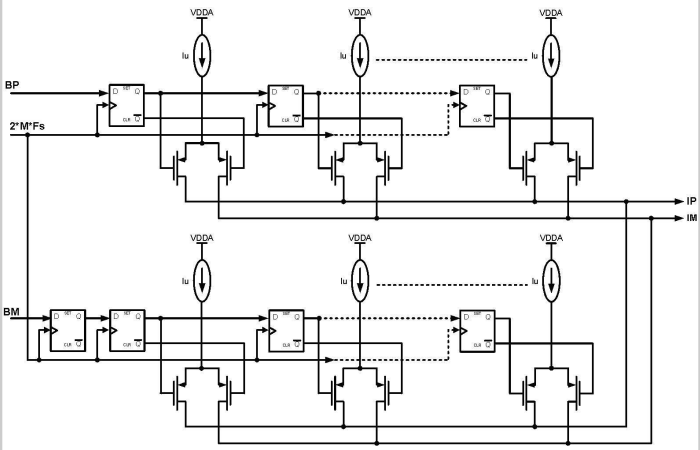

Figure 16.7.3: AFIR DAC implementation.

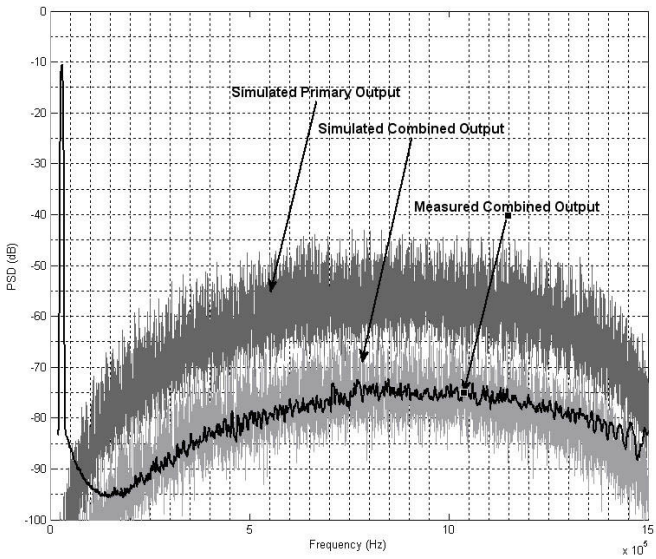

Figure 16.7.4: FFT plots for out-of-band noise.

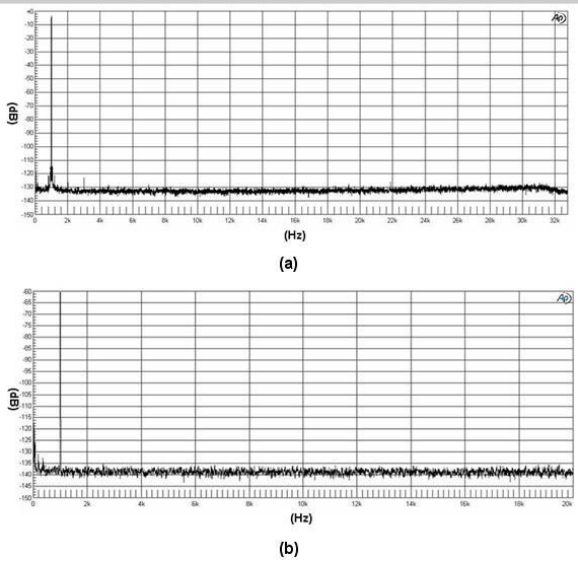

Figure 16.7.5: Measured FFT plots.

Process	45nm CMOS
Supplies	1.4V Analog 1.1V Digital
Full-scale differential output	176uA peak to peak
Digital power consumption	0.1 mW
Analog power consumption	0.4 mW
Total area	0.045mm2
OSR	64
Clock Frequency	3.072MHz and 101.376MHz
Dynamic Range (A-weighted)	110dB
THD+N	-100dB

Figure 16.7.6: Performance summary per DAC.

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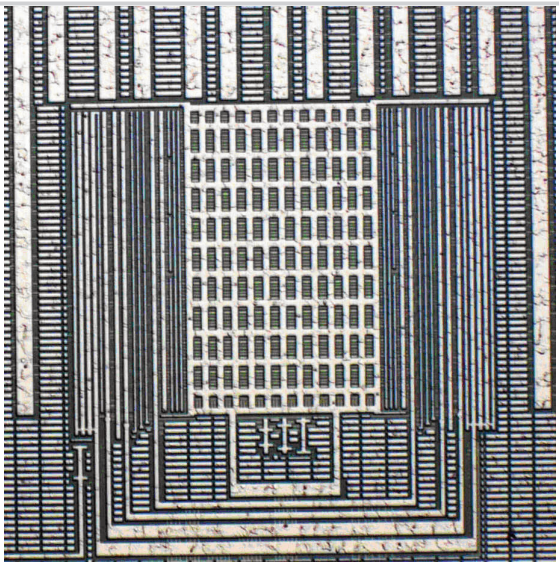

Figure 16.7.7: Die Micrograph.

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