Basic Opamp Design
and Compensation

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Transistor Model Summary

General Constants

Transistor charge — \( q = 1.602 \times 10^{-19} \text{ C} \)
Boltzmann constant — \( k = 1.38 \times 10^{-23} \text{ JK}^{-1} \)
Intrinsic silicon carrier concentration (300 K) — \( n_i = 1.1 \times 10^{16} \text{ carriers/m}^3 \)
Relative permittivity of oxide — \( K_{ox} \approx 3.9 \)
Relative permittivity of silicon — \( K_s \approx 11.8 \)

MOS Transistor Parameters

Electron mobility (typical) — \( \mu_n = 0.05 \text{ m}^2/\text{V} \cdot \text{s} \)
Hole mobility (typical) — \( \mu_p = 0.02 \text{ m}^2/\text{V} \cdot \text{s} \)
Oxide thickness (typical) — \( t_{ox} = 0.02 \mu\text{m} \)
Transistor Model Summary

Gate capacitance per unit area — \[ C_{ox} = \frac{K_{ox}\varepsilon_o}{t_{ox}} \approx 1.9 \times 10^{-3} \text{ pF/(\mu m)}^2 \]

Device parameters (typ) — \[ \mu_n C_{ox} = 90 \text{ \mu A/V}^2, \mu_p C_{ox} = 30 \text{ \mu A/V}^2 \]

Threshold voltages (typical) — \[ V_{tn} = 0.8 \text{ V}, V_{tp} = -0.9 \text{ V} \]

Threshold voltage adjustment — \[ V_{in} = V_{tn-0} + \gamma \left( \sqrt{V_{SB}^2 + 2\phi_F} - \sqrt{2\phi_F} \right) \]

Body effect parameter (typical) — \[ \gamma = 0.5 \text{ V}^{1/2} \]

Fermi potential difference (typical) — \[ \phi_F = 0.35 \text{ V} \]

Effective Gate-Source Voltage, \( V_{eff} \)

Effective gate-source voltage — \[ V_{eff} = V_{GS} - V_{tn} \]

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Triode and Active Regions

\[ I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \]

\[ I_D = \frac{\mu_n C_{ox} W}{2} (V_{GS} - V_{tn})^2 \]

- Cutoff Region: \( V_{GS} < V_{tn} \)
- Triode Region: \( V_{GS} > V_{tn}, \ V_{DS} \leq V_{eff} \)
- Active Region: \( V_{GS} > V_{tn}, \ V_{DS} \geq V_{eff} \)
**MOS Triode Equations**

Region of operation — $V_{GS} > V_{tn}$, $V_{DS} \leq V_{eff}$

Drain current — $I_D = \mu_n C_{ox} \left( \frac{W}{L} \right) \left( (V_{GS} - V_{tn})V_{DS} - 1.7 \frac{V_{DS}^2}{2} \right)$

1.7 typical term is due to body effect along channel

Small-Signal Model in Triode Region (for $V_{DS} << V_{eff}$)

$$r_{ds} = \frac{1}{\mu_n C_{ox} \left( \frac{W}{L} \right) V_{eff}}$$

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**MOS Active (or Pinch-Off) Equations**

Region of operation — $V_{GS} > V_{tn}$, $V_{DS} \geq V_{eff}$

Drain current — $I_D = \left( \frac{\mu_n C_{ox}}{2} \right) \left( \frac{W}{L} \right) (V_{GS} - V_{tn})^2 \left[ 1 + \lambda(V_{DS} - V_{eff}) \right]$ \[1\]

Output impedance constant — $\lambda \propto \frac{1}{L \sqrt{V_{DG} + V_{tn} + 0.9}}$

0.9 term is due to built-in junction potential

Effective gate-source voltage — $V_{eff} = V_{GS} - V_{tn} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$

(ignoring output impedance)
**MOS Active Equations**

**Small-Signal Model (Active Region)**

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**Transconductance**

$g_m = \mu_n C_{ox} \left( \frac{W}{L} \right) V_{eff}$

$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$

$g_m = \frac{2I_D}{V_{eff}}$

**Body effect transconductance**

$g_s = \frac{\gamma g_m}{2\sqrt{V_{SB} + |2\phi_f|}}$

**Body effect transconductance (typical)**

$g_s \approx 0.2g_m$

**Output impedance**

$r_{ds} = \frac{1}{\lambda I_D}$

$r_{ds} \approx \alpha \frac{L}{I_D} \sqrt{V_{DG} + V_{tn}}$ where $\alpha = 5 \times 10^6 \sqrt{\text{V/m}}$
Two-Stage CMOS Opamp

- Useful for describing many opamp design concepts
- Still used for low voltage applications

![Diagram]

Bias circuitry
Differential-input
first stage
Common-source
second stage
Output
buffer

all transistor lengths = 1.6 μm
Opamp Gain

- 3rd stage NOT included if driving capacitive loads
- Typical gains of 50-100 for each of stage 1 and 2

First Stage

- Differential to single-ended
  \[ A_{v1} = g_{m1} (r_{ds2} \parallel r_{ds4}) \]  
  \[ g_{m1} = \sqrt{2\mu p C_{ox} \frac{W}{L} I_{D1}} = \sqrt{2\mu p C_{ox} \frac{W}{L} \frac{I_{bias}}{2}} \]

Second Stage

- Common-source gain
  \[ A_{v2} = -g_{m7} (r_{ds6} \parallel r_{ds7}) \]

Third Stage

- Source follower
- Typical gain — slightly less than 1 (say 0.9)
- Note — \( g_{ds} = 1/r_{ds} \) and \( G_L = 1/R_L \)
  \[ A_{v3} \approx \frac{g_{m8}}{G_L + g_{m8} + g_{s8} + g_{ds8} + g_{ds9}} \]
- \( g_s \) is body-effect conductance and equals zero if source tied to substrate
- \( G_L \) is the load conductance at output
**Frequency Response**

- $C_C$ dominates at all freq except unity-gain freq
- Ignore $Q_{16}$ for now (used for lead compensation)
- Miller effect results in
  \[
  (C_{eq} = C_C(1 + A_2)) \approx C_C A_2
  \]

- At midband freq
  \[
  A_1 = g_m Z_{out} = g_m/(sC C A_2)
  \]

- Overall gain (assuming $A_3 \approx 1$)
  \[
  A_v(s) = A_2 A_1 = g_m/(sC C)
  \]

resulting in a unity-gain frequency of
  \[
  \omega_{ta} = g_m/C C
  \]
**Freq Response**

- First-order model

\[ 20 \log(A_1 A_2) \]

 Gain (dB)

\[ \omega_{ta} \approx \frac{g_{m1}}{C_C} \]

\[ \omega_{p1} \]

Freq (log)

\[ 0 \]

\[ -90 \]

\[ -180 \]

Phase (degrees)

**Slew Rate**

- Max rate output changes when input signal large
- All Q5 bias current goes into Q1 or Q2

\[ SR \equiv \left. \frac{dv_{out}}{dt} \right|_{\text{max}} = \frac{I_C}{C_C} \max = \frac{I_{D5}}{C_C} = \frac{2I_{D1}}{C_C} \]

\[ (9) \]

\[ I_{D1} \text{ is nominal bias current of input transistors} \]

- Using \( C_C = \frac{g_{m1}}{\omega_{ta}} \) and \( g_{m1} = \sqrt{2 \mu p C_{ox} \left( \frac{W}{L} \right)} I_{D1} \)
**Slew Rate**

\[ SR = \frac{2I_{D1}}{\sqrt{2\mu_p C_{ox}(W/L)_{1}I_{D1}}} \omega_{ta} = V_{eff1} \omega_{ta} \quad (10) \]

where \( V_{eff1} = \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W/L)_{1}}} \)

- Normally, little control over \( \omega_{ta} \) for a given power diss
- Increase slew-rate by increasing \( V_{eff1} \)
- This is one of main reasons for using p-channel input stage — higher slew-rate

**Systematic Offset Voltage**

- To ensure inherent offset voltage does not exist, design should satisfy
  \[ \frac{(W/L)_{7}}{(W/L)_{4}} = 2 \frac{(W/L)_{6}}{(W/L)_{5}} \quad (11) \]
  - Ensures nominal current through Q7 equals Q6
  - Found by noting
    \[ I_{D5} = 2I_{D3} = 2I_{D4} \quad (12) \]
    and
    \[ V_{GS7} = V_{DS3} = V_{GS4} \quad (13) \]
  - then setting \( I_{D7} = I_{D6} \)
N-Channel or P-Channel Input Stage

- Can also build complement opamp with an n-channel input diff pair and second-stage p-channel stage

P-channel Advantages

- Higher slew-rate — For fixed bias current, $V_{eff}$ is larger (assuming similar widths used for max gain)
- Higher unity-gain freq — higher transconductance of second stage which is proportional to unity-gain freq
- Lower 1/f noise — holes less likely to be trapped — p-channel transistors have lower 1/f noise

N-channel Advantage

- Lower thermal noise — thermal noise is lowered by high transconductance of first stage

Opamp Compensation

- Feedback circuit $\beta$ assumed to be freq independent

\[
\beta = \frac{R_1}{R_1 + R_2}
\]

\[
\beta = \frac{C_2}{C_1 + C_2}
\]
General Opamp Compensation

- Model $A(s)$ by
  \[ A(s) = \frac{A_0}{(1 + s/\omega_{p1})(1 + s/\omega_{eq})} \]  
  (14)

- $\omega_{p1}$ — first dominant-pole frequency
- $\omega_{eq}$ — pole frequency modelling higher-freq poles.
- $\omega_{eq}$ found from simulation — frequency with $-135^\circ$ phase shift ($-90^\circ$ due to $\omega_{p1}$ and another $-45^\circ$ due to higher-frequency poles and zeros)
- Closed loop gain given by
  \[ A_{CL}(s) = \frac{A(s)}{1 + \beta A(s)} \]  
  (15)

General Opamp Compensation

\[ A_{CL}(s) = \frac{A_{CL0}}{1 + \frac{s(1/\omega_{p1} + 1/\omega_{eq})}{1 + \beta A_0} + \frac{s^2}{(1 + \beta A_0)(\omega_{p1}\omega_{eq})}} \]  
(16)

where $A_{CL0} = A_0/(1 + \beta A_0) \approx 1/\beta$

- Compare to a general second-order equation
  \[ H_2(s) = \frac{K\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} = \frac{K}{1 + \frac{s}{\omega_0Q} + \frac{s^2}{\omega_0^2}} \]  
  (17)

  \[ \% \text{ overshoot} = 100e^{\sqrt{4Q^2 - 1}} \]  
  (18)
**General Opamp Compensation**

- Equating 2 equations above results in
  \[
  \omega_0 = \sqrt{(1 + \beta A_0)(\omega_{p1}\omega_{eq})} \approx \sqrt{\beta A_0\omega_{p1}\omega_{eq}} \tag{19}
  \]
  \[
  Q = \frac{\sqrt{(1 + \beta A_0)/\omega_{p1}\omega_{eq}}}{1/\omega_{p1} + 1/\omega_{eq}} \approx \frac{\beta A_0\omega_{p1}}{\omega_{eq}} \tag{20}
  \]

- To find relationship between \( Q \) and phase-margin we look at the loop gain, \( LG(s) \)
  \[
  LG(s) = \beta A(s) = \frac{\beta A_0}{(1 + s/\omega_{p1})(1 + s/\omega_{eq})} \tag{21}
  \]

- To find a relationship for the loop-gain unity-gain freq
  \[
  |LG(j\omega_t)| = 1 \tag{22}
  \]

- And rearrange and use approx that \( \omega_t \gg \omega_{p1} \)
  \[
  \frac{\beta A_0\omega_{p1}}{\omega_{eq}} = \left(\frac{\omega_t}{\omega_{eq}}\right) \sqrt{1 + \left(\frac{\omega_t}{\omega_{eq}}\right)^2} \tag{23}
  \]
  so that
  \[
  Q = \sqrt{\left(\frac{\omega_t}{\omega_{eq}}\right) \sqrt{1 + \left(\frac{\omega_t}{\omega_{eq}}\right)^2}} \tag{24}
  \]

- Would also like to relate **phase-margin** with \( \omega_t/\omega_{eq} \) and Q factor
**Phase-Margin**

-20 dB/decade

Loop Gain (dB) = \(20 \log_{10}(LG(j\omega))\)

\[\omega_p\]

\[\omega_{ta}\]

Gain Margin (GM)

\[\omega_{p1}\]

\[\omega_{ta}\]

Phase Margin (PM)

\[\omega_{p1}\]

\[\omega_{ta}\]

**General Opamp Compensation**

\[PM = \angle LG(j\omega_t) - (-180^\circ) = 90^\circ - \tan^{-1}(\omega_t/\omega_{eq})\] (25)

where \(\omega_{p1}\) adds 90° phase shift

\[\omega_t/\omega_{eq} = \tan(90^\circ - PM)\] (26)

- If non-dominant poles remains unchanged, \(\omega_t\) independent of \(\beta\) for optimally compensated circuit!

<table>
<thead>
<tr>
<th>PM (Phase margin)</th>
<th>(\omega_t/\omega_{eq})</th>
<th>Q factor</th>
<th>Percentage overshoot for a step input</th>
</tr>
</thead>
<tbody>
<tr>
<td>55°</td>
<td>0.700</td>
<td>0.925</td>
<td>13.3%</td>
</tr>
<tr>
<td>60°</td>
<td>0.580</td>
<td>0.817</td>
<td>8.7%</td>
</tr>
<tr>
<td>65°</td>
<td>0.470</td>
<td>0.717</td>
<td>4.7%</td>
</tr>
<tr>
<td>70°</td>
<td>0.360</td>
<td>0.622</td>
<td>1.4%</td>
</tr>
<tr>
<td>75°</td>
<td>0.270</td>
<td>0.527</td>
<td>0.008%</td>
</tr>
</tbody>
</table>
Compensating the 2-Stage Opamp

Q16 has $V_{DS16} = 0$ and is hard in the triode region.

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox} \left( \frac{W}{L} \right)_{16} V_{eff16}}$$

(Small signal analysis) — without $R_C$ present, right-half plane zero occurs and worsens phase-margin.
Compensating the 2-Stage Opamp

- Including $R_C$ (through Q16) places zero at

$$\omega_z = \frac{-1}{C_C(1/g_m7 - R_C)} \quad (28)$$

- Zero moved to left-half plane to aid compensation
- Good practical choice is

$$\omega_z = 1.2 \omega_t \quad (29)$$

satisfied by letting

$$R_C \approx \frac{1}{1.2g_m1} \quad (30)$$

since $\omega_t \approx g_m1/C_C$ and $\omega_z \approx 1/(R_CC_C)$ if $R_C \gg 1/g_m7$

Design Procedure

1) Find $C_C$ with $R_C=0$ for a $55^\circ$ phase margin
   — Arbitrarily choose $C'_C \approx 5$ pF and set $R_C = 0$
   — Using SPICE, find frequency $\omega_t$ where a $-125^\circ$ phase shift exists, define gain as $A'$
   — Choose new $C_C$ so $\omega_t$ becomes unity-gain frequency of the loop gain — results in a $55^\circ$ phase margin.
   — Achieved by setting $C_C = C'_CA'$
   — Might need to iterate on $C_C$ a couple of times using SPICE
Design Procedure

2) Choose $R_C$ according to

$$R_C = \frac{1}{1.2 \omega_t C_C} \quad (31)$$

— Increases $\omega_t$ by about 20 percent, leaving zero near final $\omega_t$

— Check that gain continues to decrease at frequencies above the new $\omega_t$

3) If phase margin not adequate, increase $C_C$ while leaving $R_C$ constant

Design Procedure

4) Replace $R_C$ by a transistor

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox} \left( \frac{W}{L} \right)_{16} V_{eff16}} \quad (32)$$

— SPICE can be used again to fine-tune the device dimensions to optimize phase margin
Process and Temperature Independence

• Can show non-dominant pole roughly given by

\[ \omega_{p2} \approx \frac{g_{m7}}{C_1 + C_2} \]  

(33)

• Recall zero given by

\[ \omega_{z} = \frac{-1}{C_C \left(1/g_{m7} - R_C\right)} \]  

(34)

• If \( R_C \) tracks inverse of \( g_{m7} \) then zero will track \( \omega_{p2} \)

\[ R_C = r_{ds16} = \frac{1}{\mu_n C_{ox} (W/L)_{16} V_{eff16}} \]  

(35)

\[ g_{m7} = \mu_n C_{ox} (W/L)_{7} V_{eff7} \]  

(36)

Process and Temperature Independence

• Need to ensure \( V_{eff16}/V_{eff7} \) independent of process and temperature variations

• First set \( V_{eff13} = V_{eff7} \) which makes \( V_a = V_b \)
Process and Temperature Independence

\[ \sqrt{\frac{2I_{D7}}{\mu_n C_{ox}(W/L)_7}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} \]  
\[ \frac{I_{D7}}{I_{D13}} = \frac{(W/L)_7}{(W/L)_{13}} \]  

- Since \( V_a = V_b \) and gates of Q12 and Q16 same

\[ V_{eff12} = V_{eff16} \]  
\[ \frac{V_{eff7}}{V_{eff16}} = \frac{V_{eff13}}{V_{eff12}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \frac{2I_{D12}}{\sqrt{\mu_n C_{ox}(W/L)_{12}}} \]  

Stable Transconductance Biasing

- Can bias on-chip \( g_m \) to a resistor

\[ V_{GS13} = V_{GS15} + I_{D15}R_B \]  
\[ \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D15}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D15}R_B \]  

- But \( I_{D13} = I_{D15} \) and rearrange

\[ \frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{13}I_{D13}}} \left[ 1 - \frac{W/L_{12}}{W/L_{15}} \right] = R_B \]  

- Recall \( g_{m13} = \sqrt{2\mu_n C_{ox}(W/L)_{13}I_{D13}} \)

\[ g_{m13} = 2 \left[ 1 - \frac{(W/L)_{13}}{(W/L)_{15}} \right] / R_B \]
Stable Transconductance Biasing

- Transconductance of $Q_{13}$ determined by geometric ratios only
- Independent of power-supply voltages, process parameters, temperature, etc.
- For special case $(W/L)_{15} = 4(W/L)_{13}$

$$g_{m13} = \frac{1}{R_B}$$

- Note that high-temp will decrease mobility and hence increase effective gate-source voltages
- Roughly 25% increase for 100 degree increase
- Requires a start-up circuit (might have all 0 currents)