Comparators

David Johns and Ken Martin
University of Toronto
(johns@eecg.toronto.edu)
(martin@eecg.toronto.edu)

Opamp does not work well!

\[ V_{\text{out}} = \text{sgn}(V_{\text{in}} - V_r) \]

Slow
- Compensation capacitor lowers slew-rate (should disconnect capacitor for higher speed)

Inaccurate
- Offset of input stage might be 2mV - 10mV

Limited input range
- Common-mode input range poor — not good if \( V_r \) is near one of power supplies (flash A/D converters)
Comparators — Offset Cancellation

- On \( \phi_1 \), opamp offset stored on C as well as reference voltage, \( V_r \) — comparator set to “trigger point”.
- On \( \phi_2 \), evaluation phase — difference between \( V_r \) and \( V_{in} \) amplified

Comparators - Offset Cancellation

- Shown phases does not require charging of C (on \( \phi_2 \), capacitor is not charged)
- \( \phi_{1a} \) is advanced version of \( \phi_1 \) to reduce charge-injection effects (more below)
- Opamp compensation cap should be disconnected during evaluation phase for faster slew-rate

Advantages
- Very low offset possible
- Input common-mode range of amplifier near zero
- Also reduces 1/f noise

Disadvantages
- Requires floating capacitor and switches
**Charge Injection Errors**

- Channel charge for an ON transistor (with zero Vds)
  \[ Q_{CH} = WLC_{ox} V_{eff} = WLC_{ox}(V_{GS} - V_t) \]  
  \[ (1) \]
- When turned off quickly, 1/2 charge flows out to each of source and drain
- Also overlap capacitances for each transistor

![Diagram](image)

**Making Charge Injection Signal Independent**

- Advance Q3 so it turns off first [Haigh, 83]

**Reasoning**

- Q3 off causes right side of C to be open circuited
- When Q2 turns off, charge injection cannot change charge on C
- When Q1 on, \( V' \) goes to \( V_{in} \) and \( V'' \) goes back to correct value (opamp offset voltage)
**Minimizing Charge Injection Errors**

- Can use large C but slows down circuit
- Fully differential design

![Circuit Diagram]

- Only mismatch in charge injection cause errors
- Likely 10 times smaller than single-ended case

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**Mult-Stage Comparator**

![Circuit Diagram]

- [Poujois, 78] [Vittoz, 85]
- Clock feedthrough stored on coupling caps
- Used together with fully-diff design
Multi-Stage Comparator

- When $\phi'_1$ goes low, charge OA1 output glitches but recovers
- OA1 input side goes negative causing OA1 output to go positive
- Since OA2 still being reset, error stored on C2

Latched Comparators

- 1 or 2 stages of preamp followed by track-and-latch
**Latched Comparators**

- Preamp used to improve resolution and reduce kickback
- Kickback result of charge transfer to inputs when going from track to latch mode
- Use preamp and match input impedances
- Preamp and track both have gain
- Positive feedback regenerates signal to logic levels
- Hysteresis effects reduced by setting internal nodes to known values each switching interval
- Known values likely setting latch to its trip point

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**Example CMOS Comparator**

- [Song, 90]
Example CMOS Comparator

- [Norsworthy, 89]