**Data Converter Fundamentals**

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**Introduction**

- Two main types of converters

**Nyquist-Rate Converters**

- Generate output having a one-to-one relationship with a single input value.
- Rarely sample at Nyquist-rate because of need for anti-aliasing and reconstruction filters.
- Typically 3 to 20 times input signal’s bandwidth.

**Oversampling Converters**

- Operate much faster than Nyquist-rate (20 to 512 times faster)
- Shape quantization noise out of bandwidth of interest, post signal processing filters out quantization noise.
**Ideal D/A Converter**

- $B_{in}$ defined to be an $N$-bit digital signal (or word)
  \[ B_{in} = b_12^{-1} + b_22^{-2} + \ldots + b_N2^{-N} \]  
- $b_i$ equals 1 or 0 (i.e., $b_i$ is a binary digit)
- $b_1$ is MSB while $b_N$ is LSB
- Assume $B_{in}$ is positive — unipolar conversion

- Output voltage related to digital input and reference voltage by
  \[ V_{out} = V_{ref}(b_12^{-1} + b_22^{-2} + \ldots + b_N2^{-N}) \]
  \[ = V_{ref}B_{in} \]
- Max $V_{out}$ is $V_{ref}(1 - 2^{-N})$
- Multiplying DAC realized by allowing $V_{ref}$ to be another input signal
- Ideal DAC has well-defined values (not same for A/D)
**Ideal DAC Converter**

![Diagram of Ideal DAC Converter]

- \( V_{LSB} = \frac{V_{ref}}{2^N} \) and \( 1 \text{ LSB} = \frac{1}{2^N} \)

**Example**

- An 8-bit D/A converter has \( V_{ref} = 5 \text{ V} \).
- What is the output voltage when \( B_{in} = 10110100 \)?

\[
B_{in} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} = 0.703125 \quad (3)
\]

\[
V_{out} = V_{ref}B_{in} = 3.516 \text{ V} \quad (4)
\]
- Find \( V_{LSB} \).

\[
V_{LSB} = \frac{5}{256} = 19.5 \text{ mV} \quad (5)
\]
Ideal A/D Converter

\[ V_{\text{ref}}(b_12^{-1} + b_22^{-2} + \ldots + b_N2^{-N}) = V_{\text{in}} \pm V_x \]  

(6)

where

\[ -\frac{1}{2}V_{\text{LSB}} \leq V_x < \frac{1}{2}V_{\text{LSB}} \]  

(7)

Ideal A/D Converter

- A range of valid input values produces same digital output word — quantization error.
- No quantization error in D/A converter case.
**Ideal A/D Converter**

- Transitions offset by $0.5V_{LSB}$ so midpoint are same as D/A case

**Quantizer Overload**

- Quantization error limited to $\pm V_{LSB}/2$ otherwise quantizer is said to be “overloaded”.
- Overloading occurs when input signal is beyond one $V_{LSB}$ of the two last transition voltages.
- In 2-bit example, input should be greater than $-1/8 \ V_{ref}$ and less than $7/8 \ V_{ref}$

**Quantization Noise**

\[
V_Q = V_1 - V_{in} \quad \text{or} \quad V_1 = V_{in} + V_Q
\]
Quantization Noise

- Above model is exact
  — approx made when assumptions made about $V_Q$
- Often assume $V_Q$ is white, uniformly distributed number between $\pm V_{LSB}/2$

Quantization Noise

- Average of quantization noise is zero.
- Power of quantization noise can be shown to equal
  \[ V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} \]  
  \[ (9) \]
- Each extra bit results in noise power decrease of 3dB
- Noise power is \textit{independent} of sampling frequency
- If assume input signal is a sinusoid of peak amplitude of $V_{ref}/2$

\[
SNR = 20 \log \left( \frac{V_{in(rms)}}{V_{Q(rms)}} \right) = 20 \log \left( \frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})} \right)
\]

\[
SNR = 6.02N + 1.76 \text{ dB}
\]
Quantization Noise

10-bit

- SNR reaches max when input signal is max
- (might improve SNR if oversampling used)

Example

- A 100-mVpp sinusoidal signal is applied to an ideal 12-bit A/D converter for which \( V_{\text{ref}} = 5 \text{ V} \).
- Find the SNR of the digitized output signal.
- 
- First, find max SNR if full-scale sinusoidal waveform of ±2.5 V applied
  \[
  \text{SNR}_{\text{max}} = 6.02 \times 12 + 1.76 = 74 \text{ dB} \tag{10}
  \]
- Since input is only ±100-mV it is 28 dB below full scale, so SNR of digitized output is
  \[
  \text{SNR} = 74 - 28 = 46 \text{ dB} \tag{11}
  \]
Signed Codes

- Often need converters for both positive and negative signals — signed codes

Sign Magnitude
- Neg numbers simply invert MSB

1’s Complement
- Neg numbers invert all bits

Offset Binary
- Assign 000… to most negative number and count up

2’s Complement
- Invert MSB of offset binary case or ...
- Neg numbers are 1 LSB larger than 1’s complement

<table>
<thead>
<tr>
<th>Number</th>
<th>Normalized number</th>
<th>Sign magnitude</th>
<th>1’s complement</th>
<th>Offset binary</th>
<th>2’s complement</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3</td>
<td>+3/4</td>
<td>011</td>
<td>011</td>
<td>111</td>
<td>011</td>
</tr>
<tr>
<td>+2</td>
<td>+2/4</td>
<td>010</td>
<td>010</td>
<td>110</td>
<td>010</td>
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<tr>
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<td>+1/4</td>
<td>001</td>
<td>001</td>
<td>101</td>
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<tr>
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<tr>
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<td>(–0)</td>
<td>(100)</td>
<td>(111)</td>
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<td></td>
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<td>–1/4</td>
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<td>110</td>
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<td>100</td>
<td></td>
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</tr>
</tbody>
</table>

- 2’s complement most common when doing signal processing
2’s Complement

- Each have *wrap-around* behaviour

Offset Binary

$000$ -4 $001$ -3 $010$ -2 $011$ -1 $100$ 0 $101$ 1 $110$ 2 $111$ 3

2’s Complement

$010$ -4 $011$ -3 $100$ -2 $101$ -1 $110$ 0 $111$ 1

2’s Complement Benefits

- Addition of both positive numbers is done with simple addition (nothing extra needed)
- Subtraction of $A - B$ done by complementing bits of $B$ and adding LSB into carry-in of adder
- Can go above max as long as final result is within range (no overflow hardware needed)

Example

- $2 + 3 + (-4) = 1$
  
  $010 + 011 + 100 = 101 + 100 = 001$

- Final result of 1 correct though temp result of -3 obtained
Performance Limitations

- For D/A measure, use output voltage levels
- For A/D measure, use transition points (easier than midpoints)

![Graph showing performance limitations with VLSB and Vref](image)

Offset and Gain Error

![Graph showing offset and gain error with Vout, Vref, and Vin](image)
Offset and Gain Error

- D/A converter — units of LSB: \( E_{\text{off}(D/A)} = \frac{V_{\text{out}}}{V_{\text{LSB}}} \bigg|_{0 \ldots 0} \)

- A/D converter — deviation of \( V_{0 \ldots 01} \) from \( 1/2 \text{ LSB} \)

\[
E_{\text{off}(A/D)} = \frac{V_{0 \ldots 01}}{V_{\text{LSB}}} - \frac{1}{2} \text{ LSB} \quad (12)
\]

- With gain error, set offset error to zero

\[
E_{\text{gain}(D/A)} = \left( \frac{V_{\text{out}}}{V_{\text{LSB}}} \bigg|_{1 \ldots 1} - \frac{V_{\text{out}}}{V_{\text{LSB}}} \bigg|_{0 \ldots 0} \right) - (2^N - 1) \quad (13)
\]

\[
E_{\text{gain}(A/D)} = \left( \frac{V_{1 \ldots 1}}{V_{\text{LSB}}} - \frac{V_{0 \ldots 01}}{V_{\text{LSB}}} \right) - (2^N - 2) \quad (14)
\]

Resolution and Accuracy

Resolution

- Number of distinct analog levels — \( n \) \( N \)-bit resolution can resolve \( 2^N \) distinct analog levels.

Absolute Accuracy

- Difference between the expected and actual transfer responses — includes offset, gain and linearity errors

Relative Accuracy

- After offset and gain errors removed — also called maximum integral nonlinearity error

- A 12-bit accuracy implies that the converter’s error is less than the full-scale value divided by \( 2^{12} \)
Resolution and Accuracy

- A converter may have 12-bit resolution with only 10-bit accuracy.
- Another converter may have 10-bit resolution with 12-bit accuracy.
- Accuracy greater than resolution means converter’s transfer response is very precisely controlled — better than the number of bits of resolution.

Example

- A two bit D/A (resolution 2-bits) with output levels at 0.0, 1/4, 2/4, 3/4 is ideal (infinite bit accuracy since no errors).

Integral Nonlinearity (INL) Error
**INL Error**

- After both offset and gain errors removed, *integral nonlinearity (INL) error* is deviation from a straight line.
- Can use endpoint or best fit straight lines — endpoint more conservative
- INL plotted for each digital word

![INL Error Diagram](image)

- Maximum INL also referred to as relative accuracy

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**Differential Nonlinearity (DNL) Error**

- Ideally, each step is 1 LSB away from adjacent level
- DNL defined as variation in step sizes from 1 LSB (once gain and offset errors removed)
- Example — Max DNL = 0.5 LSB has at least one step size which is either 0.5 LSB or 1.5 LSB
- As in INL error, DNL plotted for each digital word and max is maximum magnitude.

![DNL Error Diagram](image)

- Step size between 00 and 01 is 1.5 LSB
- Step size between 10 and 11 is 0.7 LSB
Monotonicity

Monotonic D/A Converters
- Where output always increases as input increases — no negative slope in transfer-response
- Important for some control loop applications
- If max DNL < 1 LSB, converter is monotonic
- Can be monotonic and have DNL > 1 LSB
- If max INL < 0.5 LSB, converter is monotonic

Missing Code A/D Converters
- Similar to monotonic but for A/D converter
- Increasing analog input skips some digital codes
- If max DNL < 1 LSB or max INL < 0.5 LSB, no missing codes

Converter Speed

A/D Conversion Time and Sampling Rate
- Conversion time — time for a single measurement
- Sampling rate — max sampling rate (typically inverse of conversion time)
- Note that converter might have latency due to pipelining

D/A Settling Time and Sampling Rate
- Settling time — time for converter to settle to within a specified resolution (typically 0.5 LSB)
- Sampling rate — max rate (typically inverse of settling time)
Sampling-Time Uncertainty

- Error due to variations in sampling time
- Consider full-scale sine wave: \[ V_{in} = \frac{V_{ref}}{2} \sin(2\pi f_{in} t) \]
- Rate of change is max at zero crossing
- If sampling time has variation \( \Delta t \), then to keep \( \Delta V \) less than 1 LSB, require that
  \[ \Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}} \]  
  \( N \) is bits
- Example — 250 MHz sinusoidal signal must keep \( \Delta t < 5 \text{ ps} \) for 8-bit accuracy
- Same 5ps for 16-bit accuracy and 1 MHz sinusoid

Dynamic Range

- Ratio of rms value of max amplitude input sinusoid to rms output noise plus distortion
- Can be expressed as \( N \), effective number of bits
  \[ \text{SNR} = 6.02N + 1.76 \text{ dB} \]  
  \( \text{SNR} \) in dB
- Often a function of freq of input signal (lower SNR as freq increases)
  — more realistic than only using INL and DNL
- Note, distortion of some converters not a function of input signal level
- Other converters (such as oversampling), distortion decreases as signal level decreases (similar to other analog circuits)
Example

- 3-bit D/A converter, $V_{\text{ref}} = 4 \text{ V}$, with following values:
  \{ 0.011 : 0.507 : 1.002 : 1.501 : 1.996 : 2.495 : 2.996 : 3.491 \}

- 1 LSB — $V_{\text{ref}}/2^3 = 0.5 \text{ V}$

- Offset voltage is 11 mV resulting in
  \[ E_{\text{off}(D/A)} = \frac{0.011}{0.5} = 0.022 \text{ LSB} \]  \hspace{1cm} (17)

- Gain error
  \[ E_{\text{gain}(D/A)} = \left( \frac{3.491 - 0.011}{0.5} \right) - (2^3 - 1) = -0.04 \text{ LSB} \]  \hspace{1cm} (18)

- For INL and DNL errors, first remove both offset and gain errors

- Offset error removed by subtracting 0.022 LSB

- Gain error removed by subtracting off scaled values of gain error. Example — new value for 1.002 (scaled to 1 LSB) given by
  \[ \frac{1.002}{0.5} - 0.022 + \left( \frac{2}{7} \right)(0.04) = 1.993 \]  \hspace{1cm} (19)

- Offset-free, gain-free, scaled values are
  \{ 0.0 : 0.998 : 1.993 : 2.997 : 3.993 : 4.997 : 6.004 : 7.0 \}  \hspace{1cm} (20)

- INL errors — Since now in units of LSBs, given by difference between values and ideal values
  \{ 0 : -0.002 : -0.007 : -0.003 : -0.007 : -0.003 : 0.004 : 0 \}  \hspace{1cm} (21)

- DNL errors — difference between adjacent values and 1 LSB
  \{-0.002 : -0.005 : 0.004 : -0.004 : 0.004 : 0.007 : -0.004 \}  \hspace{1cm} (22)
Example

- A full-scale sinusoidal is applied to a 12-bit A/D
- If fundamental has a normalized power of 1 W and remaining power is 0.5 μW, what is the effective number of bits for the converter?

\[ SNR = 6.02N_{eff} + 1.76 \]  \hspace{1cm} (23)

- In this case, SNR given by

\[ SNR = 10 \log \left( \frac{1}{0.5 \times 10^{-6}} \right) = 63 \text{ dB} \]  \hspace{1cm} (24)

resulting in

\[ N_{eff} = \frac{63 - 1.76}{6.02} = 10.2 \text{ effective bits} \]  \hspace{1cm} (25)