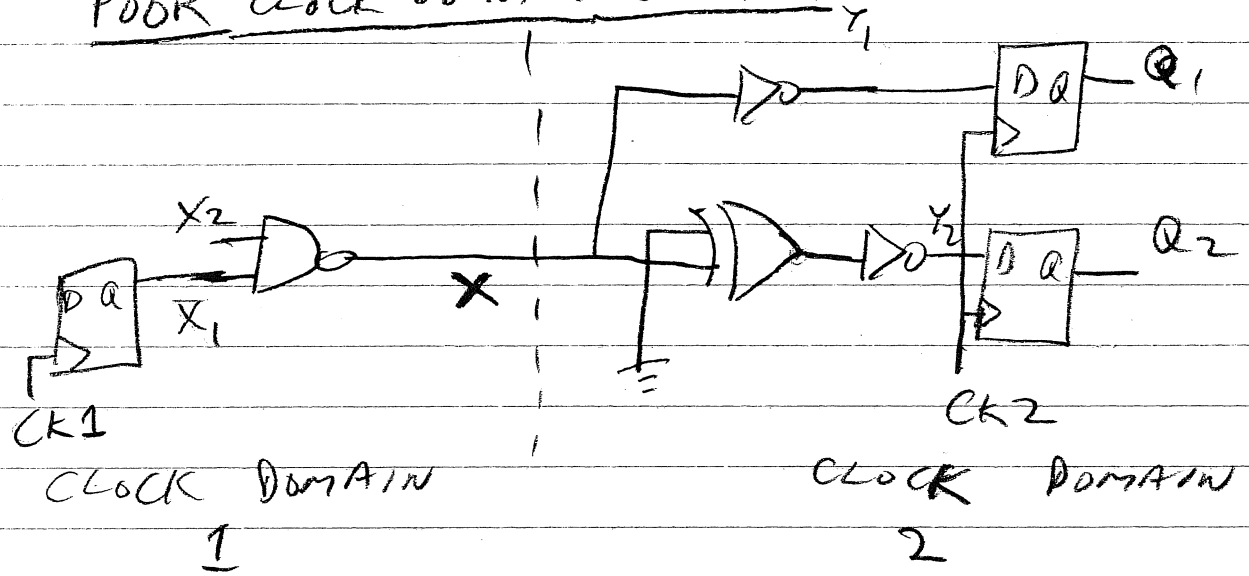
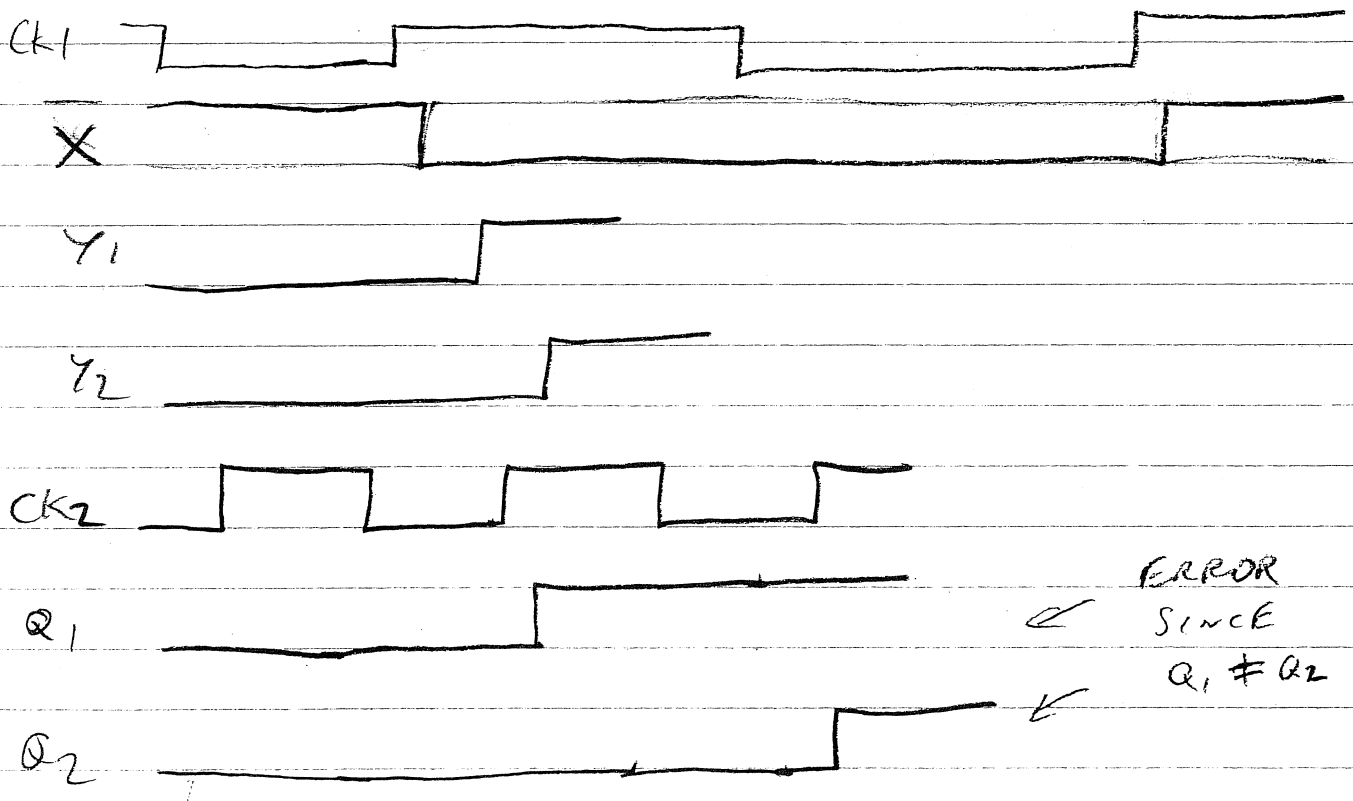
# SYNCHRONIZERS & METASTABILITY.

CONSIDER AN ASYNCHRONOUS SIGNAL OR 2 DIFFERENT CLOCK DOMAINS.

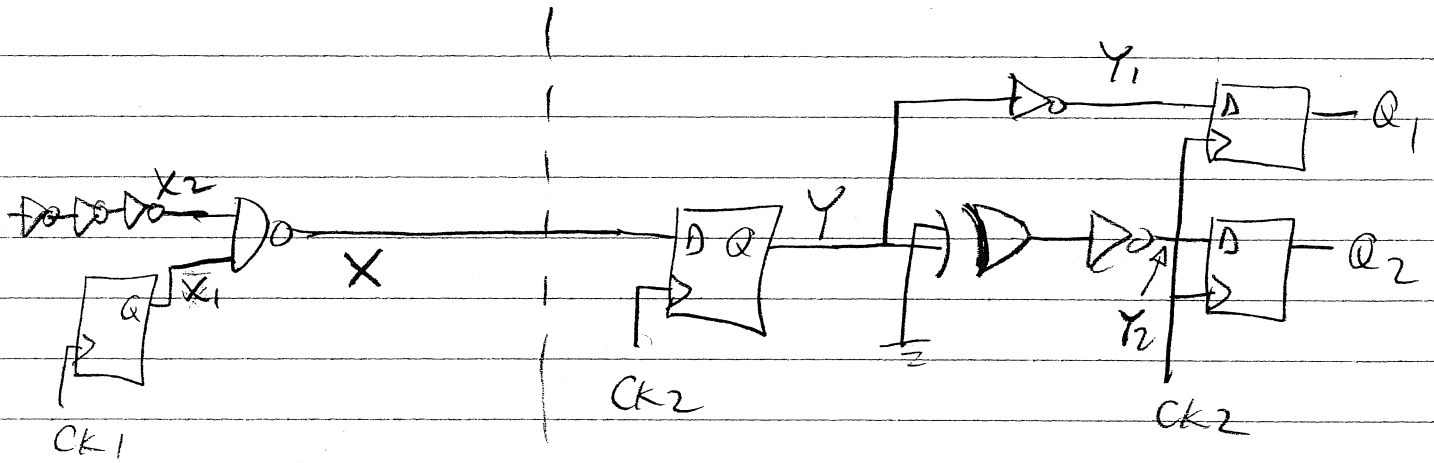
## POOR CLOCK DOMAIN CROSSING

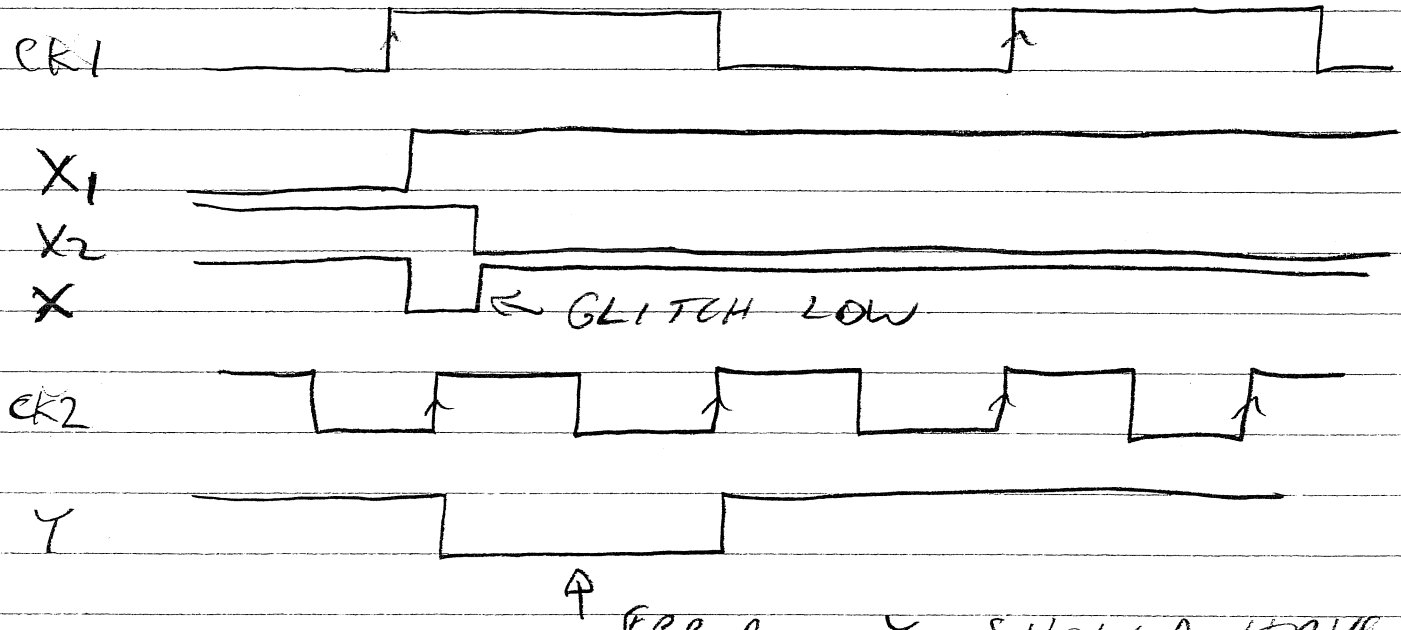


ERROR SINCE $Y_1$ & $Y_2$ MAY HAVE DIFFERENT DELAYS

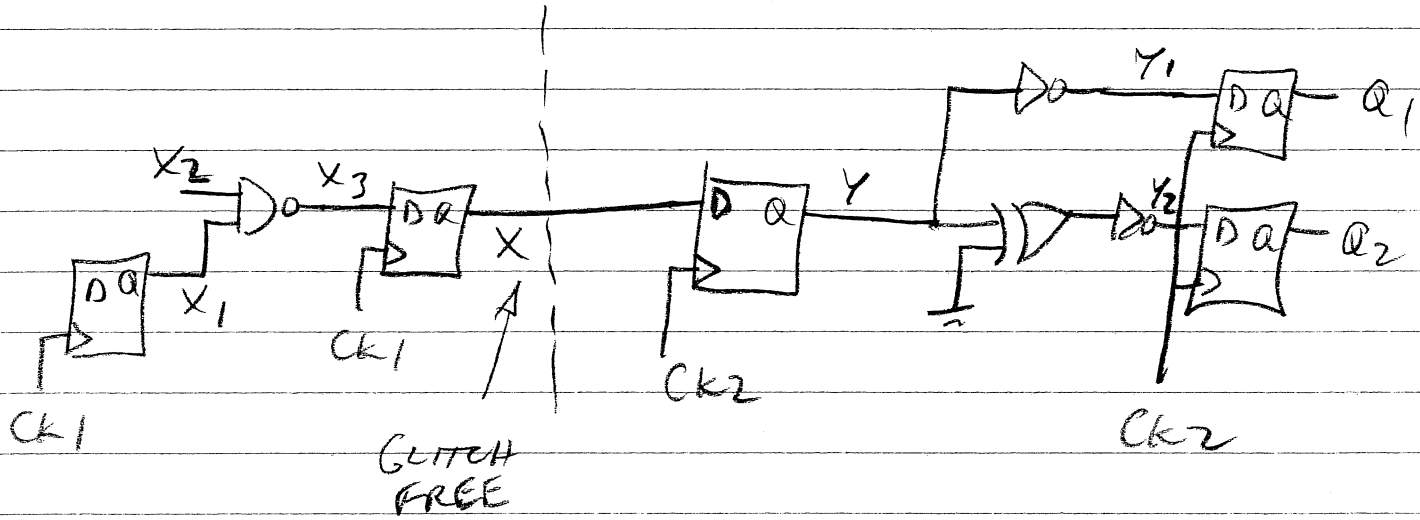
BETTER SOLUTION 1

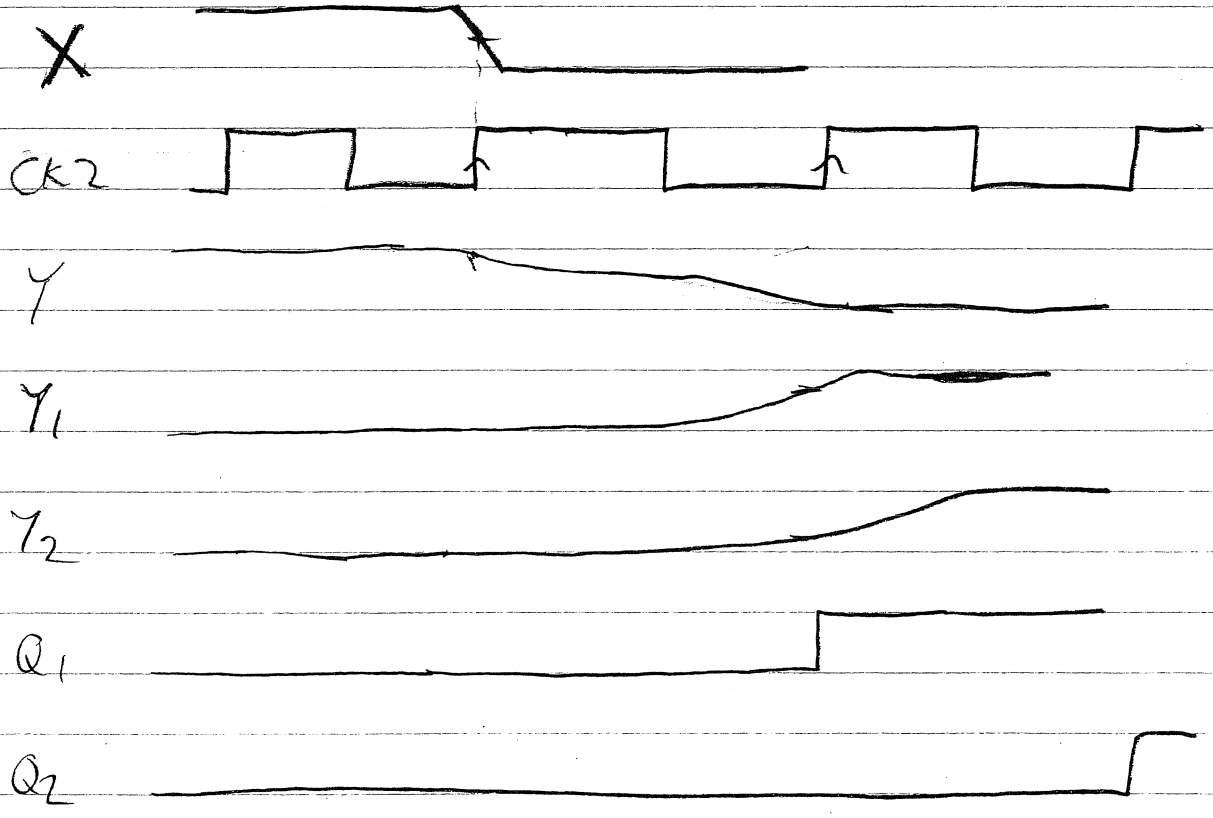



ERROR Y SHOULD HAVE REMAINED HIGH BUT PICKED UP A GLITCH

# BETTER SOLUTION 2

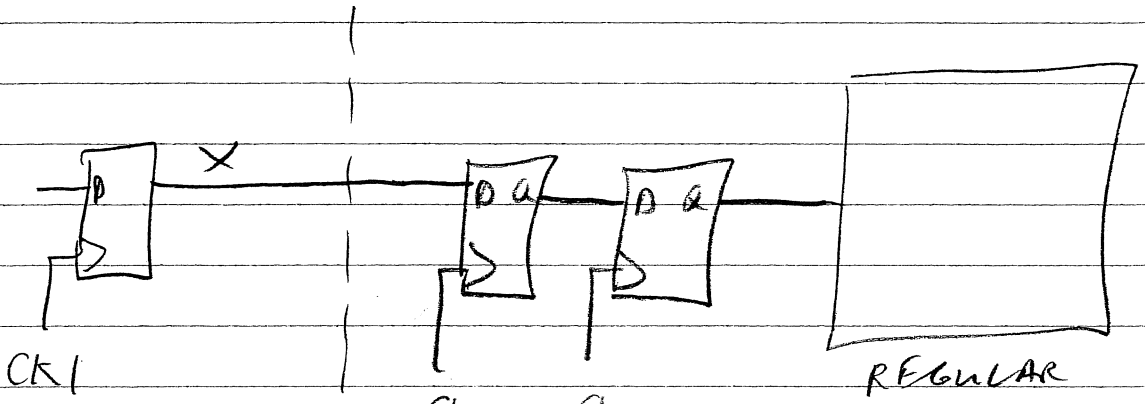



ERROR DUE TO METASTABILITY!!

SAMPLING X AT $V_M$ + UNKNOWN $t_{pcq}$

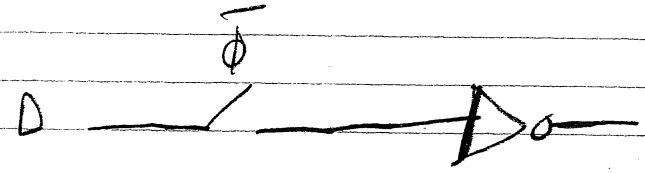
# BETTER (BEST) SOLUTION

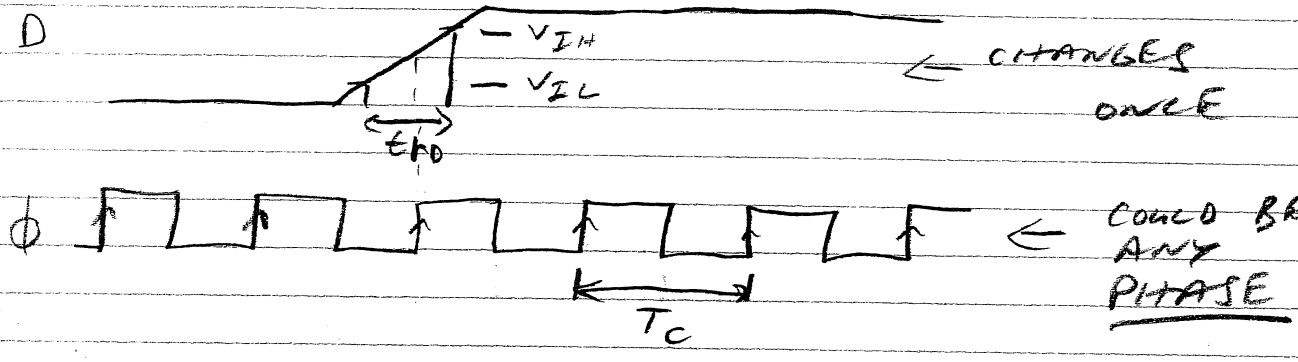



1 LATCH
TO
ELIMINATE
GLITCHES

2 LATCHES
TO REDUCE
METASTABILITY
ERRORS
(MORE LATCHES
FURTHER REDUCES METASTABILITY
ERRORS BUT USUALLY
2 IS ENOUGH TO
REDUCE ERROR TO
PERHAPS 1 ERROR IN 1000 YEARS.

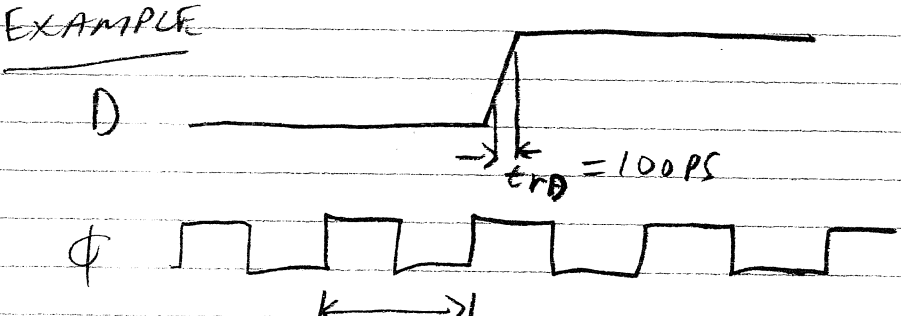
SAMPLING A SINGLE DATA TRANSITION INTO AN INVERTER WITH NO POSITIVE FEEDBACK



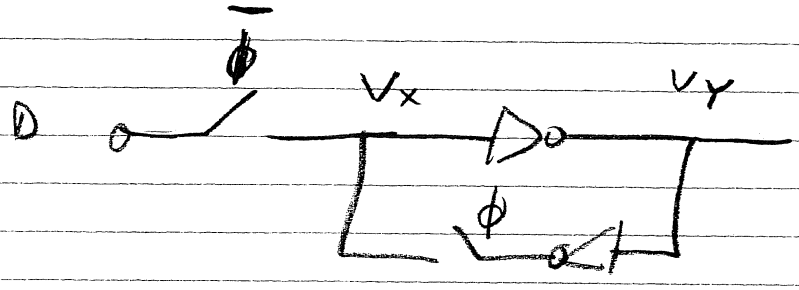

$$P_{ERROR} = \frac{t_{rD}}{T_C} \quad \text{ASSUMING} \quad T_C > t_{rD}$$

EXAMPLE



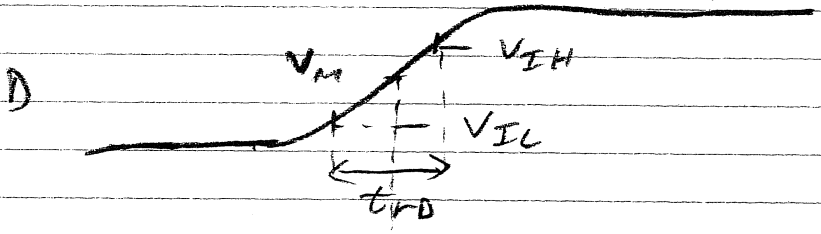

$$P_{ERROR} = \frac{100PS}{10ns} = 0.01 \quad \text{OR} \quad 1\%$$

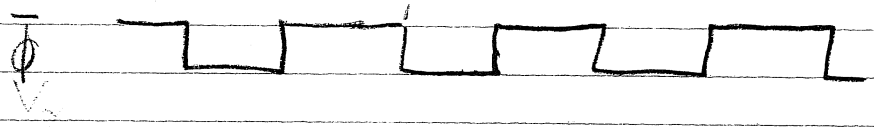
# SAMPLING A SINGLE DATA TRANSITION INTO A LATCH WITH POSITIVE FEEDBACK

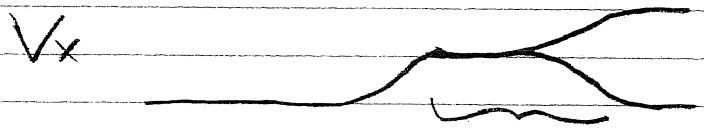



ASSUME

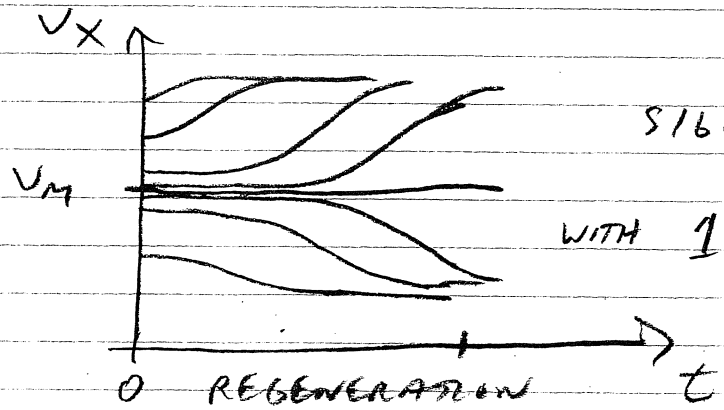
$V_M$ IS LATCH THRESHOLD




REGENERATION REGION




SIGNAL GROWS EXPONENTIALLY WITH 1ST ORDER TIME CONSTANT.

REGENERATION DUE TO POSITIVE FEEDBACK

$$V_x(t) = V_M + (V_x(0) - V_M)\, e^{+t/\tau_{LS}}$$

WHERE $\tau_{LS}$ IS LATCH TIME CONSTANT

$\tau_{LS}$ DEPENDS ON $-g_m$ OF TRANSISTORS
$-$ INTERNAL CAPACITANCES

SO IF WE WAIT T SECONDS BEFORE USING SIGNAL

$$P_{ERROR} = \frac{t_{rD}}{T_C}\left(e^{-T/\tau_{LS}}\right)$$

BECAUSE SAMPLED SIGNAL CAN BE
$e^{T/\tau_{LS}}$ TIMES SMALLER

IF N DATA TRANSITIONS/SECOND (ON AVERAGE)

$$P_{ERR\_S} = N\,\frac{t_{rD}}{T_C}\,e^{-T/\tau_{LS}} \quad [\text{ERRORS/SECOND}]$$
(ON AVERAGE)

MEAN TIME BETWEEN FAILURES

$$MTBF = \frac{1}{P_{ERR\_S}} = \frac{T_C\, e^{T/\tau_{CS}}}{N\, t_{rD}} \quad [\text{SECONDS/ERROR}]$$

$\leftarrow$ ($T_D = t_{rD}$ IN TEXTBOOK)

IF DATA HAS N TRANSITIONS/SECOND

CAN DEFINE

AVERAGE TRANSITION FREQUENCY

$F_D = N$ $\leftarrow$ (AVERAGE DATA CLOCK FREQ)

& CLOCK FREQ $F_{CLK} = \frac{1}{T_C}$

& DEFINE $K_1 = \frac{1}{t_{rD}}$

$$MTBF = \frac{K_1\, e^{T/\tau_{CS}}}{F_D\, F_{CLK}}$$

$T = T_C$ IF 2 FLOP SYNCHRONIZER USED & $T_{SETUP}$ IGNORED

EXAMPLE

GIVEN $t_{rD} = 15ps$ $\tau_{CS} = 20ps$

ASSUMING DATA AVERAGE TRANSITION FREQ

$F_D = 50MHz$

a) FIND MAX CLOCK RATE IF 2 FLOP SYNCHRONIZER USED & MTBF ≥ 1000 YEARS

$1000 \text{ YEARS} = 1000 \times 60 \times 60 \times 24 \times 365 = 3.15 e10 \text{ SECONDS}$

$$3.15 e10 = \frac{T_c \, e^{\left(\frac{T_c}{20PS}\right)}}{(50e6)(15e-12)}$$

TRIAL & ERROR GIVES $T_c = 760$ pS

$F_{CLK} = 1.32$ GHz

b) FIND MTBF IF $F_D = 1$KHz & $F_{CLK} = 100$MHz & 2 FLOP SYNCHRONIZER USED

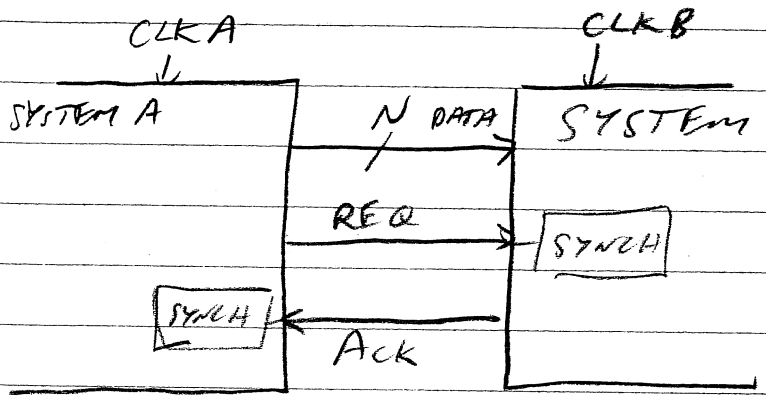
$$MTBF = \left(\frac{1}{15PS}\right)\left(\frac{e^{\left(\frac{10ns}{20PS}\right)}}{(1e3)(10^8)}\right)$$

$= 2.97 e209$ YEARS !!

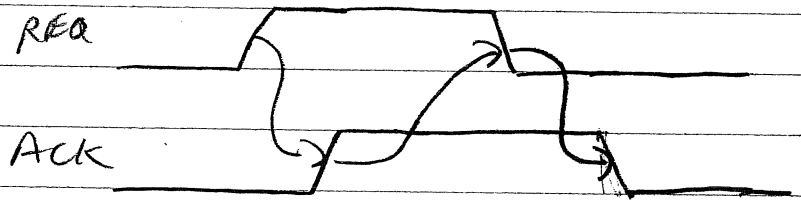
c) FIND MTBF IF $F_D = 1$KHz & $F_{CLK} = 100$MHz & NO SYNCHRONIZER USED

$$MTBF = \left(\frac{1}{15PS}\right)\left(\frac{1}{(1e3)(10^8)}\right) = 0.67 \text{ SECONDS !!}$$

COMMUNICATING AN N-BIT DATA WORD ACROSS CLOCK DOMAINS.

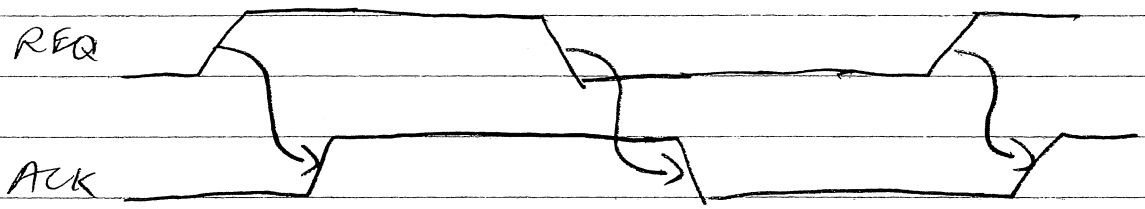



WITH N BIT DATA STABLE
(NO SYNCHRONIZER NEEDED ON DATA INPUTS)




4 PHASE HANDSHAKE

| | | | |
|---|---|---|---|
| REQ | H164 | INDICATES | DATA STABLE |
| ACK | " | " | DATA READ |
| REQ | LOW | " | ACK RECEIVED |
| ACK | LOW | " | REQ LOW RECEIVED |




2 PHASE

REQ CHANGES LOGIC LEVEL => DATA STABLE
ACK " " " => DATA READ