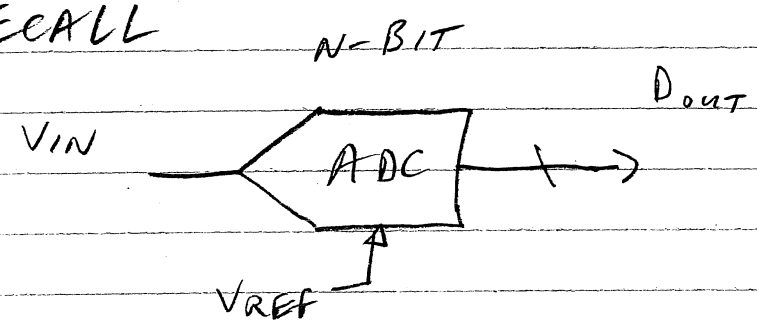
MULTI STAGE CONVERTERS

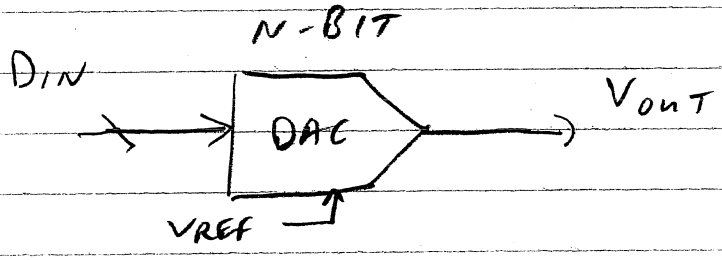
RECALL



QUANTIZATION ERROR

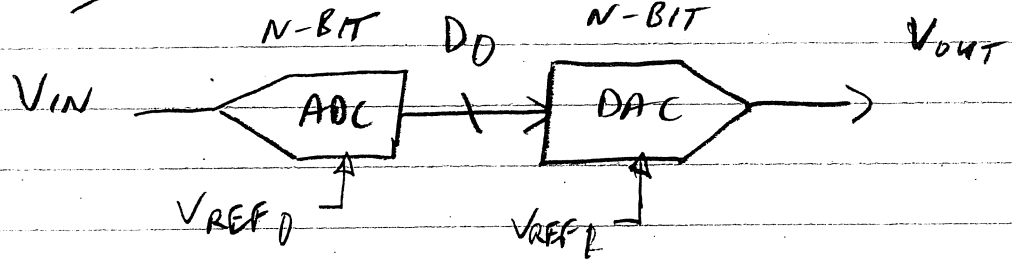
$$V_{IN} = V_{REF} D_{OUT} - E_Q$$

$$-\frac{1}{2}V_{LSB} \leq E_Q \leq \frac{1}{2}V_{LSB} = \frac{1}{2}\frac{V_{REF}}{2^N}$$



$$V_{OUT} = V_{REF} D_{IN}$$

SD



$$V_{IN} = V_{REF_0} D_0 - E_Q$$

$$D_0 = \frac{V_{IN}}{V_{REF_0}} + \frac{E_Q}{V_{REF_0}}$$

$$V_{OUT} = V_{REF_1} D_0$$

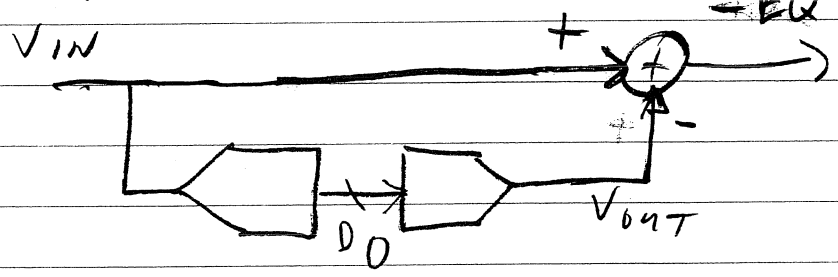
$$V_{OUT} = V_{IN}\left(\frac{V_{REF_1}}{V_{REF_0}}\right) + E_Q\left(\frac{V_{REF_1}}{V_{REF_0}}\right)$$

IF $V_{REF_1} = V_{REF_0} \equiv V_{REF}$

[FROM NOW ON ALL ADCs & DACs USE "V_{REF}"]

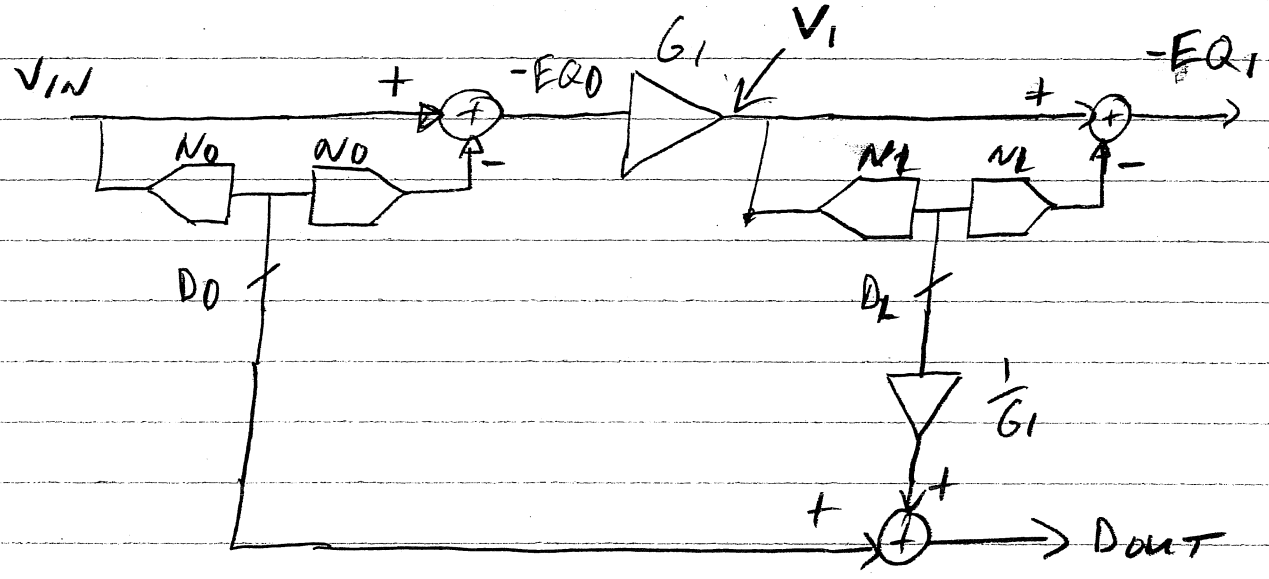
$$V_{OUT} = V_{IN} + E_Q$$

SO



$$D_0 = \frac{V_{IN} + E_Q}{V_{REF}}$$

MULTI-STAGE CONVERTER (2 STAGE)



$$D_0 = \frac{V_{IN} + EQ_0}{V_{REF}}$$

$$D_1 = \frac{-G_1 EQ_0 + EQ_1}{V_{REF}}$$

$$D_{OUT} = D_0 + \frac{1}{G_1} D_1$$

$$= \left(\frac{1}{V_{REF}}\right) V_{IN} + \frac{1}{G_1} \frac{EQ_1}{V_{REF}} \qquad (1)$$

FINAL QUANTIZATION ERROR IS $\frac{EQ_1}{G_1 V_{REF}}$

SO "G_1" TIMES SMALLER THAN $\frac{EQ_1}{V_{REF}}$

$N_{TOTAL} = N_1 + \log_2(G_1)$ OVERALL CONVERTER BITS.

TO ALLOW FOR MORE TOLERANCE ON ADC CONVERTERS USE OVERLAP CORRECTION

IF N_0 ADC IDEAL THEN

$G_1 = 2^{N_0}$ SO THAT FULL SCALE VALUE AT V_1 IS $\pm \frac{V_{REF}}{2}$

HOWEVER, ANY ERRORS IN ADC 0 WILL CAUSE $|EQ_0| > \frac{1}{2} V_{LSB}$ AND

0 0 WILL OVERLOAD ADC 1 SINCE $V_1 > \pm \frac{V_{REF}}{2}$

REDUCE G_1

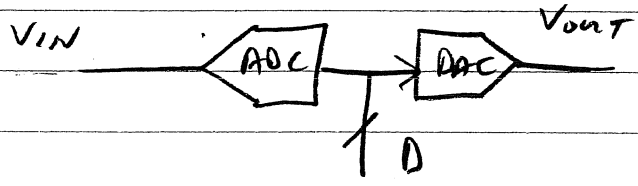
LET $G_1 = 2^{N_0 - 1}$

EX IF $N_0 = 3$ LET $G_1 = 2^2 = 4$

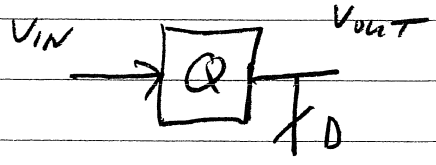
AS A RESULT OVERALL ADC WILL HAVE LARGER QUANTIZATION ERROR (SEE ①) AND OVERALL BIT ACCURACY OF N_{TOTAL}

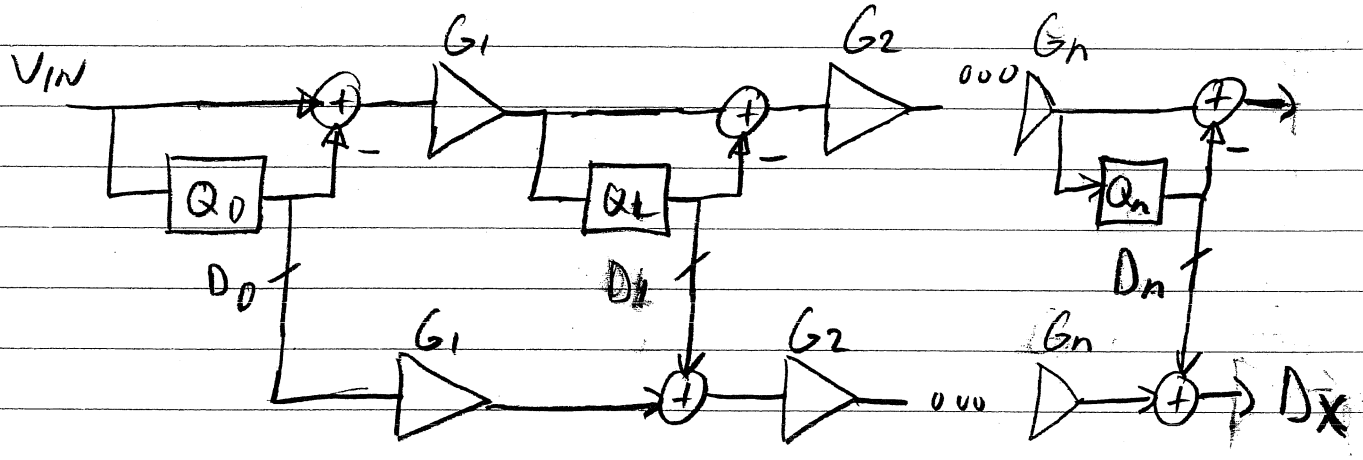
IN GENERAL

LET



SHOWN AS





$$D_{OUT} = \left(\prod_{i=1}^{n} G_i \right)^{-1} D_X$$

$$= \left(\frac{1}{V_{REF}} \right) V_{IN} + \left(\prod_{i=1}^{n} G_i \right)^{-1} \frac{EQ_n}{V_{REF}}$$

EXAMPLE

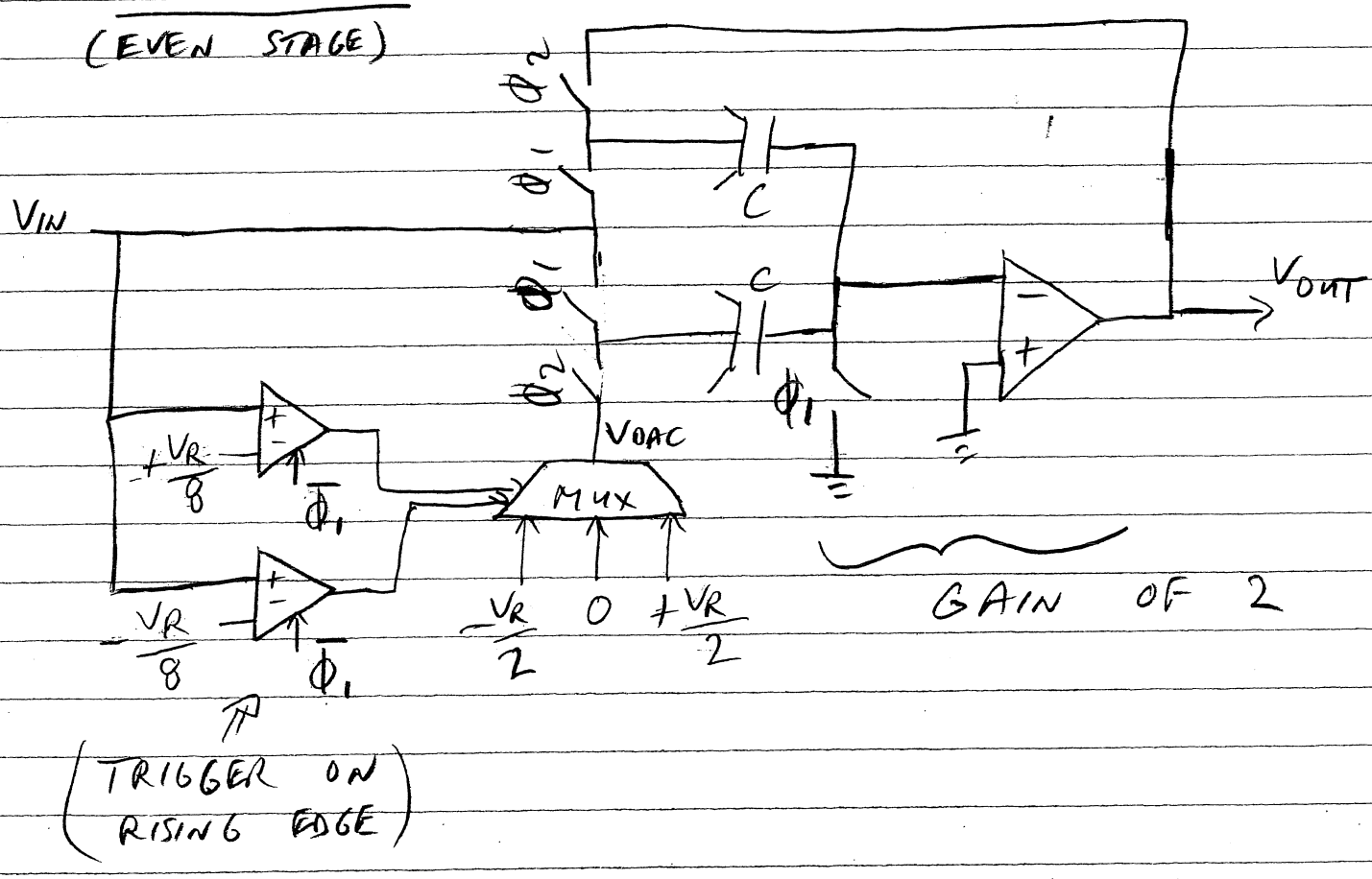
COMMON APPROACH IS 1.5 BITS/STAGE

AND $G_i = 2$ FOR EACH STAGE

ASSUME FULL SCALE INPUT IS $\pm \frac{V_R}{2}$

ONE STAGE

(EVEN STAGE)

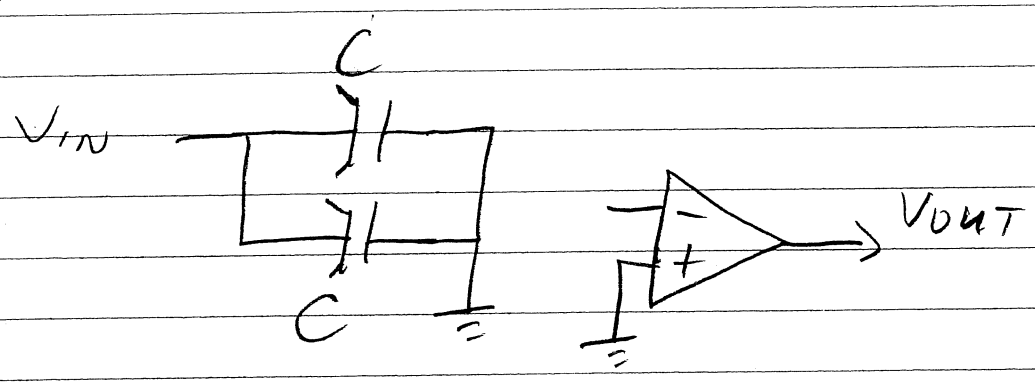


ODD STAGES ARE SAME <u>BUT</u> SAMPLED ON OPPOSITE PHASES

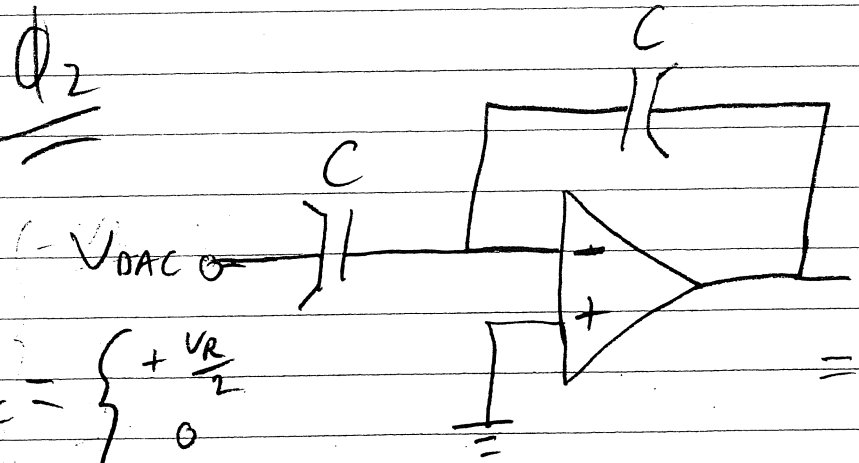
SO DELAY IN 10 BIT PIPELINED ADC WITH 1.5 BITS/STAGES IS ONLY 5 CLOCK CYCLES.

ALSO OPAMP CAN BE POWERED DOWN DURING ϕ_1 TO SAVE POWER

ϕ_1



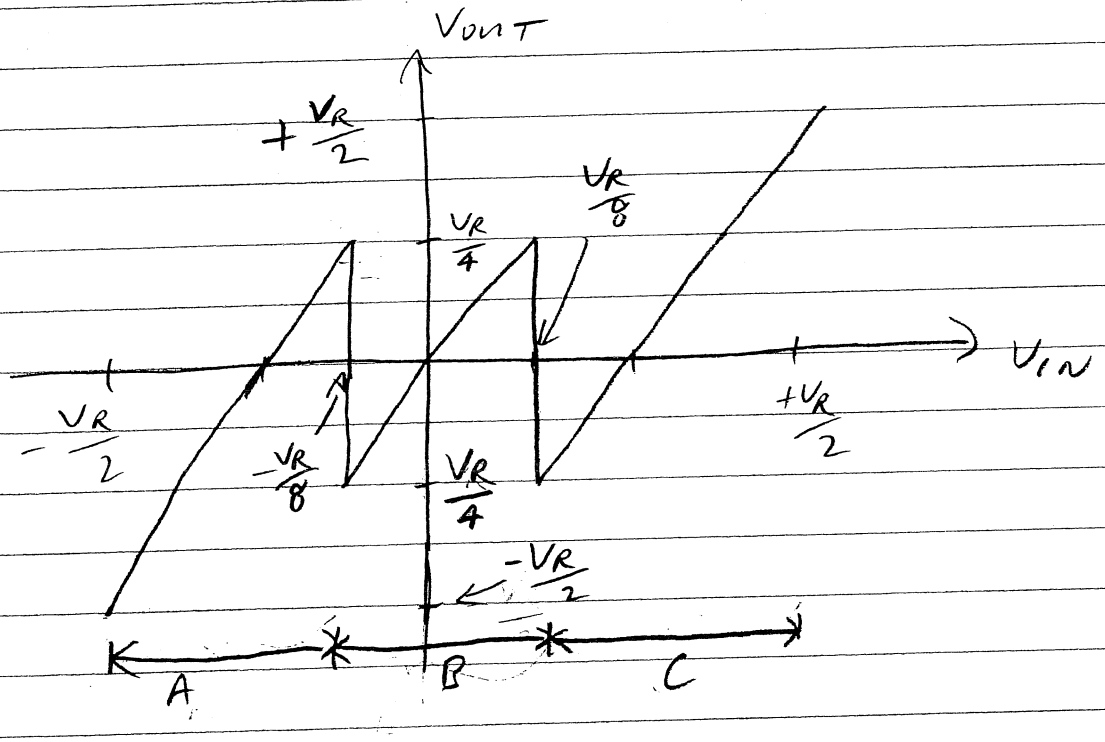
ϕ_2



$$V_{DAC} = \begin{cases} +\frac{V_R}{2} \\ 0 \\ -\frac{V_R}{2} \end{cases}$$

$$= 2V_{IN} - V_{DAC}$$

V_{IN} vs V_{OUT}



A => $V_{OUT} = 2V_{IN} + \frac{V_R}{2}$

B => $V_{OUT} = 2V_{IN}$

C => $V_{OUT} = 2V_{IN} - \frac{V_R}{2}$