MULTI-STAGE CONVERTERS

RECALL

\[ V_{IN} = V_{REF} \cdot D_{OUT} - E_Q \]

\[-\frac{1}{2} V_{LSB} \leq E_Q \leq \frac{1}{2} V_{LSB} = \frac{1}{2} \frac{V_{REF}}{2^N} \]

\[ V_{OUT} = V_{REF} \cdot D_{IN} \]

\[ S \]

\[ V_{IN} \rightarrow A\text{DC} \rightarrow D_{OUT} \rightarrow D\text{AC} \rightarrow V_{OUT} \]
\[ V_{in} = V_{ref0} D_0 - E_Q \]

\[ D_0 = \frac{V_{in}}{V_{ref0}} + \frac{E_Q}{V_{ref0}} \]

\[ V_{out} = V_{ref1} D_0 \]

\[ V_{out} = V_{in} \left( \frac{V_{ref1}}{V_{ref0}} \right) + E_Q \left( \frac{V_{ref1}}{V_{ref0}} \right) \]

If \( V_{ref1} = V_{ref0} = V_{ref} \) \[ \text{FROM NOW ON} \]

\[ \text{ALL ADCS AND DACS USE} \]

\[ \text{"VREF"} \]

So,

\[ \frac{V_{in} + E_Q}{V_{ref}} \]

\[ D_0 = \frac{V_{in} + E_Q}{V_{ref}} \]
MULTI-STAGE CONVERTER

(2 STAGE)

\[ D_0 = \frac{V_{IN} + EQD}{V_{REF}} \]

\[ D_1 = \frac{-G_1 \cdot EQD + EQL}{V_{REF}} \]

\[ D_{OUT} = D_0 + \frac{1}{G_1} D_1 \]

\[ = \left(\frac{1}{V_{REF}}\right) V_{IN} + \frac{1}{G_1} \frac{EQL}{V_{REF}} \quad (1) \]

FINAL QUANTIZATION ERROR IS \( \frac{EQL}{G_1 V_{REF}} \)

SO "G_1" TIMES SMALLER THAN \( \frac{EQL}{V_{REF}} \)

\[ N_{TOTAL} = N_1 + \log_2(G_1) \]

OVERALL CONVERTER BITS.
TO ALLOW FOR MORE TOLERANCE ON ADC CONVERTERS USE OVERLAP CORRECTION

IF NO ADC IDEAL THEN

\[ G_1 = 2 \text{ }^\text{no} \text{ so that full scale value at } V_1 \text{ is } \pm \frac{V_{\text{Ref}}}{2} \]

HOWEVER, ANY ERRORS IN ADC 0 WILL CAUSE \(|E_{\text{eq}}| > \frac{1}{2}V_{\text{LSB}}\) AND 0° WILL OVERLOAD ADC 1 since \(V_1 > \pm \frac{V_{\text{Ref}}}{2}\)

REDUCE \(G_1\)

LET \(G_1 = 2^{\text{no}-1}\)

EX IF \(\text{no} = 3\) LET \(G_1 = 2^2 = 4\)

AS A RESULT OVERALL ADC WILL HAVE LARGER QUANTIZATION ERROR (SEE 1) AND OVERALL BIT ACCURACY OF \(N_{\text{TOTAL}}\)
In General

Let

Shown as

\[ D_{out} = \left( \prod_{i=1}^{n} G_i \right)^{-1} D_X \]

\[ = \left( \frac{1}{V_{REF}} \right) V_{IN} + \left( \prod_{i=1}^{n} G_i \right)^{-1} \frac{FQ_n}{V_{REF}} \]
EXAMPLE

COMMON APPROACH IS 1.5 BITS/STAGE

AND $G_i = 2$ FOR EACH STAGE

ASSUME FULL SCALE INPUT IS $\pm \frac{V_R}{2}$

ONE STAGE
(EVEN STAGE)

VIN

\[ \frac{V_R}{8} \]

\[ \frac{V_R}{2} \]

\[ 0 + \frac{V_R}{2} \]

GAIN OF 2

(Trigger on rising edge)

Odd stages are same but sampled on opposite phases
50 delay in 10 bit pipelined ADC with 1.5 bits/stages is only 5 clock cycles.

Also opamp can be powered down during $\phi_1$ to save power.

$\phi_1$

\[ V_{in} \]

\[ \frac{C}{2} \]

\[ V_{out} \]

$\phi_2$

\[ V_{DAC} \]

\[ \frac{C}{2} \]

\[ V_{out} = 2V_{in} - V_{DAC} \]
$V_{IN}$  $V_S$  $V_{OUT}$

$A \Rightarrow V_{OUT} = 2V_{IN} + \frac{V_R}{2}$

$B \Rightarrow V_{OUT} = 2V_{IN}$

$C \Rightarrow V_{OUT} = 2V_{IN} - \frac{V_R}{2}$