University of Toronto

Final

Date - April 12, 2007

Duration: 2.0 Hr.

ECE1371S — Advanced Analog Circuit Design
Lecturer - D.A. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. 1 aid sheet allowed.

2. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: ______________________

First Name: ______________________

Student #: ______________________

(max grade = 30)

[6] Question 1: Circle T (for True) and F (for False) in statements below.

IMPORTANT NOTE: For each question, a correct answer gets "1", a wrong answer gets "-1", no answer (no circle) gets "0". (A negative mark is possible for this question if you circle more wrong answers than correct answers - do not guess).

T F If a spectrum analyzer measures random circuit noise in the vicinity of 100MHz to be 10 mV (rms) when using a resolution bandwidth of 1MHz, then if the resolution bandwidth is changed to 10kHz, the new measurement around 100MHz would be 0.1 mV(rms).

T F When realizing a folded cascode opamp, an n-channel differential input stage results in a higher loop unity gain frequency over using a p-channel differential input stage.

T F Typically, multi-stage noise shaping delta-sigma converters (using multiple quantizers) are more sensitive to finite opamp gain than single-stage delta-sigma converters.

T F The main benefit of digital error correction in two-step A/D converters is to reduce the accuracy requirements of the first stage D/A converter.

T F One can measure the third-order intercept point by applying a large enough input signal such that the third-order distortion term is equal in power to the power of the fundamental.

T F Typically, when a transistor is in the triode region, beta mismatch effects dominate over Vt mismatch effects.

[6] Question 2: Given a quantizer can be modelled by the equation

$$v = ky + e$$

where v is the quantizer output, y is the quantizer input, e is the quantization noise and k is the quantizer gain, derive the result

$$k = \frac{E[|y|]}{E[y^2]}$$

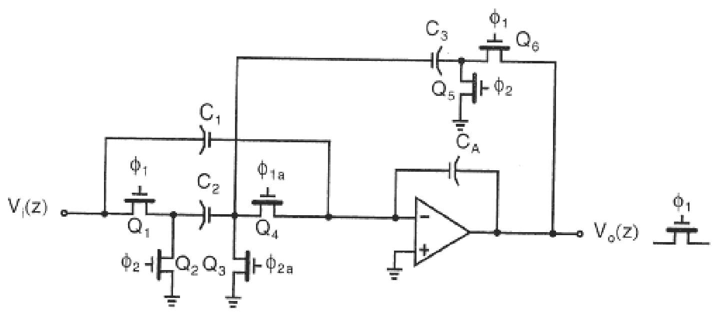
for a 2 level quantizer.

[6] Question 3:

a) Using differential Gm transconductors driving differential capacitances (and ignoring common-mode feedback circuits), design a first-order cont-time delta-sigma ADC based on switched-capacitor/resistor equivalence assuming the 2-level quantizer is clocked at 10MHz. Choose an integrating capacitor of size 10pF, feedback levels of +/-1V differential and for the discrete-time prototype ADC, STF = z^{-1} and NTF = $1 - z^{-1}$. Assume k=1 for the quantizer. Show the cont-time block diagram as well as the Gm sizes.

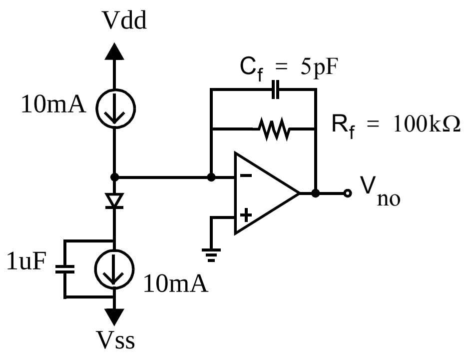
b) Repeat a) but use the exact cont-time ADC derivation with the discrete-time ADC as the prototype.

[6] Question 4: For the circuit below and assuming an ideal opamp, estimate the output dc offset due to channel-charge injection (ignore overlap charge injection) when $C_1 = 0$, $C_2 = C_A = 10C_3 = 10\text{pF}$. Assume that switches Q3 and Q4 are nmos devices with $V_{tn} = 0.8V$, width of 30um, length of 0.8um, $C_{ox} = 1.9e-3\text{pF/u}m^2$ and power supplies of +/-2.5V.



[6] Question 5:

a) Find the total output noise for the circuit shown below where the opamp and current sources are ideal and noiseless but the diode and resistors have thermal noise. Assume the temperature is 300 degrees Kelvin.



b) How much larger or smaller (in dB) is the output noise found in a) compared to kT/C noise that would be found on a 5pF capacitor.