Mosfet Large Signal Modelling

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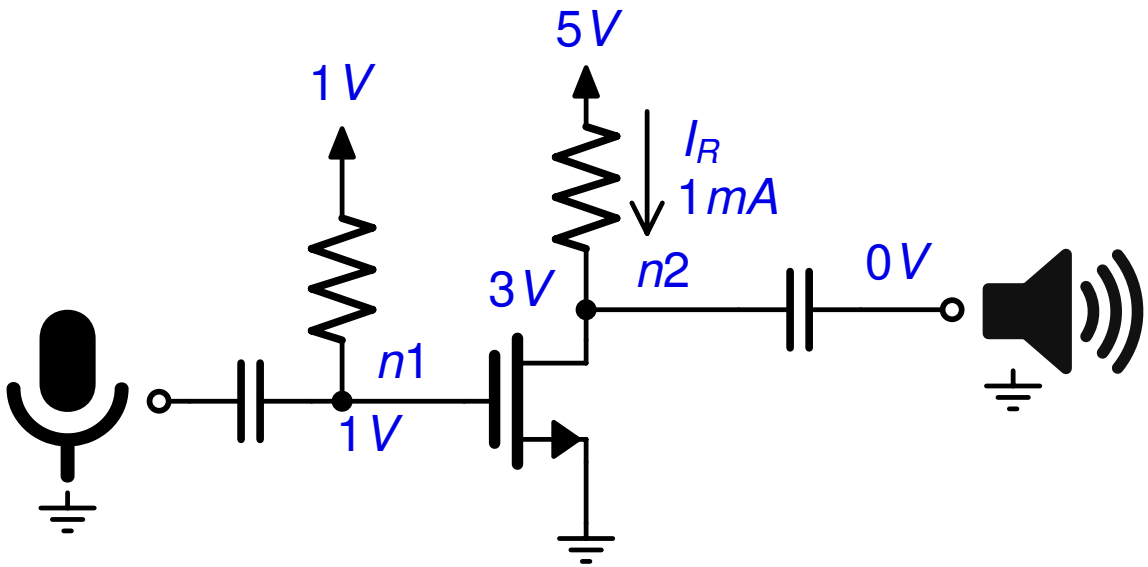
Large/Small Signal Analysis

- Large Signal Analysis
  - Used when voltage/current changes are large such that non-linear behavior of the transistor must be taken into accounted
  - Large signal analysis mainly used for finding the bias conditions of a circuit
- DC Operating Point
  - Set of voltage/current values for a circuit when all input signals set to a dc value.
  - Example: if circuit is a microphone amp, dc bias conditions for that amp is set of voltage/current values for amp when there is no audio signal on the microphone.
- Small Signal Analysis
  - Ignore non-linear behavior and look at variations in the voltage/current values from their bias values
  - Example: looking at how a microphone responds to a small audio signal input.

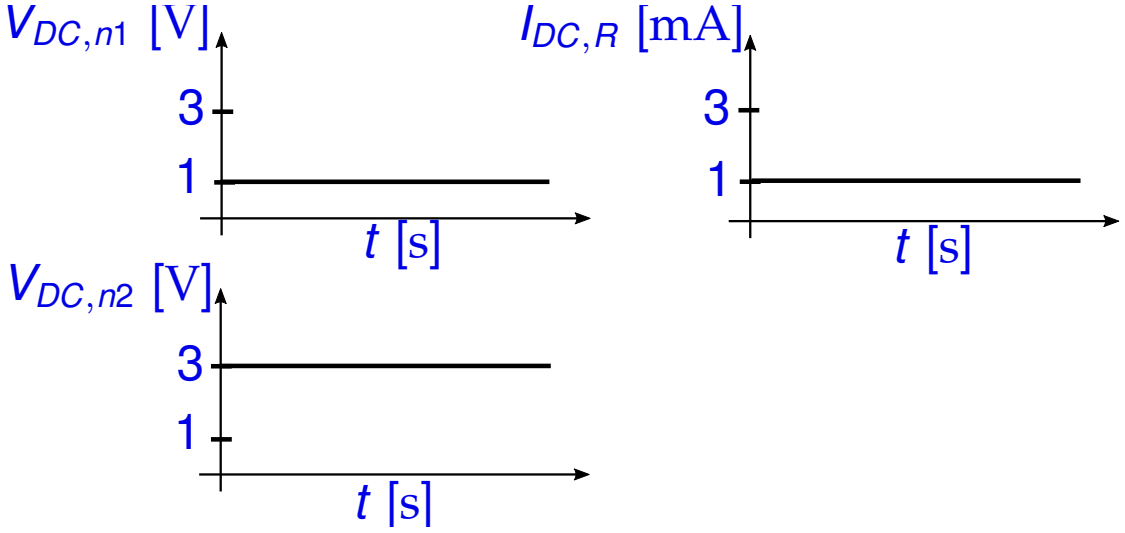
Large/Small Signal Analysis

- One transistor amp

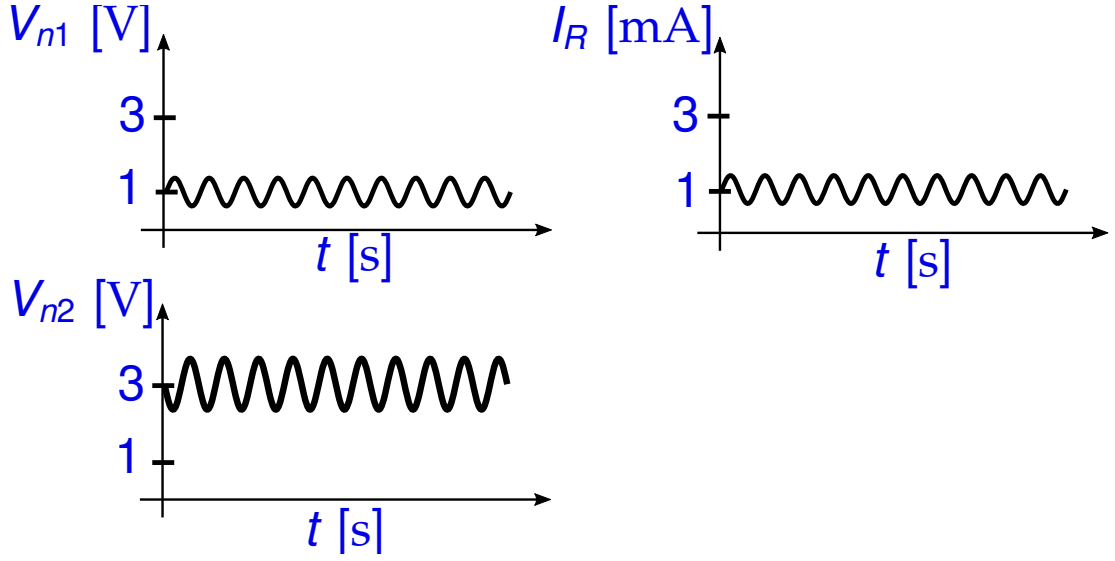


Large/Small Signal Analysis

- DC bias voltage (no signal on Mic)

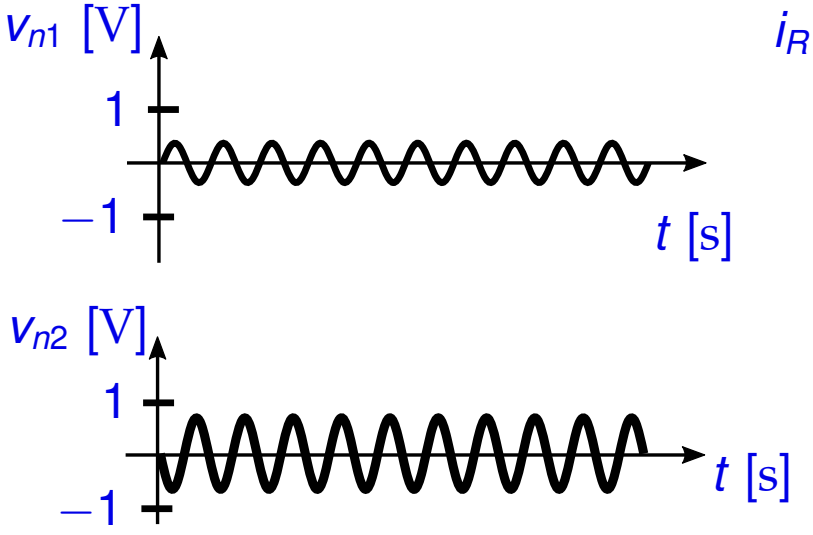


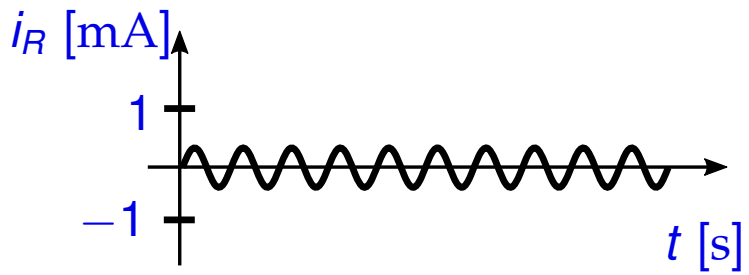
- With a sinusoidal signal on Mic



Large/Small Signal Analysis

- Small signal voltage





- $v_{n1} = V_{n1} - V_{DC,n1}$
- In general: $v = V - V_{DC}$
- The small-signal voltage is the difference between the actual signal, V, and the dc bias voltage, V_{DC}

Notation: Large/Small Signal

- DC value: Capital letter subscript capital letters
  - Example: V_{B2}
- small signal value: small letter subscript small letters
  - Example: v_{B2}
- total signal value: small letter subscript capital letters
  - Example: v_{b2}
- Total = DC value + small-signal
  - Example: $v_{B2} = V_{B2} + v_{b2}$

Large/Small Signal Analysis

- A sinusoid is shown here but it could be a dc small-signal voltage.
- In the example above for $V_{DC,n1} = 1\text{V}$, $V_{DC,n1} = 3\text{V}$
  - if a dc input signal of 0.1V is added to node $n1$
  - new voltage on $n1$ is $V_{n1} = 1.1\text{V}$
  - small-signal voltage on node $n1$ is $v = 0.1\text{V}$
  - If gain of amp is -4V/V, then new voltage on $n2$ is $V_{n1} = 2.6\text{V}$
  - small-signal voltage on node $n2$ is $v = -0.4\text{V}$
- So small-signal analysis is valid for dc to high frequency signals.

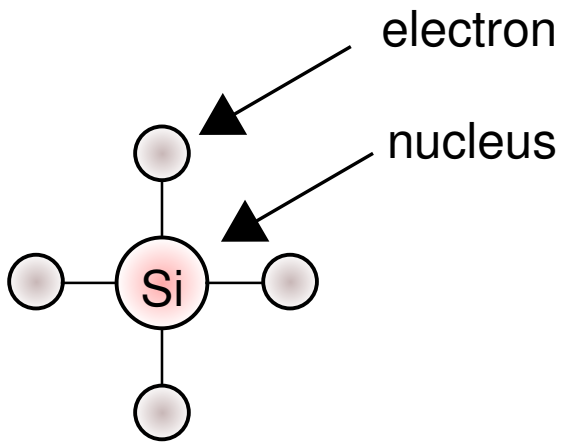
- These slides will cover **Large Signal Analysis** for Mosfet transistors (including dc bias analysis)

Semiconductor Materials

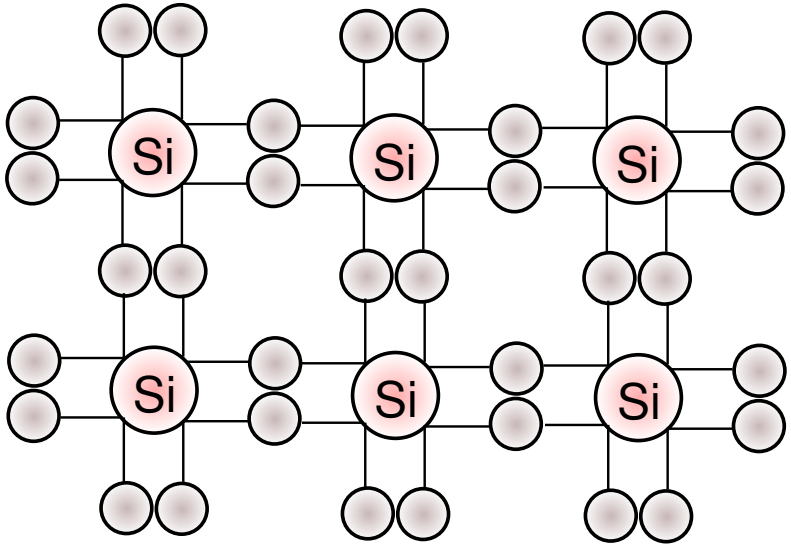
- Valence band
  - Outermost electron shell
  - Can be around atom or molecule
- Conductor
  - Loosly held electrons in valence band
    typically 1,2 or 3 electrons in valence band
  - Examples: Copper, Gold, Silver, Aluminum
- Insulator
  - Strongly held electrons in valence band
    typically 8 electrons in valence band
  - Example: SiO2
    8 electrons in valence band of molecule
- Semiconductor
  - typically 4 electrons in valence band
  - Examples: Silicon, Carbon

Semiconductor Materials

- Silicon Atom



- Silicon crystal

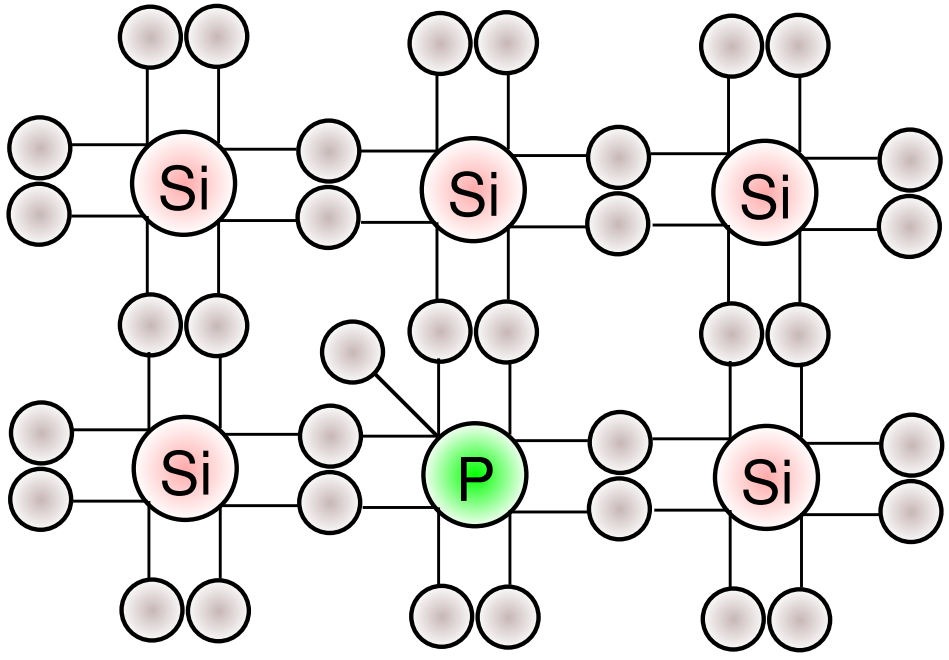


Semiconductor Materials

- Silicon crystal
  - Above is shown as 2-D when in reality, it is a 3-D lattice structure
  - Each Si atom is bonded with 4 other Si atoms and they share electrons so it appears as each Si atom has 8 valence electrons
  - Pure silicon is called Instrinsic Silicon
- Silicon Crystal at absolute zero temp
  - No free electrons, so Si crystal is an insulator at absolute zero
- Silicon Crystal at above absolute zero temp
  - Some electrons leave their bond and travel around lattice
  - This results in a free electron and a hole where the electon left
  - These are called minority carriers (we will see that majority carriers are due to doping)

Semiconductor Materials

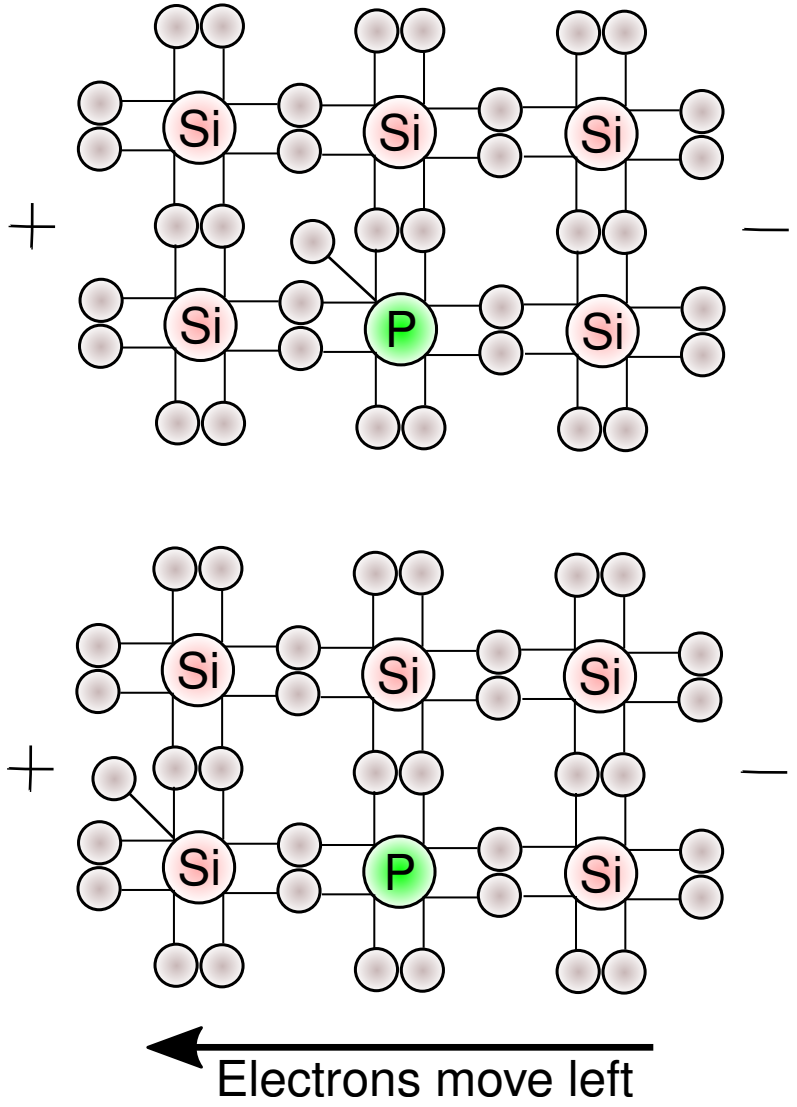
- N-type Silicon



  - Add a bit of Phosphorus (which has 5 electrons in its valence shell)
  - The charge remains neutral as the nucleus has 1 more proton that cancels the extra electron charge
  - This extra electron can break free and roam the lattice leaving a fixed positive charge

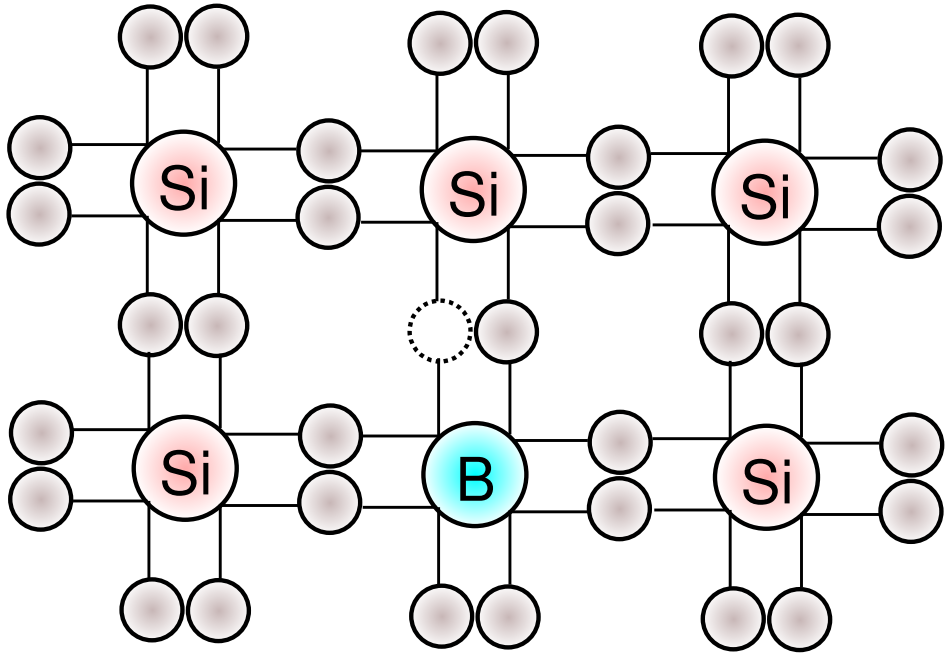
Semiconductor Materials

- N-type Silicon in an electric field



Semiconductor Materials

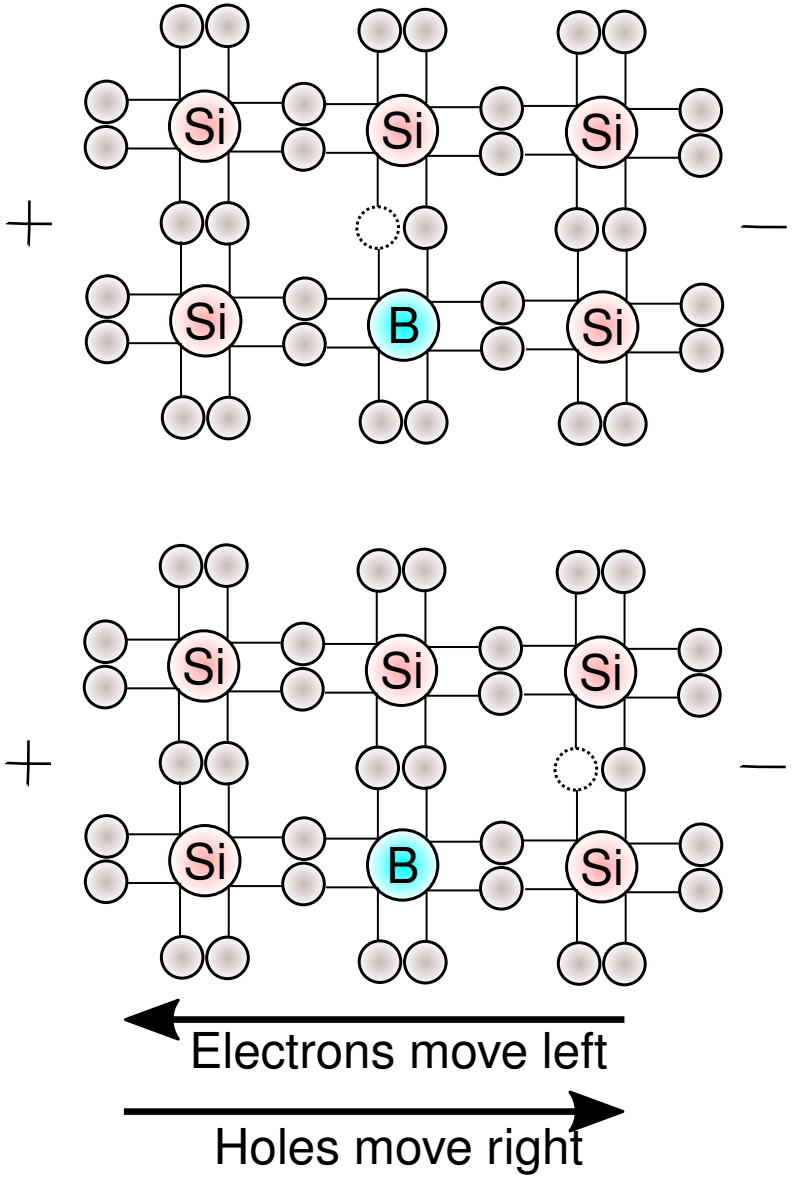
- P-type Silicon



  - Add a bit of Boron (which has 3 electrons in its valence shell)
  - The charge remains neutral as the nucleus has 1 less proton that cancels the lost electron charge
  - This ”hole” can move around the lattice

Semiconductor Materials

- P-type Silicon in an electric field



Semiconductor Materials

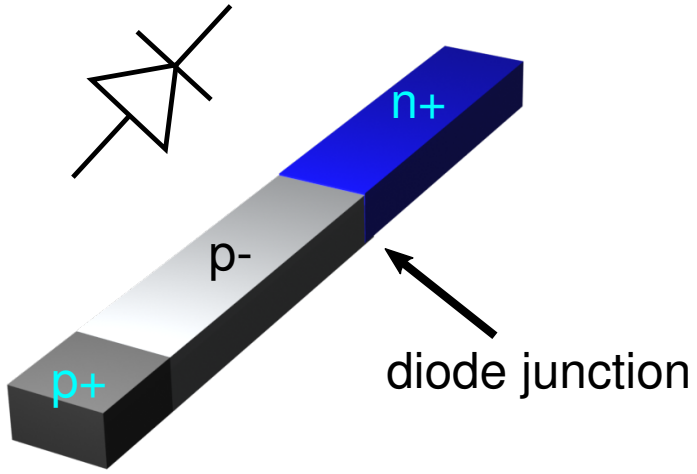
- N-type Silicon
  - Majority carriers are electrons (due to doping)
  - Minority carriers are holes (due to thermal energy)
- P-type Silicon
  - Majority carriers are holes (due to doping)
  - Minority carriers are electrons (due to thermal energy)

Diode (pn junction)

- Made by putting p-type silicon together with n-type silicon
- n+/p+: strongly doped
- n-/p-: lightly doped
- pn-junction discovered in 1939
- metal/crystal junctions discovered in 1874

- Current flows from p to n type if more than about 0.7V applied
- Current is blocked from flowing if less than about 0.7V applied

Diode (pn junction)



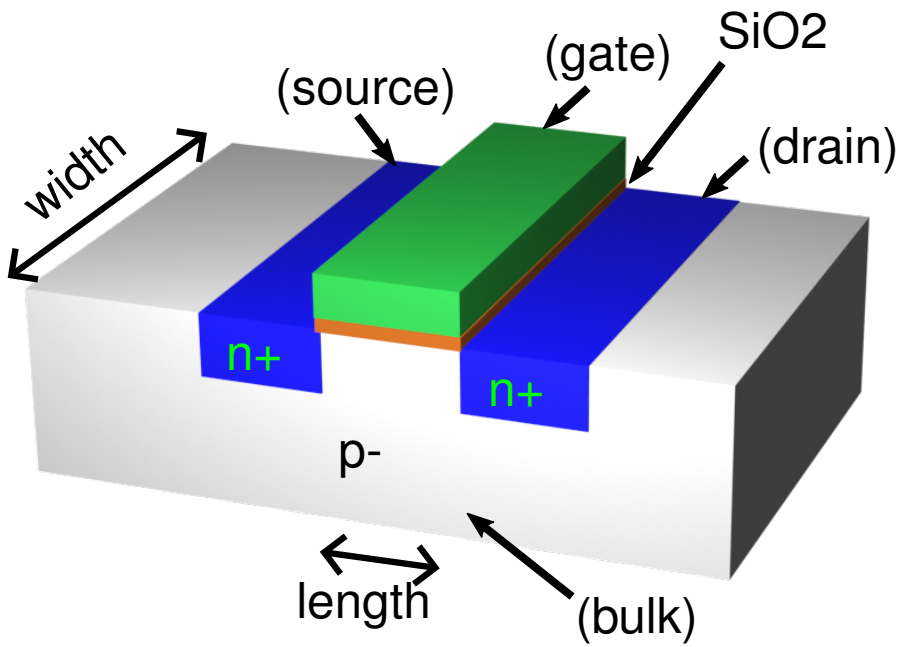
- p+ region needed for ohmic contact to p-
- metal/p- is a schottky diode
- If light shines on a reversed biased pn junction, reverse bias current increases with light intensity.

Mosfet Transistors

- Mosfet Transistor
  - **M**etal-**O**xide-**S**emiconductor-**F**ield-**E**ffect-**T**ransistor
- Bipolar transistor invented in 1948
- Mosfet transistor first working in 1959
  - First patent for a Mosfet transistor in 1925
  - Bell labs patents for Mosfet rejected in 1940s due to the 1925 patent
  - In 1959, breakthrough was to use a thin layer of SiO2 used for gate insulator
- MOS transistors became dominant for digital circuits due to almost zero static power dissipation.
  - Static power dissipation is power being dissipated even when logic states do not change.

Mosfet Transistors

- Mosfet transistors are a 4 terminal device
- The 4 terminals are:
  - Drain (D)
  - Gate (G) (metal or polysilicon)
  - Source (S)
  - Bulk (B)
- NMOS shown below

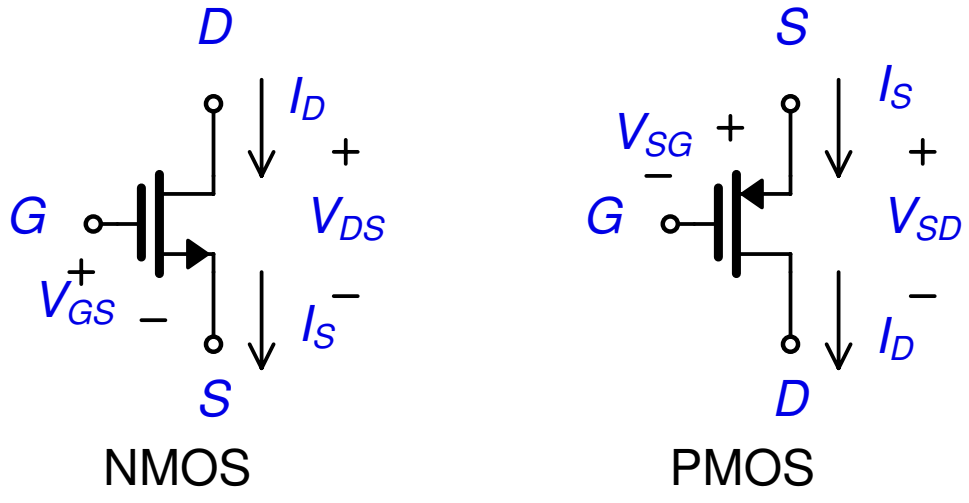


Mosfet Transistors

- For simplicity
  - We will assume the bulk and source are connected together
  - Therefore, we can treat the transistor as a 3 terminal device ... Drain/Gate/Source
  - Later, we will look at when the bulk/source are not connected together
- 2 main types of Mosfet transistor
- NMOS
  - drain/source are n+, bulk is p-
  - turns on when $V_G \geq V_S + V_{tn}$
  - source is drain/source terminal with lower voltage
- PMOS
  - drain/source are p+, bulk is n-
  - turns on when $V_G \leq V_S - |V_{tp}|$
  - source is drain/source terminal with higher voltage

Mosfet Transistors

- Mosfet symbols



- NMOS
  - Drain shown at top of symbol so that drain current, I_D flows from top to bottom
  - I_D flows into drain and out of source
- PMOS
  - Drain at bottom of symbol; I_D flows from top to bottom; I_D flows out of drain

Mosfet Transistors

- For both NMOS and PMOS
  - The gate current, I_G is essentially zero

$$I_G = 0 \tag{1}$$

  - Since the gate current equals zero, the source current equals the drain current

$$I_D = I_S \tag{2}$$

Mosfet Parameters

- Threshold voltage
  - NMOS: $V_{tn} > 0$
  - PMOS: $V_{tp} < 0$
  - Units: $[V]$
- Mobility
  - electron: μ_n ; hole: μ_p
  - determines speed of carrier for given potential field
  - Units: $[m^2/(Vs)]$
- Gate capacitance per unit area
  - C_{ox}
  - typically the same for NMOS and PMOS
  - Units: $[F/m^2]$
- Often mobility and gate capacitance combined as
  - $\mu_n C_{ox}$ or $\mu_p C_{ox}$
  - Units: $[A/V^2]$

Mosfet Parameters

- Width of channel: W
  - Units: $[m]$
- Length of channel: L
  - Units: $[m]$
- Often W/L is used which is unitless
- Channel length modulation parameter
  - NMOS: $\lambda_n > 0$
  - PMOS: $\lambda_p < 0$
  - Units: $[V^{-1}]$
  - In an ideal transistor, $\lambda = 0$

Transistor Overdrive Voltage, V_{ov}

- We define the following overdrive voltages
- For NMOS

$$V_{ov} \equiv V_{GS} - V_{tn} \tag{3}$$

- For PMOS

$$V_{ov} \equiv V_{SG} - |V_{tp}| \tag{4}$$

  - For PMOS, the gate voltage must be lower than the source voltage by $|V_{tp}|$ to turn on the transistor

- V_{ov} indicates how strong the transistor is turned on
  - For $V_{ov} \leq 0$: transistor is off
  - For $V_{ov} > 0$: transistor is on
  - As V_{ov} is increased, the transistor turns on stronger

NMOS Large Signal Model

- There are 3 regions of operations in large signal model
- Each region has a different equation for the current, I_D
- The 3 regions are:
  - Cutoff Region
  - Triode Region
  - Active (or Saturation) Region
- Which region the transistor is in depends on V_{ov} and V_{DS}

NMOS Large Signal Model

- Cutoff Region
  - Condition: $V_{ov} < 0$ (or equivalently $V_{GS} < V_{tn}$)

$$I_D = 0 \tag{5}$$

- Triode Region
  - Condition: $V_{ov} > 0$ and $V_{DS} < V_{ov}$

$$I_D = \mu_n C_{ox}(W/L)(V_{ov} - V_{DS}/2)V_{DS} \tag{6}$$

  - Note that $I_D > 0$ and flows INTO the drain

NMOS Large Signal Model

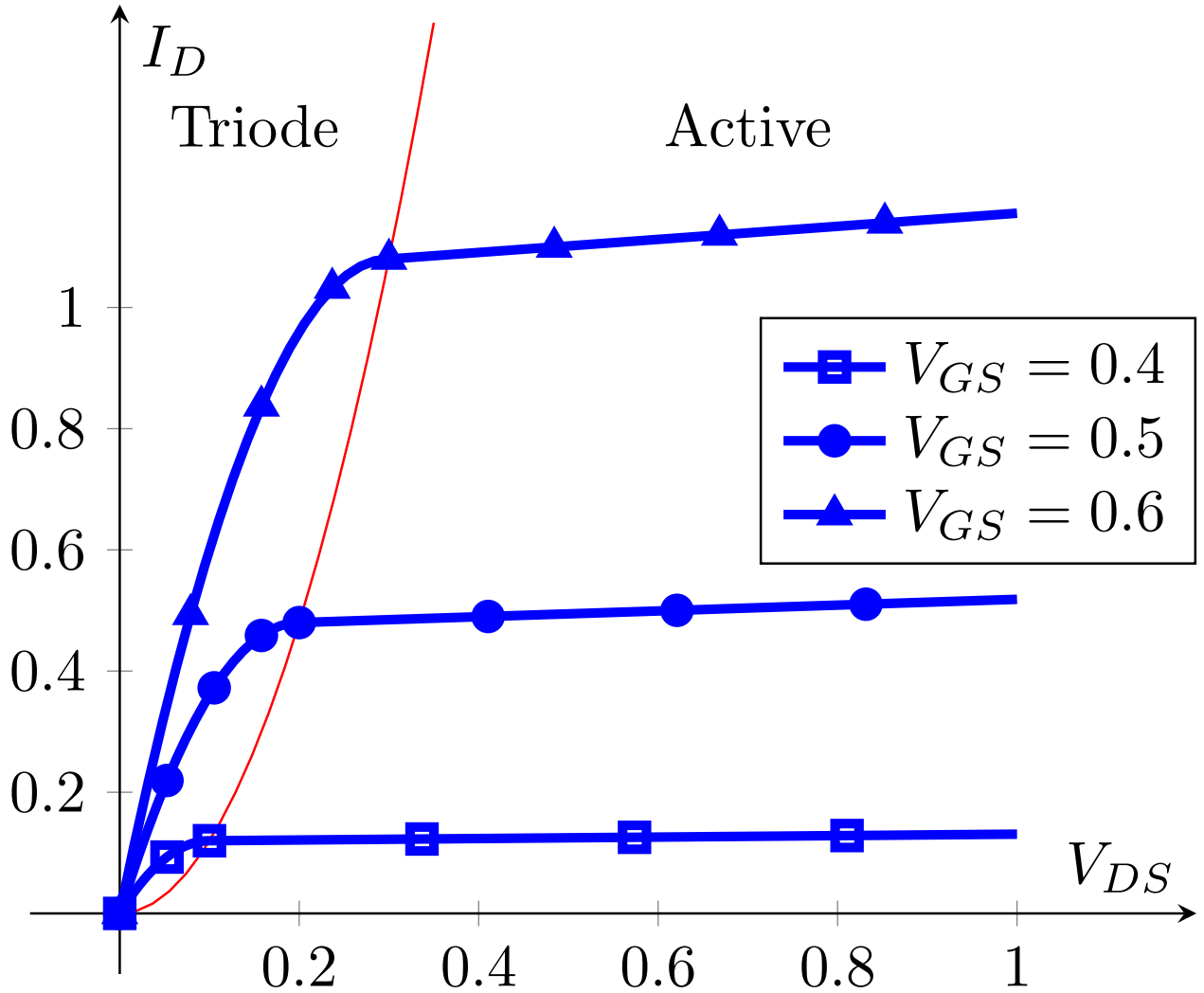
- Active (or Saturation) Region
  - Condition: $V_{ov} > 0$ and $V_{DS} > V_{ov}$

$$I_D = \left(\frac{\mu_n C_{ox}}{2}\right)\left(\frac{W}{L}\right) V_{ov}^2(1 + \lambda_n V'_{DS}) \tag{7}$$

    where $V'_{DS} \equiv V_{DS} - V_{ov}$
  - Note that $I_D > 0$ and flows INTO the drain
- In some textbooks, V_{DS} is used instead of V'_{DS}
  - Using V_{DS} leads to a discontinuity in I_D between the triode and active regions

NMOS I_D vs V_{DS} Plot

- $V_{tn} = 0.3V$; $\mu_n C_{ox} = 240\mu A/V^2$; $W/L = 100$; $\lambda_n = 0.1\,V^{-1}$



PMOS Large Signal Model

- The PMOS large signal equations are similar to those for an NMOS transistor
- Recall

$$V_{ov} \equiv V_{SG} - |V_{tp}| \tag{8}$$

- Cutoff Region
  - Condition: $V_{ov} < 0$ (or equivalently $V_{SG} \leq |V_{tp}|$)

$$I_D = 0 \tag{9}$$

PMOS Large Signal Model

- Triode Region
  - Condition: $V_{ov} > 0$ and $V_{SD} < V_{ov}$

$$I_D = \mu_p C_{ox}(W/L)(V_{ov} - V_{SD}/2)V_{SD} \tag{10}$$

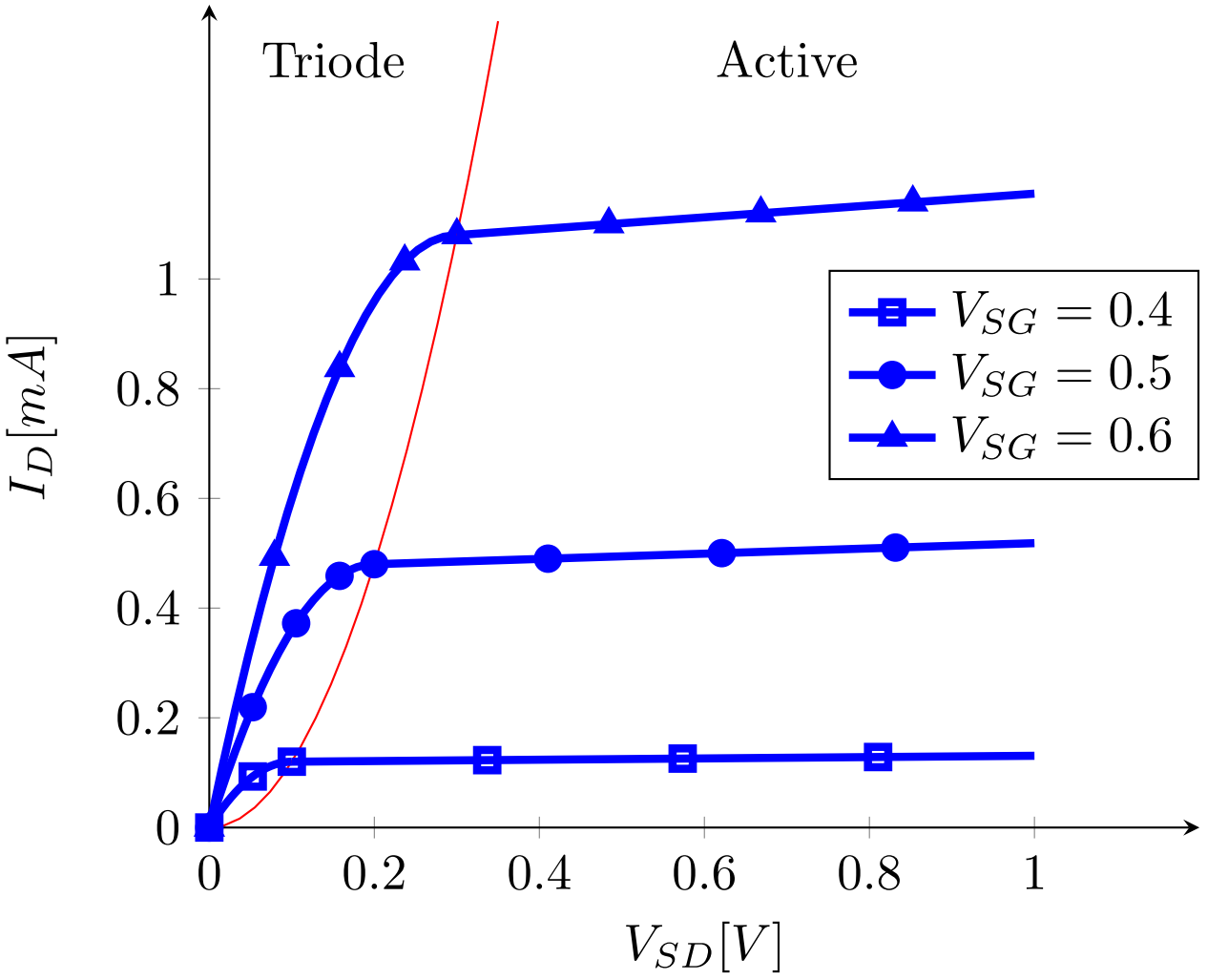
  - Note that $I_D > 0$ and flows OUT OF the drain
- Active (or Saturation) Region
  - Condition: $V_{ov} > 0$ and $V_{SD} > V_{ov}$

$$I_D = \left(\frac{\mu_p C_{ox}}{2}\right)\left(\frac{W}{L}\right) V_{ov}^2(1 + |\lambda_p| V'_{SD}) \tag{11}$$

    where $V'_{SD} \equiv V_{SD} - V_{ov}$
  - Note that $I_D > 0$ and flows OUT OF the drain

PMOS I_D vs V_{SD} Plot

- $V_{tp} = -0.3V$; $\mu_p C_{ox} = 240\mu A/V^2$; $W/L = 100$; $\lambda_p = -0.1V^{-1}$



Triode or Active Regions

- NMOS: Active: $V_{DS} \geq V_{ov}$ Triode: $V_{DS} < V_{ov}$
- An alternative (equivalent) condition is ...
  - Active: $V_D \geq V_G - V_{tn}$ Triode: $V_D < V_G - V_{tn}$
  - Proof...

$$V_{DS} \geq V_{ov}$$
$$V_D - V_S \geq V_G - V_S - V_{tn}$$
$$V_D \geq V_G - V_{tn}$$

- It is sometimes easier to check V_D relative to $V_G - V_{tn}$
- For PMOS
  - Active: $V_D \leq V_G + |V_{tp}|$ Triode: $V_D > V_G + |V_{tp}|$

Finding the DC Operating Point

- Software simulators (like Spice) find the dc operating point very differently than hand analysis
- Software simulators
  - They find roots of non-linear equations that model the transistor over all the operating regions.
  - They find the roots using an iterative approach
- Hand analysis
  - We have different equations depending on what region of operation the transistor is in... but we don't know which region the transistor is in until we do our analysis
  - So we GUESS a region of operation, do our analysis... then check if the answer is consistent with our guess

Finding the DC Operating Point

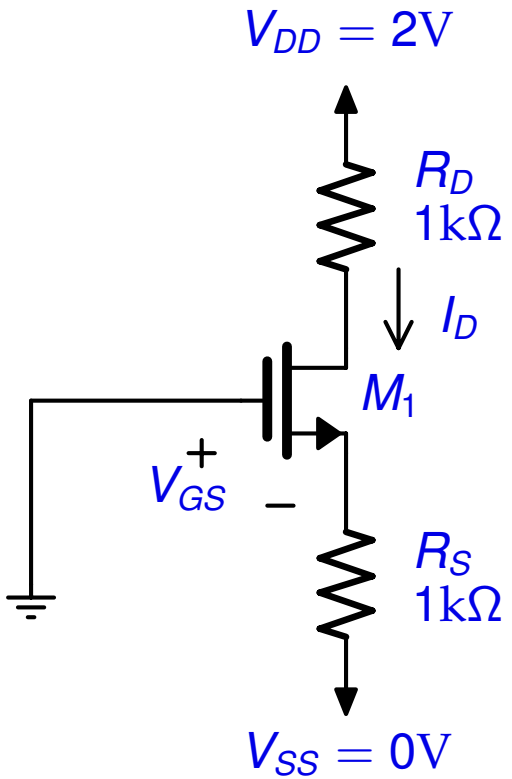
- Hand analysis approach
  1. Guess a set of operating regions for each transistor
  2. Perform hand analysis
  3. Check to see if results agree that the transistors are in the guessed operating regions
  4. If the results do not agree, guess another set of operating regions for each transistor
- Fortunately, for most analog circuits, the operating regions of the transistors are usually in cutoff or active.

Finding the DC Operating Point

- Often set $\lambda = 0$ for finding the DC operating point
  - makes analysis much simpler
  - generally results in a small error in the dc voltages and currents
- Can NOT set $\lambda = 0$ for small-signal analysis
  - would often result in gross errors
  - $\lambda = 0$ implies the drain current is NOT a function of V_{DS} in the active region...
  - so the small-signal output impedance of the transistor would be infinity
- In general, for dc analysis... assume $\lambda = 0$ unless there is a reason not to do so
  - For example, finding the matching accuracy between 2 currents from 2 different transistors.

DC Bias Example 1

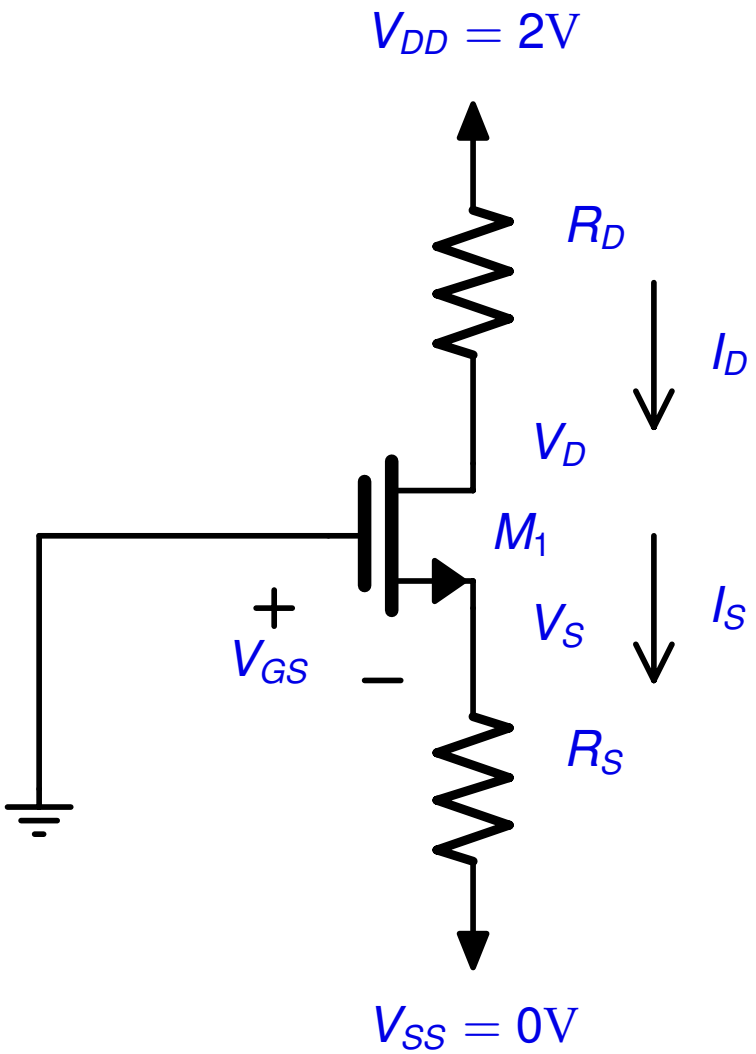
- Find V_S, V_{GS}, V_{DS} and I_D for ...



$V_{tn} = 0.3\text{V}$
$\mu_n C_{ox} = 240\mu\text{A/V}^2$
$W = 10\mu\text{m}$
$L = 0.1\mu\text{m}$
$\lambda_n = 0.1\text{V}^{-1}$

DC Bias Example 1

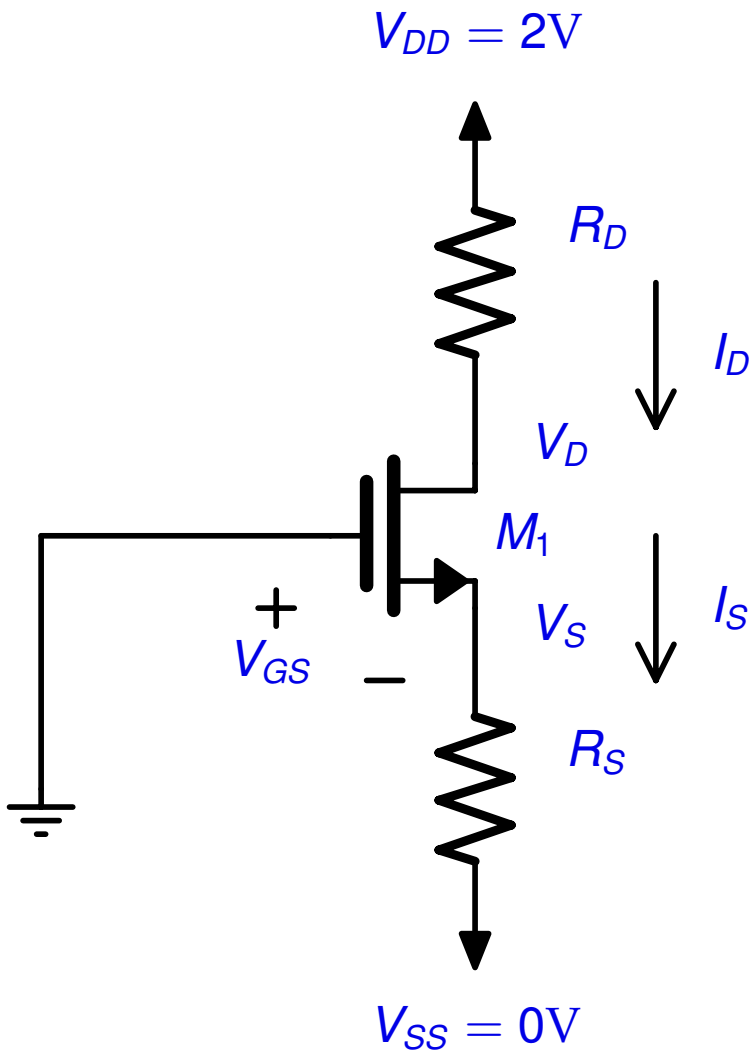
- Assume M_1 is in the active region



- $V_{GS} > V_{tn} = 0.3V$ so $V_S < -0.3V$
- $I_S < (-0.3 - V_{SS})/R_S$ so $I_S < 0$
- $I_D = I_S$ so $I_D < 0$
- but I_D should be greater than zero when in the active region
- **Contradiction**... M_1 is not in the active region

DC Bias Example 1

- Assume M_1 is in the cutoff region



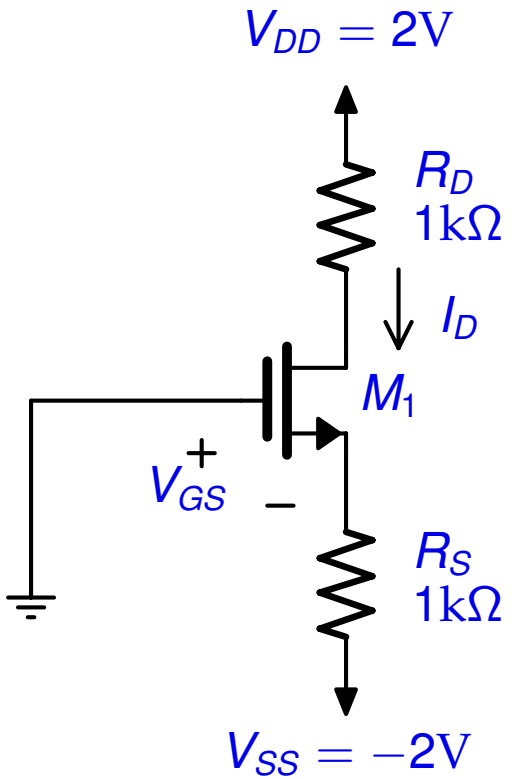
- $I_D = 0$ so $I_S = 0$
- $V_S = V_{SS} + I_S R_S = V_{SS} + 0 = 0$
- $V_{GS} = V_G - V_S = 0 - 0 = 0$
- $V_D = V_{DD} - I_D R_D = V_{DD} - 0 = 2\text{V}$
- $V_{DS} = V_D - V_S = 2 - 0 = 2\text{V}$
- No contradiction, so we have the solution

  $V_S = 0;\ V_{GS} = 0;\ V_{DS} = 2\text{V}$

  $I_D = 0$

DC Bias Example 2

- Find V_S, V_{GS}, V_{DS} and I_D for ...



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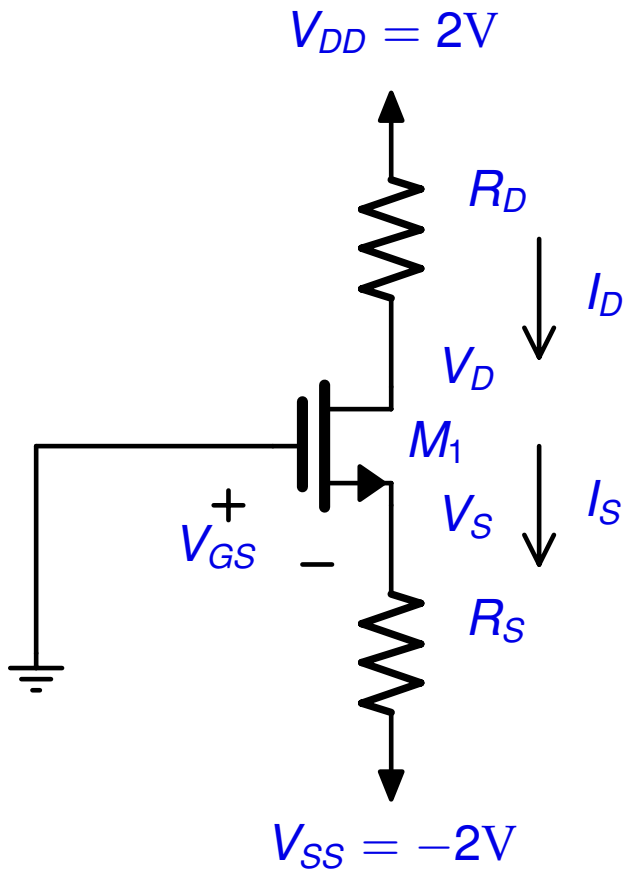
DC Bias Example 2

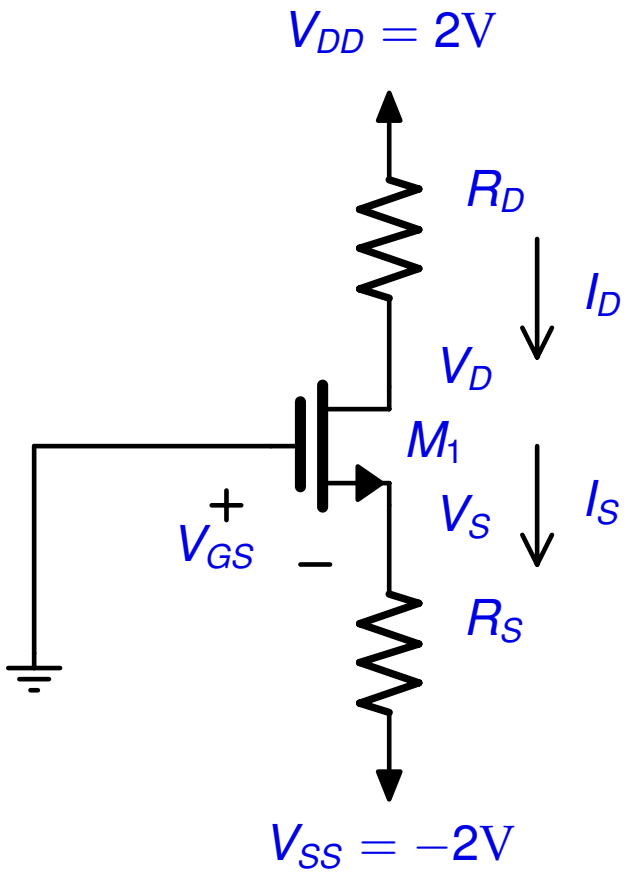
- Assume M_1 is in the cutoff region



- $I_D = 0$ and $I_S = 0$
- $V_S = V_{SS} + I_D R_S = V_{SS} + 0 = -2\text{V}$
- $V_{GS} = V_G - V_S = 0 - (-2) = 2\text{V}$
- $V_{GS} = 2\text{V} > V_{tn} = 0.3\text{V}$
- **Contradiction** since $V_{GS} > V_{tn}$ so M_1 is not in the cutoff region

DC Bias Example 2

- Assume M_1 is in the active region



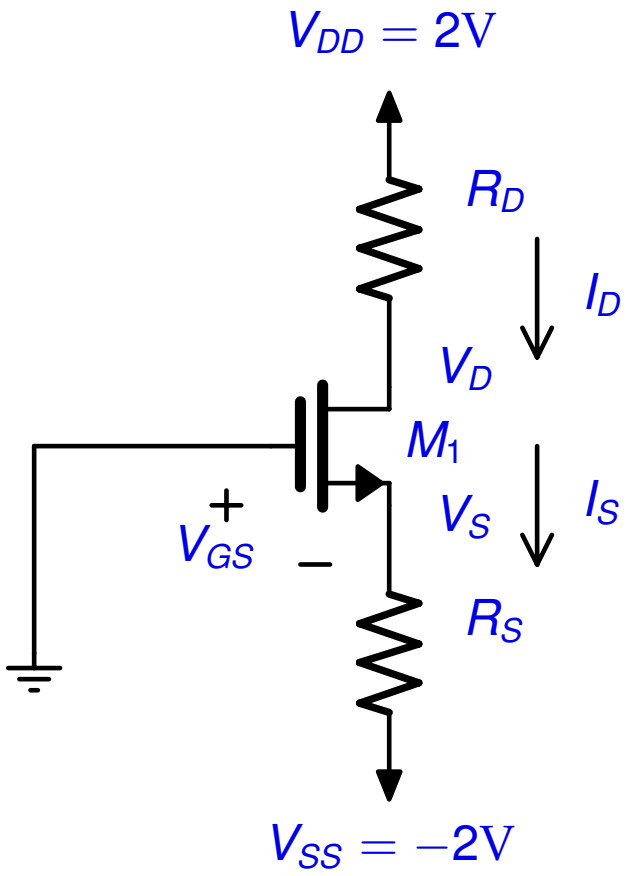
- Let $\lambda_n = 0$ as discussed above
- $I_S = \frac{V_S - V_{SS}}{R_S} = \frac{-(V_{ov}+V_{tn})-V_{SS}}{R_S}$
- $I_S = I_D = 0.5\mu_n C_{ox}(W/L)(V_{ov})^2$
- Putting in numerical values, we have 2 equations for I_S

$$I_S = 0.0017 - 0.001\,V_{ov} \qquad (12)$$

$$I_S = 0.012\,V_{ov}^2 \qquad (13)$$

DC Bias Example 2

- Assume M_1 is in the active region



- Combining the above 2 equations, we have
- $V_{ov}^2 + 0.0833 V_{ov} - 0.1417 = 0$
- The roots are found to be $V_{ov} = 0.337\text{V} \text{ and } -0.4204\text{V}$
- However, we know that $V_{ov} > 0$ so $V_{ov} = 0.337\text{V}$
- $V_{GS} = V_{ov} + V_{tn} = 0.637\text{V}$
- $I_D = I_S = 0.012 V_{ov}^2 = 1.363\text{mA}$

DC Bias Example 2

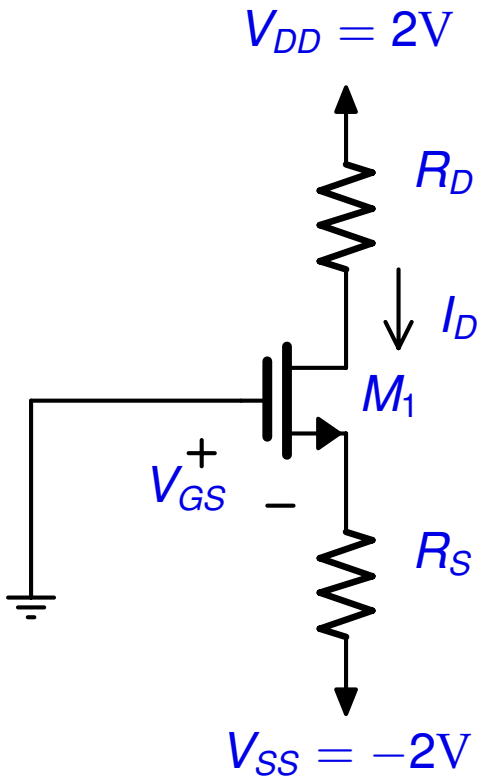
- Finally, we need to find V_D **AND check that** $V_D \geq V_G - V_{tn}$ **to ensure that** M_1 **is in the active region**
- $V_D = V_{DD} - I_D R_D = 0.637\text{V}$
- $V_G - V_{tn} = (0) - (0.3) = -0.3\text{V}$
- Since $V_D > (-0.3)$, and there are no contractions...
  M_1 is in the active region
- We also have $V_S = V_G - V_{GS} = (0) - (0.637) = -0.637\text{V}$
- Solution:

  $V_S = -0.637\text{V};\ V_{GS} = 0.637\text{V}$

  $V_{DS} = 1.274\text{V};\ I_D = 1.363\text{mA}$

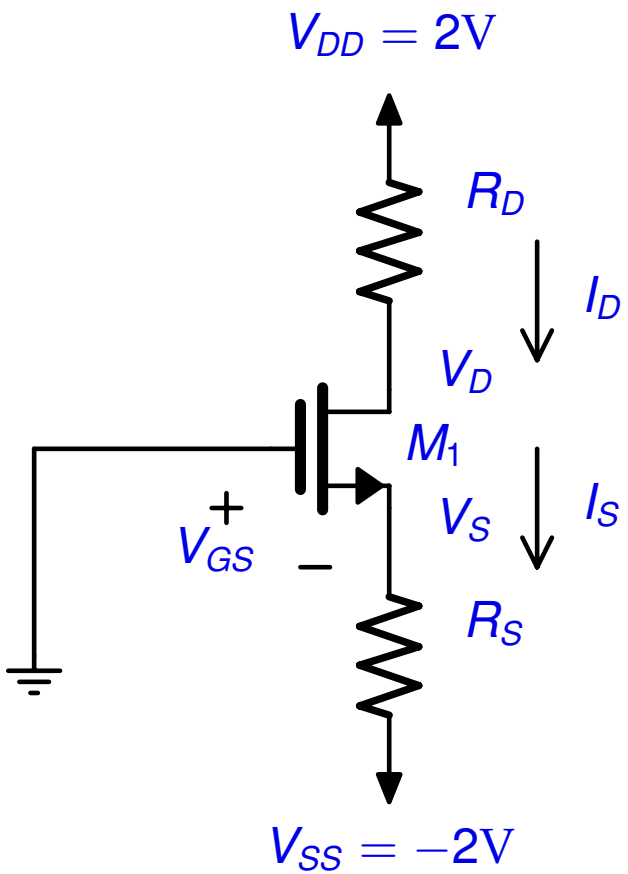
DC Bias Example 3

- For the circuit below, find values for R_D and R_S such that $I_D = 1\text{mA}$ and $V_D = 1\text{V}$



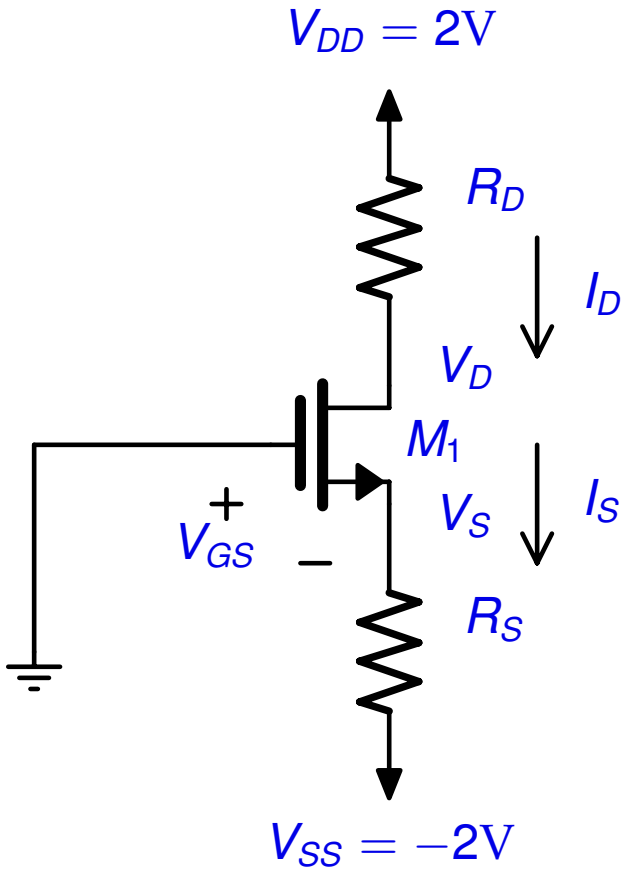
$V_{tn} = 0.3\text{V}$
$\mu_n C_{ox} = 240\mu\text{A/V}^2$
$W = 10\mu\text{m}$
$L = 0.1\mu\text{m}$
$\lambda_n = 0.1\text{V}^{-1}$

DC Bias Example 3



- Since $I_D = 1\text{mA}$ and $V_D = 1\text{V}$, we can find R_D from
- $I_D = (V_{DD} - V_D)/R_D$ leading to
- $R_D = (V_{DD} - V_D)/I_D = 1\text{k}\Omega$
- To find R_S, we guess that M_1 is in the active region and find V_{ov} using the drain current equation...
- $I_D = 0.5\mu C_{ox}(W/L)V_{ov}^2$
- $1\text{mA} = 0.012V_{ov}^2$

DC Bias Example 3



- $V_{ov} = \sqrt{0.001/0.012} = 0.2887\text{V}$
  - we take the positive root since $V_{ov} > 0$
- $V_{GS} = V_{ov} + V_{tn} = 0.5887\text{V}$
- $V_S = V_G - V_{GS} = 0 - 0.5887 = -0.5887\text{V}$
- $R_S = (V_S - V_{SS})/I_D = 1.411\text{k}\Omega$

DC Bias Example 3

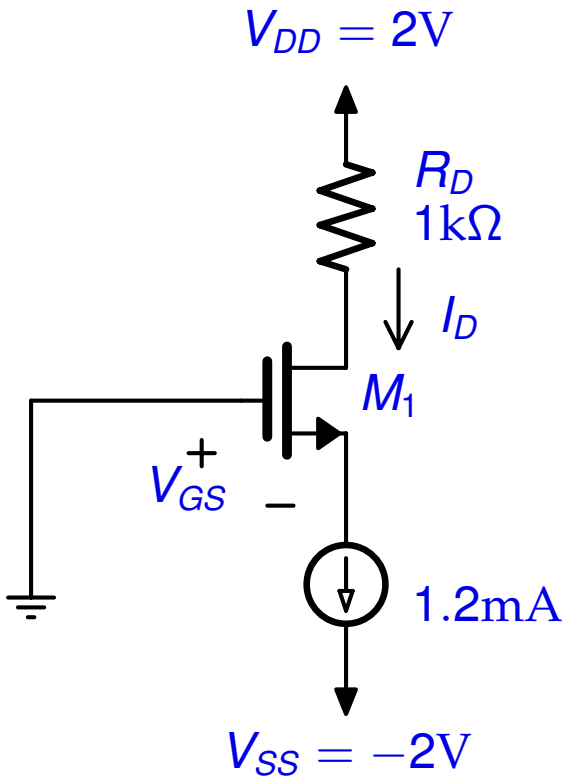
- Finally, we need to find V_D **AND check that** $V_D \geq V_G - V_{tn}$ **to ensure that** M_1 **is in the active region**
- $V_D = 1\text{V}$ (a given parameter)
- $V_G - V_{tn} = -0.3\text{V}$
- Since $V_D > -0.3\text{V}$, and there are no contradictions... M_1 is in the active region
- Solution:

  $R_D = 1\text{k}\Omega;\ R_S = 1.411\text{k}\Omega$

- Note that the solution to this problem did not require solving a quadratic equation.
  - Before we needed to solve for I_D and V_{ov} at the same time while in this problem, I_D was given.

DC Bias Example 4

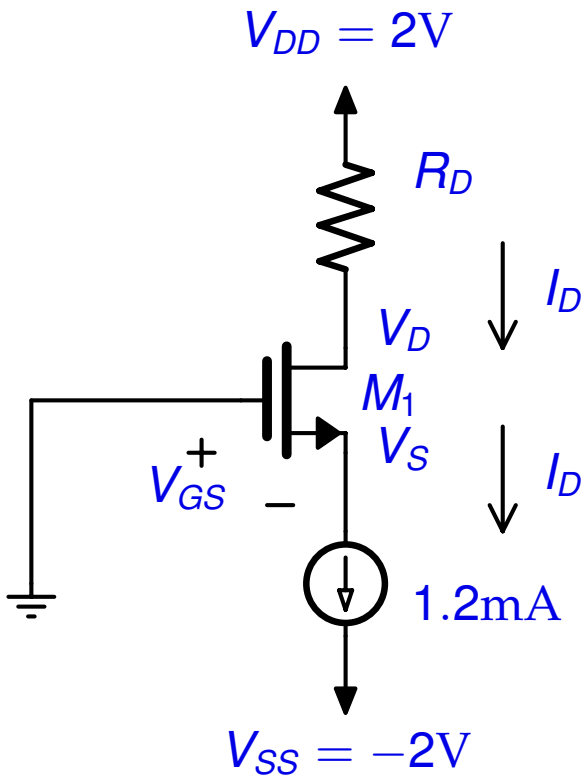
- Find V_S, V_{GS}, V_{DS} and I_D for ...



$V_{tn} = 0.3\text{V}$
$\mu_n C_{ox} = 240\mu\text{A/V}^2$
$W = 10\mu\text{m}$
$L = 0.1\mu\text{m}$
$\lambda_n = 0.1\text{V}^{-1}$

DC Bias Example 4

- Assume M_1 is in the active region



- $I_D = I_S = 1.2\text{mA}$
- $I_D = 0.5\mu_n C_{ox}(W/L)V_{ov}^2$
- $1.2\text{mA} = 0.012V_{ov}^2$
- $V_{ov} = 0.3162\text{V}$
- $V_{GS} = V_{ov} + V_{tn} = 0.6162\text{V}$
- $V_S = V_G - V_{GS} = -0.6162\text{V}$
- $V_D = V_{DD} - I_D R_D = 0.8\text{V}$

DC Bias Example 4

- Finally, we need to find V_{DS} **AND check that** $V_{DS} \geq V_{ov}$ **to ensure that** M_1 **is in the active region**
- $V_{DS} = V_D - V_S = (0.8) - (-0.6162) = 1.416\text{V}$
- Since $V_{DS} > V_{ov}$, and there are no contradictions... M_1 is in the active region
- Solution:

  $V_S = -0.6162\text{V};\ V_{GS} = 0.6162\text{V}$

  $V_{DS} = 1.416\text{V};\ I_D = 1.2\text{mA}$

- Note that using a current source is a common way to set up the dc bias conditions for analog circuits.
  - We will see how to create current sources in a future section.

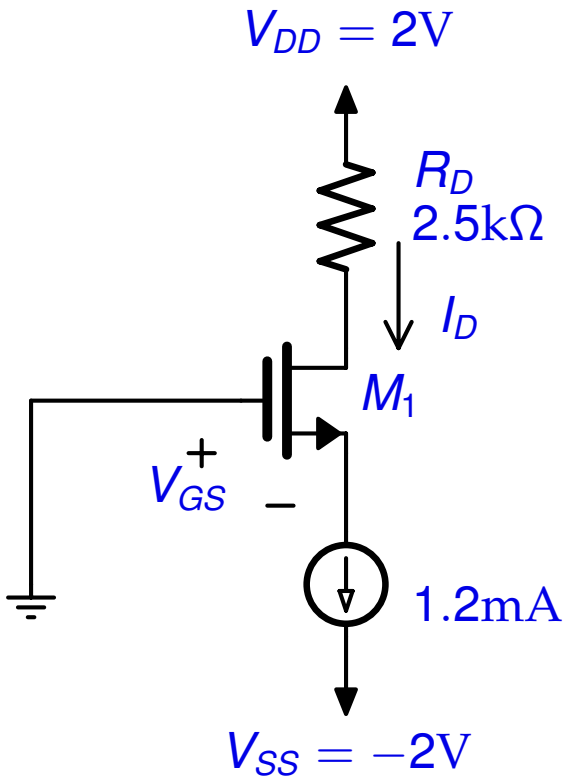
Topics Covered

- Difference between large/small signal analysis
- Semiconductor materials
- Mosfet transistors
  - NMOS/PMOS parameters
  - Overdrive voltage
  - Cutoff/Triode/Active regions
  - DC operating point

- Bonus Slides

DC Bias Example 5

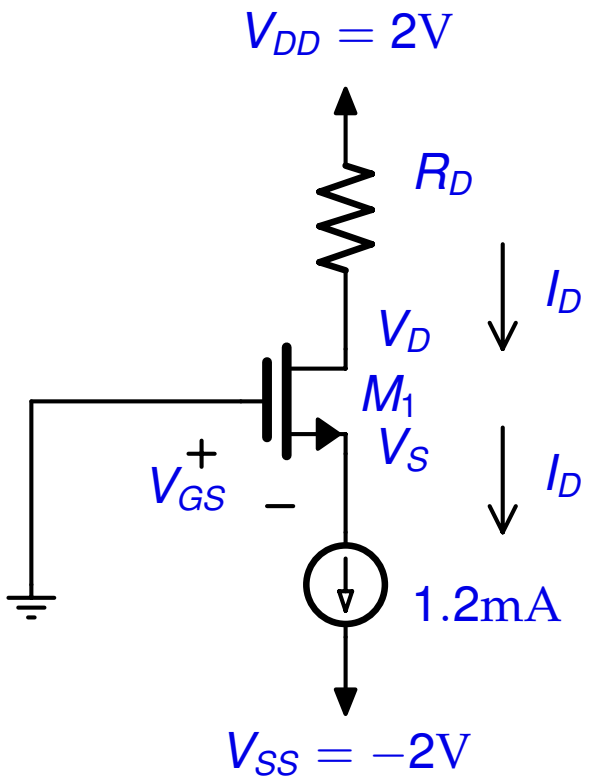
- Find V_S, V_{GS}, V_{DS} and I_D for ...



$V_{tn} = 0.3\text{V}$
$\mu_n C_{ox} = 240\mu\text{A/V}^2$
$W = 10\mu\text{m}$
$L = 100\mu\text{m}$
$\lambda_n = 0.1\text{V}^{-1}$

DC Bias Example 5

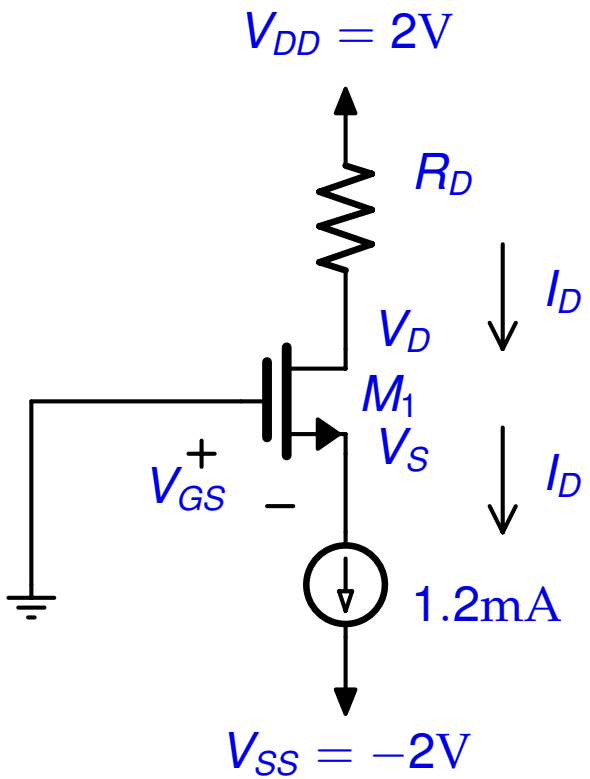
- Assume M_1 is in the active region



- We have the same result as in Example 4 for V_{GS} and V_S however, now with the new value for R_D ...
- $V_D = V_{DD} - I_D R_D = -1\text{V}$
- Since V_D is not greater than $V_G - V_{tn} = -0.3\text{V}$
- **Contradiction**...
  - M_1 is NOT in the active region

DC Bias Example 5

- Assume M_1 is in the triode region



- $I_D = I_S = 1.2\text{mA}$
- $I_D = \mu_n C_{ox}(W/L)(V_{ov} - V_{DS}/2)V_{DS}$
- $1.2\text{mA} = 0.024(V_{ov} - V_{DS}/2)V_{DS}$
- We now have one equation with 2 unknowns so we need to find a relationship between V_{ov} and V_{DS}
- $V_{DS} = V_D - (-V_{ov} - V_{tn})$
- $V_{ov} = V_{DS} - V_{tn} - V_D$
- where $V_D = V_{DD} - I_D R_D = -1\text{V}$

DC Bias Example 5

- Combine V_{DS} eqn with triode I_D eqn

$$1.2e-3 = 0.024(V_{ov} - 0.5V_{DS})V_{DS}$$
$$1.2e-3 = 0.024((V_{DS} - V_{tn} - V_D) - 0.5V_{DS})V_{DS}$$
$$1.2e-3 = 0.024(0.5V_{DS}^2 - (V_{tn} + V_D)V_{DS})$$

  resulting in

$$0.5V_{DS}^2 + 0.7V_{DS} - 0.05 = 0$$

- $V_{DS} = 68.11\text{mV}$ and -1.468V
  - (we ignore the negative solution since $V_{DS} > 0$)
- $V_{ov} = V_{DS} - V_{tn} - V_D = 0.7681\text{V}$
- $V_{GS} = V_{ov} + V_{tn} = 1.068\text{V}$
- $V_S = 0 - V_{GS} = -1.068\text{V}$
- $I_D = 1.2\text{mA}$