Single Transistor Gain Circuit

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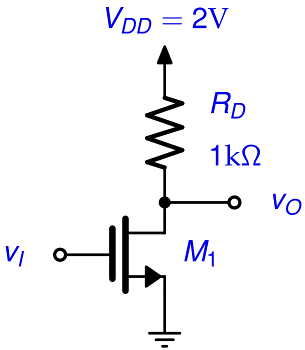
Single Transistor Gain Circuit

- In general, a gain circuit consists of
  - Drive stage
  - Load stage
- Drive stage
  - Single transistor
- Load stage is one of
  - Resistor
  - Current source (made with a transistor)

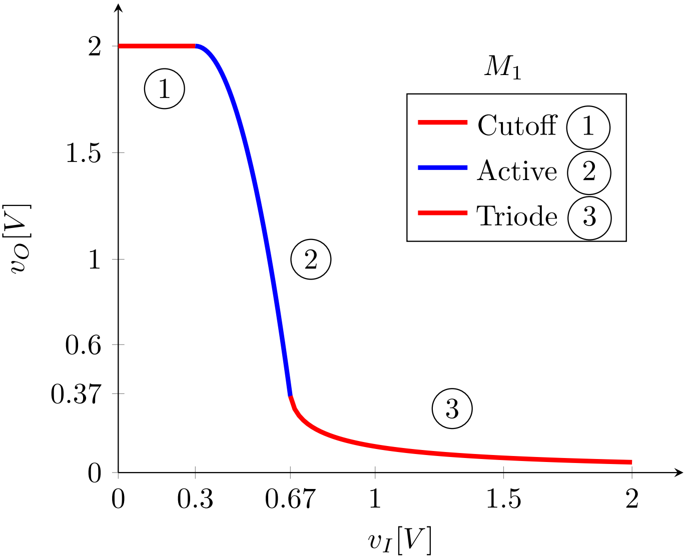
- ”Single transistor” gain circuit refers to the drive stage consisting of a single transistor

Gain Circuit with Resistor Load



- $V_{tn} = 0.3\mathrm{V};\ \mu_n C_{ox} = 240\mu\mathrm{A/V}^2$
- $(W/L) = 100$
- Let $\lambda_n = 0$
  - results in $r_o \to \infty$
- Want to plot v_O vs v_I
  - as v_I goes from 0 to V_{DD}

Gain Circuit with Resistor Load



Gain Circuit with Resistor Load

- M_1 is cutoff in region 1
  - v_I is less than V_{tn}
- M_1 is active in region 2
  - As soon as $v_I > V_{tn}$, M_1 on and active
  - remains active until $v_O < v_I - V_{tn}$

    when drain voltage is less than gate voltage by a threshold voltage

    $v_O = V_{DD} - i_D * R_D$

    $i_D = 0.5\mu_n C_{ox}(W/L)(v_I - V_{tn})^2$
  - In this case, end of active is $v_I = 0.67\mathrm{V}$, $v_O = 0.37\mathrm{V}$
- M_1 is triode in region 3

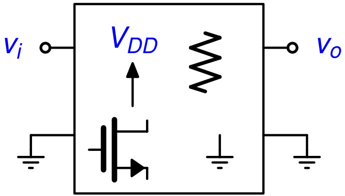
    $v_O = V_{DD} - i_D * R_D$

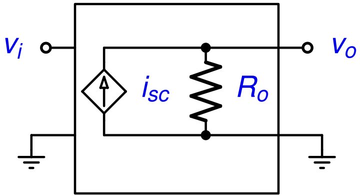
    $i_D = \mu_n C_{ox}(W/L)(v_I - V_{tn} - 0.5v_O)v_O$

Gain Circuit with Resistor Load

- Largest small signal gain
  - where the slope of v_O/v_I is largest in magnitude
  - Then a small change in v_I can cause a large change in v_O
- For above example, occurs at $v_I = 0.67\mathrm{V}$
  - But this bias point would give very little headroom as M_1 would go into triode as v_O decreases and gain would drop
  - A better bias point might be around $v_O = 1\mathrm{V}$

- Good method to find small signal voltage gain
  - Model circuit as Norton equivalent
  - Find output impedance, R_o, at output node
  - Find short circuit current, i_{sc} at output node as function of v_i
  - $v_o = i_{sc} R_o$

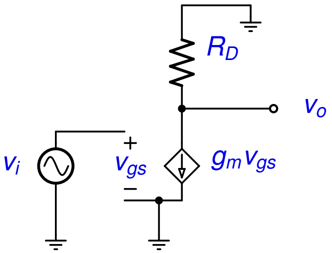




$i_{sc} = G_m v_i$

Small Signal - Gain Circuit/Resistor Load

- Active region



- $R_o = R_D$; $i_{sc} = -g_m v_i$
- $v_o = -g_m R_D v_i$
- $v_o / v_i = -g_m R_D$
- **To increase gain... increase g_m or R_D**
- Recall

$$g_m = \mu_n C_{ox} (W/L) V_{ov}$$
$$g_m = 2 I_D / V_{ov}$$
$$g_m = \sqrt{2 \mu_n C_{ox} (W/L) I_D}$$

- $\mu_n C_{ox}$ set by fabrication and not controlled by designer
- If output bias voltage fixed at say $1\mathrm{V}$, then I_D is fixed if R_D is fixed.

Small Signal - Gain Circuit/Resistor Load

- Can increase g_m by decreasing V_{ov} but...
  - g_m does not increase for V_{ov} below about $50\mathrm{mV}$
  - a practical effect seen with better modelling
- What about increasing R_D?
  - If R_D increased, I_D must decrease to keep v_O around $1\mathrm{V}$
- In summary, it is difficult to get a large gain from a gain circuit with a resistor load
- Would like a large load resistance that does not need to have a large of dc bias voltage across it

  - **Replace R_D with a current source**

Practical Ideal Current Source

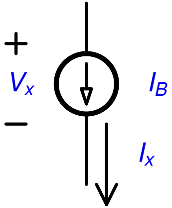
- Ideal current source would give constant current no matter what voltage, V_x, across it
- "Practical ideal" current source

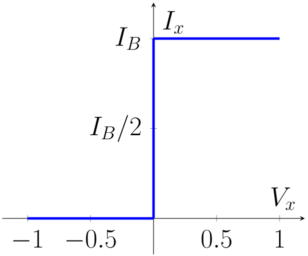
  $V_x > 0$ then $I_x = I_B$

  $V_x = 0$ then $0 < I_x < I_B$

  $V_x < 0$ then $I_x = 0$

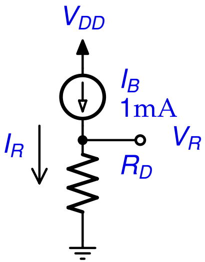
- I_B is desired current; I_x is actual current





Practical Ideal Current Source

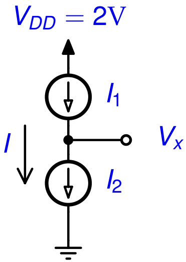
Practical Ideal



- For $V_{DD} = 2\text{V};\ R_D = 1\text{k}\Omega$
  $I_R = 1\text{mA};\ V_R = 1\text{V}$
- For $V_{DD} = 3\text{V};\ R_D = 1\text{k}\Omega$
  $I_R = 1\text{mA};\ V_R = 1\text{V}$
- For $V_{DD} = 0.5\text{V};\ R_D = 1\text{k}\Omega$
  $I_R = 0.5\text{mA};\ V_R = 0.5\text{V}$
- For $V_{DD} = 2\text{V};\ R_D = 4\text{k}\Omega$
  $I_R = 0.5\text{mA};\ V_R = 2\text{V}$
- For $V_{DD} = -1\text{V};\ R_D = 1\text{k}\Omega$
  $I_R = 0\text{mA};\ V_R = 0\text{V}$

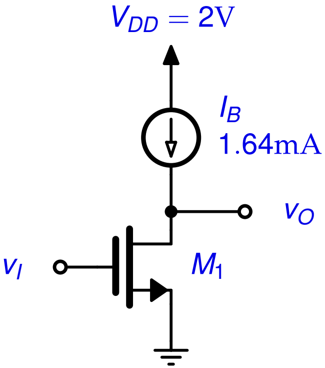
Current Source/Current Source Circuit

Practical Ideal



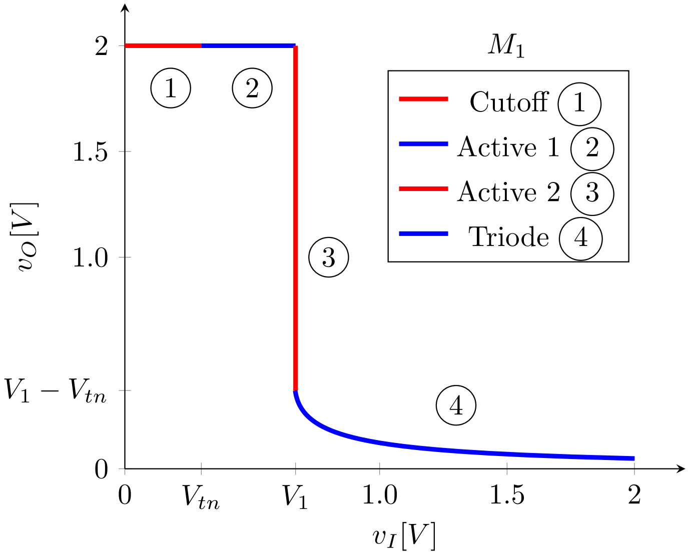
- For $I_1 = 1\mathrm{mA};\ I_2 = 0.5\mathrm{mA}$
  $V_x = V_{DD} = 2\mathrm{V}$
- For $I_1 > I_2$
  $V_x = V_{DD} = 2\mathrm{V}$
- For $I_1 < I_2$
  $V_x = 0\mathrm{V}$
- For $I_1 = I_2$
  $0 < V_x < V_{DD}$
  V_x can be anywhere between 0 and V_{DD}

Gain Circuit with Current Source Load: $\lambda = 0$



- Ideal current source
  (always assume practical)
- $V_{tn} = 0.3\mathrm{V};\ \mu_n C_{ox} = 240\mu\mathrm{A}/\mathrm{V}^2$
- $(W/L) = 100$
- Let $\lambda_n = 0$
  - results in $r_o \to \infty$
- Want to plot v_O vs v_I
  - as v_I goes from 0 to V_{DD}

Gain Circuit with Current Source Load: $\lambda = 0$



Gain Circuit with Current Source Load: $\lambda = 0$

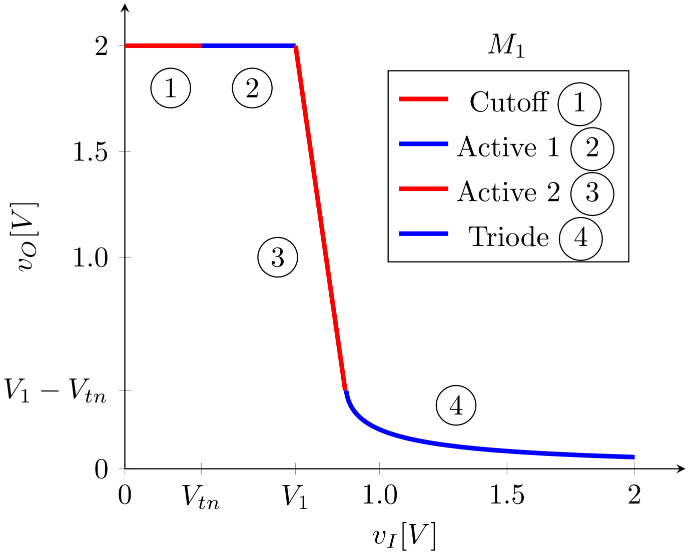
- M_1 is cutoff in region 1
- M_1 is active in region 2
  - $I_{D1} < I_B = 1.64\text{mA}$
  - Results in $v_O = V_{DD}$
  - Current pulled from V_{DD} is I_{D1}
- M_1 is active in region 3
  - $I_{D1} = I_B = 1.64\text{mA}$
  - v_O somewhere between V_{DD} and where M_1 goes into triode
- In region 3
  - Gain is ∞ since slope is ∞
- M_1 is triode in region 4
  - Edge of triode at ...
  - drain of M_1 is $V_{G1} - V_{tn}$
  - and $V_{G1} = V_1$
  - $I_{D1} = I_B = 1.64\text{mA}$ in this region

- V_1 found from $I_{D1} = 0.5\mu_n C_{ox}(W/L)(V_1 - V_{tn})^2 = I_B$
- $V_1 = 0.67\text{V}$

Gain Circuit with Current Source Load: λ finite

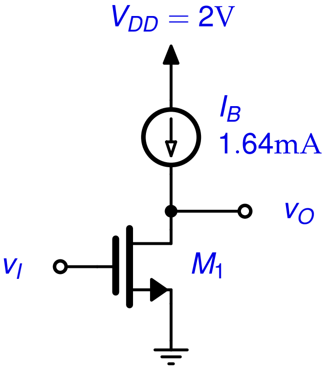
- Now let $\lambda > 0$
- Same as before except that region 3 has a finite slope

Gain Circuit with Current Source Load: λ finite

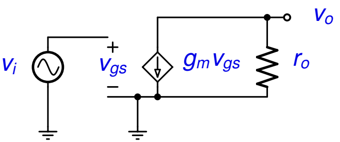


Small Signal - Gain Circuit/Ideal Current Source Load

- In region 2, I_B acts as a short circuit
  - Small signal gain = 0
- In region 3, we have the following

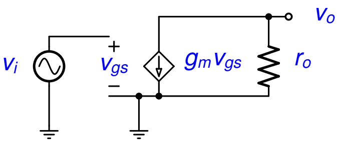


Small signal in active region 3



Small Signal - Gain Circuit/Ideal Current Source Load

- Active region

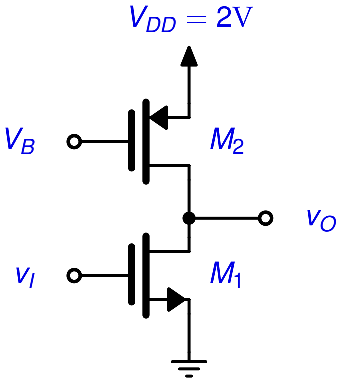


- $R_o = r_o$; $i_{sc} = -g_m v_i$
- $v_o = -g_m r_o v_i$
- $v_o / v_i = -g_m r_o$
- $g_m = 2I_D / V_{ov}$
- $r_o = L / (\lambda' I_D)$
- $v_o / v_i = \frac{-2L}{\lambda' V_{ov}}$

- Intrinsic gain of single transistor with $L = 0.2\mu\mathrm{m}$
- Typical values
  - $V_{ov} = 0.2\mathrm{V}$; $\lambda' = 0.1\mu\mathrm{m}/\mathrm{V}$
  - Intrinsic gain: $v_o / v_i = 20\mathrm{V}/\mathrm{V}$

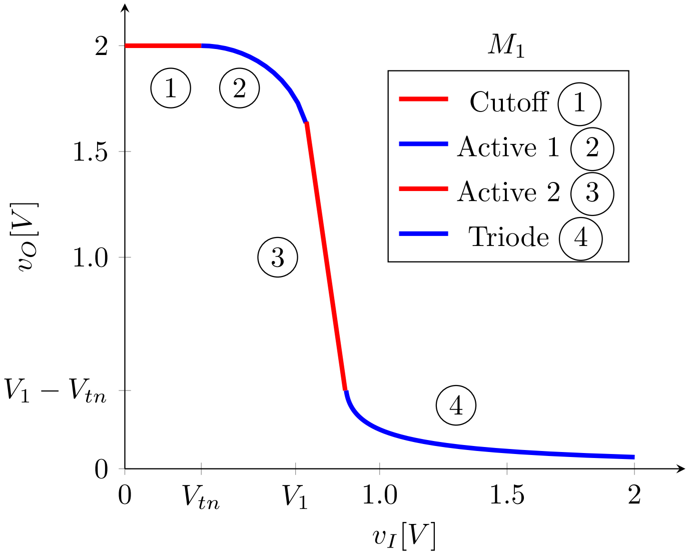
Gain Circuit with PMOS Load

- Use a single PMOS transistor to build current source load for NMOS drive transistor



- V_B is a constant dc voltage
  - When M_2 active, M_2 acts like a current source
  - M_2 will be triode when v_O close to V_{DD}

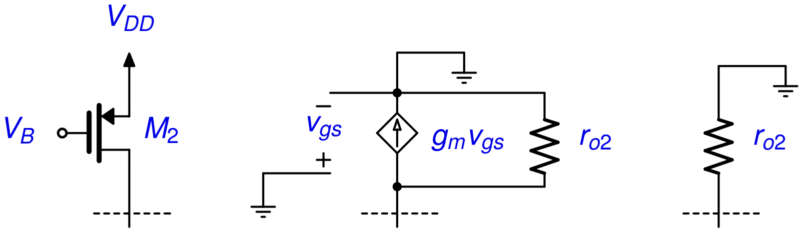
Gain Circuit with PMOS Load



Gain Circuit with PMOS Load

- Region 1
  - M_1 cutoff; M_2 triode
- Region 2
  - M_1 active; M_2 triode
- Region 3
  - M_1 active; M_2 active
- Region 4
  - M_1 triode; M_2 active
- As a gain circuit, want the circuit to be in region 3
  - Small signal model for M_2 is just a resistor of value r_{o2}

Gain Circuit with PMOS Load

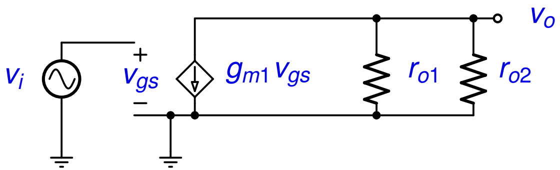


- Since $v_{gs} = 0$, $g_m v_{gs} = 0$ so ...

  Looking into the drain of M_2 is r_{o2}

Small Signal - Gain Circuit/PMOS Load

- Active region



- $R_o = r_{o1} || r_{o2};\ i_{sc} = -g_m v_i$
- $v_o / v_i = -g_{m1}(r_{o1} || r_{o2})$
- If $r_o \equiv r_{o1} = r_{o2}$

  $v_o / v_i = -\frac{g_{m1} r_o}{2}$
- The typical gain is one half of the intrinsic transistor gain

Small Signal - Gain Circuit/PMOS Load

- $g_m = 2I_D/V_{ov}; \; r_o = L/(\lambda' I_D)$
- $v_o/v_i = -\frac{g_{m1} r_o}{2} = L/(\lambda' V_{ov})$
- How can we increase gain?
- Decrease V_{ov}
  - Stops increasing g_m when $V_{ov} < 50\mathrm{mV}$
- Increase L
  - Need to also increase W to maintain same V_{ov}
  - Increases input capacitance so slower circuit
- Is there another way?.. Yes!
  - Cascade amp
  - Cascode amp

Topics Covered

- Single transistor gain circuit
- Small-signal gain analysis
- Replace load R_D with current source
- Gain circuit with PMOS load