Current Mirrors

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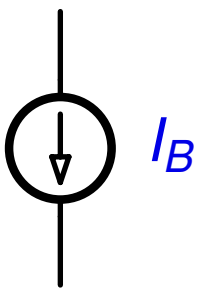
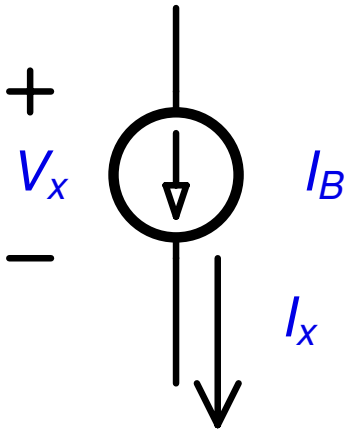
Current Source

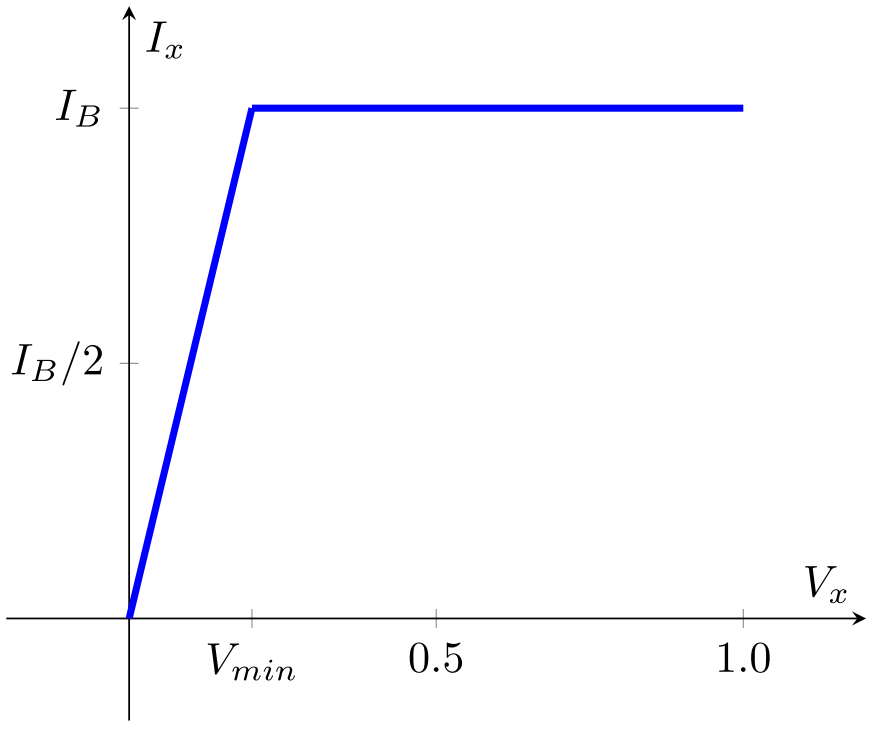
- Current sources are often used for general circuit biasing and used as loads for amplifiers
- A current **source** is created using a current **mirror**



Current source symbol

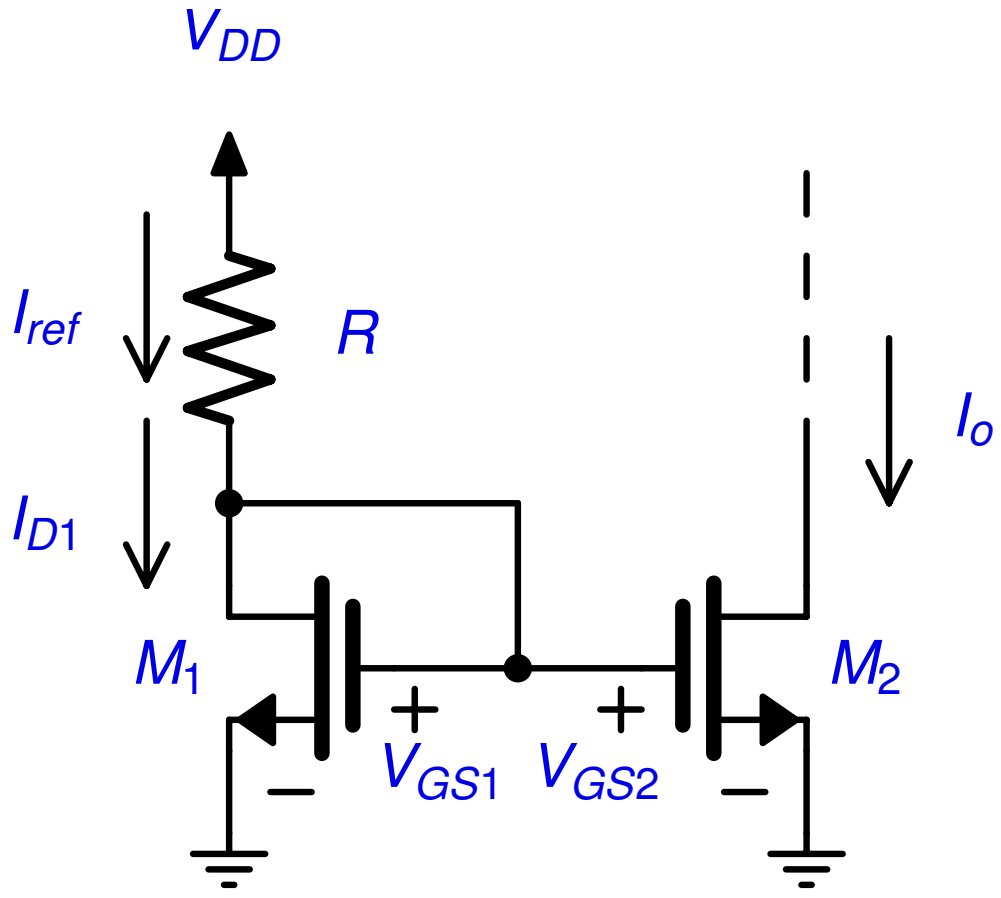
Current Source Specs





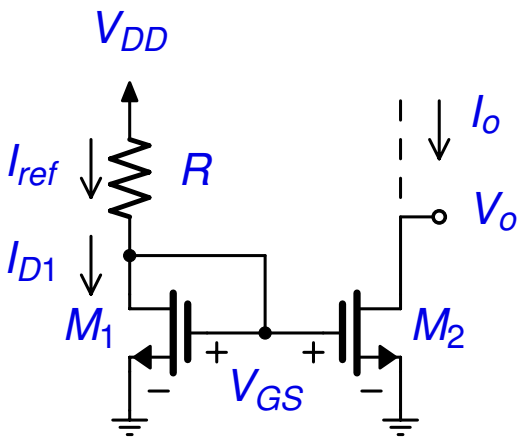
- 3 main specs
  - I_B - value of current source
  - R_o - output impedance (ideally ∞)
  - V_{min} - minimum voltage required (ideally 0)
- If $R_o \to \infty$, then $I_x = I_B$ for $V_x > V_{min} > 0$

Current Mirror



- Here, M_2 is the current source while M_1 sets the voltage V_{GS2} which sets the current for M_2
- We will start by assuming $\lambda_n = 0$

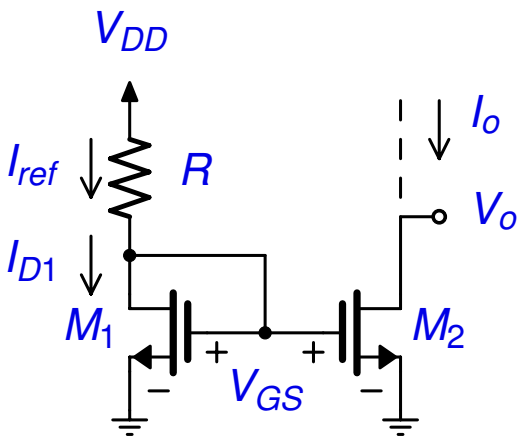
Current Mirror



- For current mirror, we assume M_1 and M_2 are matched
  - $\mu_n \equiv \mu_{n1} = \mu_{n2}$
  - $C_{ox} \equiv C_{ox1} = C_{ox3}$
  - $V_{tn} \equiv V_{tn1} = V_{tn2}$
  - This is achieved by having the 2 transistors on the same integrated circuit and relatively close to each other.
- We also have

  $$V_{GS} \equiv V_{GS1} = V_{GS2}$$

Current Mirror



- For M_1
  - Since $V_{DS1} = V_{GS1}$
    - In either cutoff or active region (not triode)
    - In cutoff ONLY IF $V_{DD} \leq V_{tn}$
  - $I_{D1} = 0.5\mu_n C_{ox}(W/L)_1(V_{GS} - V_{tn})^2$
  - $I_{D1} = I_{ref} = (V_{DD} - V_{GS})/R$
  - Combine above 2 eqn to find V_{GS} and I_{ref}
- For M_2
  - $I_{D2} = 0.5\mu_n C_{ox}(W/L)_2(V_{GS} - V_{tn})^2$

- Comparing I_{D1} and I_{D2} equations, we have

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \tag{1}$$

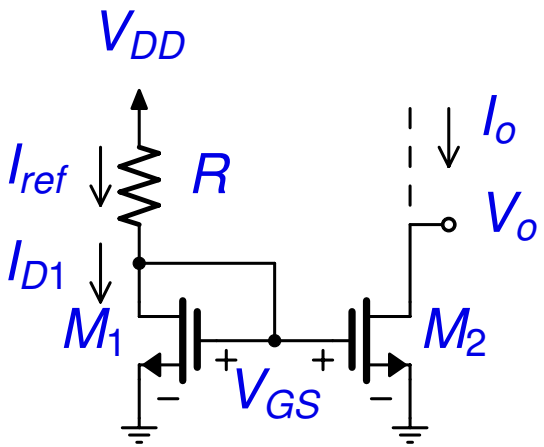
Current Mirror

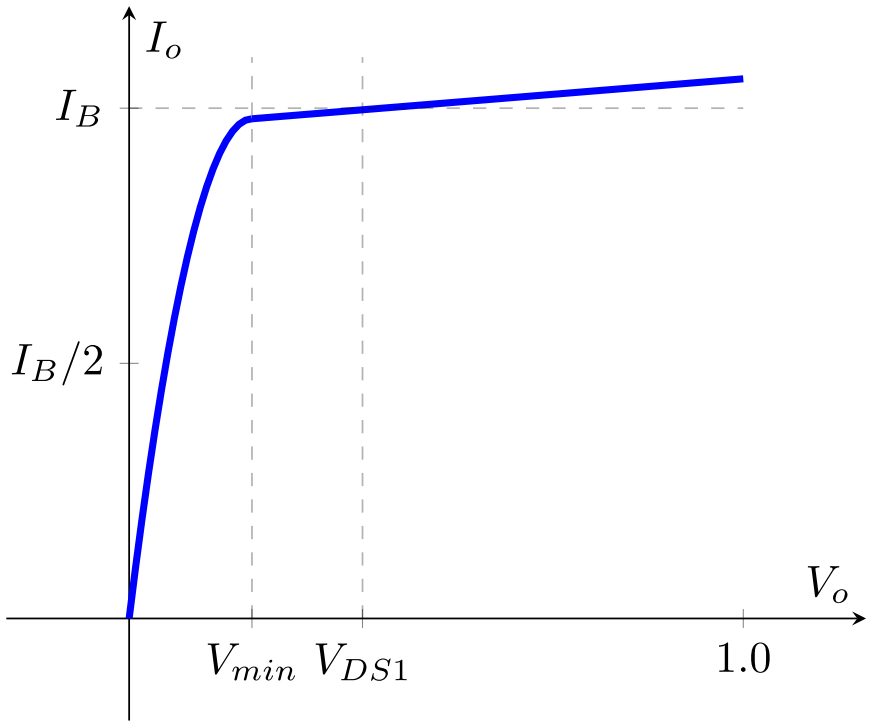
- The above is valid as long as both transistors are in the active region
- For M_1
  - $V_{DD} \geq V_{tn}$
- For M_2
  - $V_{DS2} \geq V_{min}$ where $V_{min} = V_{ov2} = V_{GS} - V_{tn}$
  - So M_2 remains active as long as its drain voltage is high enough
  - So it depends on what is attached to the M_2 current source
- Also, in general, the length of M_1 and M_2 are also matched
  - This would make the above I_{D2}/I_{D1} equation accurate even when $\lambda_n \neq 0$ for the case $V_{DS2} = V_{DS1}$

Current Mirror with $\lambda_n \neq 0$

- For the case $\lambda_n \neq 0$ we have
- $I_{D1} = 0.5\mu_n C_{ox}(W_1/L_1)(V_{GS} - V_{tn})^2(1 + (\lambda'_n/L_1)V'_{DS1})$
- $I_{D2} = 0.5\mu_n C_{ox}(W_2/L_2)(V_{GS} - V_{tn})^2(1 + (\lambda'_n/L_2)V'_{DS2})$
- Recall $V'_{DS} \equiv V_{DS} - V_{ov}$
- So if $L_2 = L_1$ then we have I_{D2} precisely equals $(W_2/W_1)I_{D1}$ at the time when $V_{DS2} = V_{DS1}$
- So when the drain source voltages of the 2 transistors are equal, our current mirror output, I_{D2} will be accurately related to the reference current, I_{D1}.

Current Mirror Plot

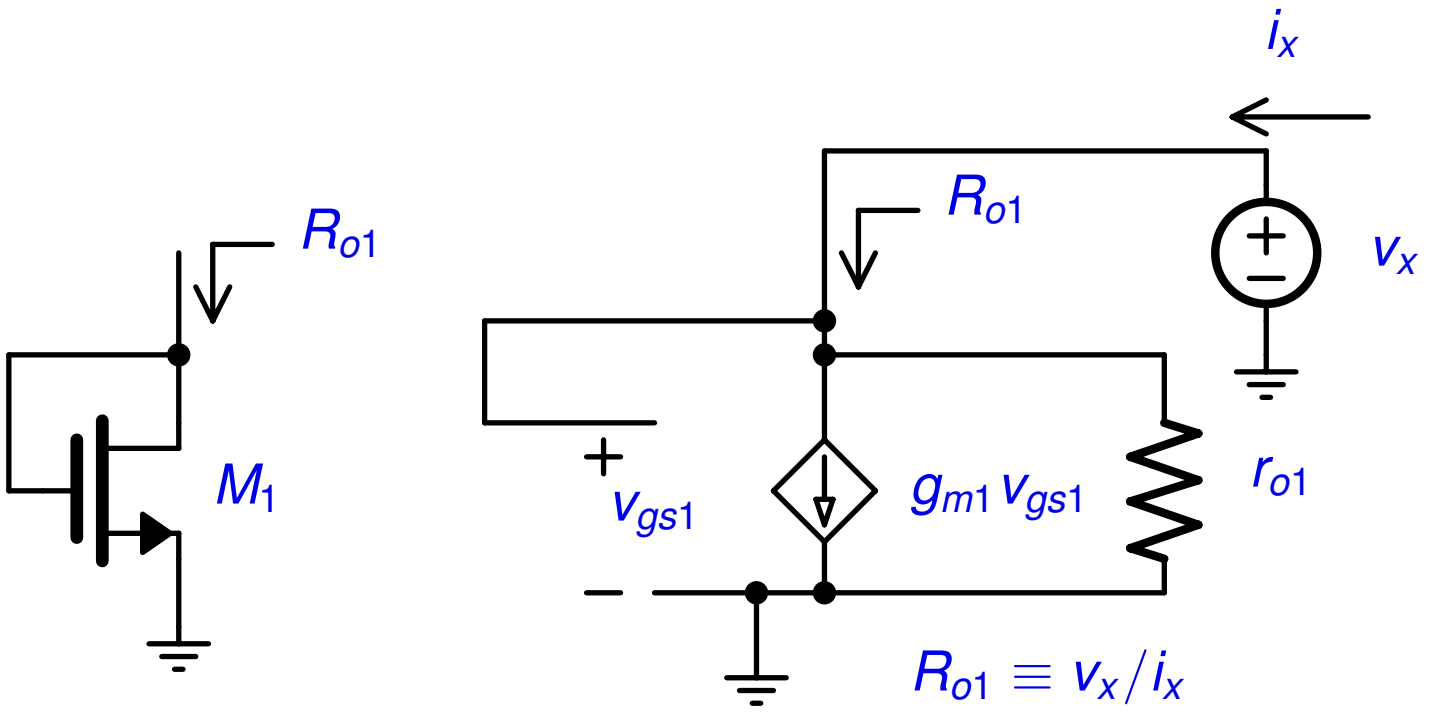




- The non-zero slope for $V_o > V_{min}$ is due to the finite output impedance of M_2
- This slope equals $1/R_o$ where in this case, $R_o = r_{o2}$
- I_o precisely equals our desired I_B when $V_{DS2} = V_{DS1}$ which is higher than V_{min}

Small Signal Impedances

- We know the impedance looking into the drain of M_2 is r_{o2}
- What is the impedance looking into the gate/drain of M_1?



Small Signal Impedances

- $i_x = g_{m1} v_x + (v_x / r_{o1}) = (g_{m1} + (1/r_{o1}) v_x$
- $R_{o1} = v_x / i_x = (g_{m1} + (1/r_{o1}))^{-1} = \frac{1}{g_{m1}} || r_{o1}$
- $R_{o1} = \frac{1}{g_{m1}} || r_{o1}$
- This configuration is often referred to as a ”diode connected transistor”
  - The term ”diode connected” comes from Bipolar transistors
  - Bipolar transistors (npn or pnp) are back to back diodes and in this case, one of the diodes is short circuited.

Current Mirror Example 1

- Given $I_{ref} = 40\mu\text{A}$, $W_1 = 2\mu\text{m}$ and

  $\mu_n C_{ox} = 120\mu\text{A/V}^2$; $V_{tn} = 0.3\text{V}$; $\lambda'_n = 50\text{nm/V}$

  $L_1 = L_2 = 200\text{nm}$

  (a) Find W_2 so that $I_{D2} = 20\mu\text{A}$

  (b) Find the output impedance, R_o, of the current source for M_2

  (c) Find the lowest possible output voltage, V_o, for the current source while keeping M_2 active

  (d) At what value of V_o does $I_{D2} = 20\mu\text{A}$?

  (e) Estimate the value of I_{D2} if $V_o = 1\text{V}$ based on small signal analysis

Current Mirror Example 1

Solution

(a) $I_{D2} = (W_2/W_1)I_{D1}$ and we have
$I_{D1} = I_{ref} = 40\mu\text{A};\ W_1 = 2\mu\text{m};\ I_{D2} = 20\mu\text{A}$
Solving, we find $W_2 = 1\mu\text{m}$

(b) The output impedance of the current source is the output impedance of M_2 which is r_{o2}
$r_{o2} = L/(\lambda'_n I_{D2}) = (200e-9)/(50e-9*20e-6) = 200\text{k}\Omega$
So $R_o = r_{o2} = 200\text{k}\Omega$

(c) Since we are finding a dc bias voltage, we will assume $\lambda'_n = 0$
$I_{D2} = 0.5\mu_n C_{ox}(W_2/L_2)V_{ov2}^2$
$20e-6 = 0.5(120e-6)(1/0.2)V_{ov2}^2$
Solving for V_{ov2}, we find $V_{ov2} = 0.258\text{V}$
(we ignore the negative solution since that would make the transistor cutoff)
For M_2 to remain active, $V_{DS2} \geq V_{ov2}$ and since $V_o = V_{DS2}$ the minimum output voltage for V_o is 0.258V

Current Mirror Example 1

Solution

(d) The current mirror will be perfectly matched when $V_{DS2} = V_{DS1}$ since all the other values are the same (except for W which scales the output current).
$V_{DS1} = V_{GS1} = V_{ov1} + V_{tn}$ and since $V_{GS1} = V_{GS2}$ and the threshold voltages are the same, $V_{ov1} = V_{ov2} = 0.258\text{V}$
$V_{DS1} = 0.258 + 0.3 = 0.558\text{V}$
So the $I_{D2} = 20\mu\text{A}$ when $V_o = 0.558\text{V}$
When $V_o > 0.558$, I_{D2} will be higher than $20\mu\text{A}$
When $V_o < 0.558$, I_{D2} will be lower than $20\mu\text{A}$

Current Mirror Example 1

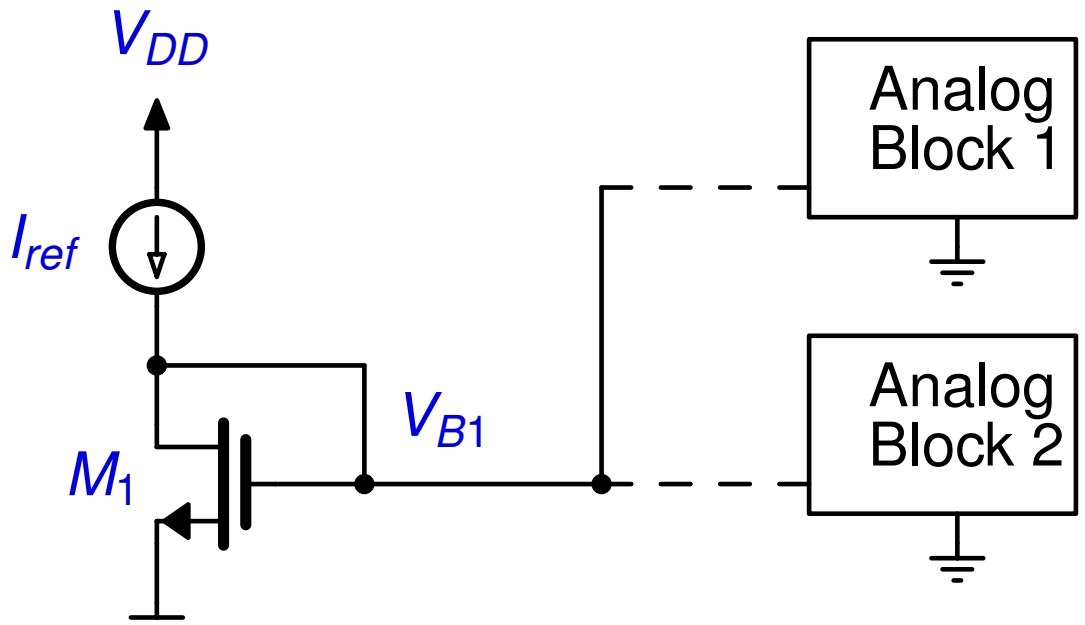
Solution

(e) From small signal analysis, we have
$\Delta I_{D2} = \Delta V_o / R_o$ where R_o is the output impedance of the current source and we found $R_o = 200\text{k}\Omega$
We know from above $I_{D2,0.558} = 20\mu\text{A}$ at $V_o = 0.558\text{V}$ and we want to estimate the current at $V_o = 1\text{V}$
In this case, the change in output voltage is
$\Delta V_o = 1 - 0.558 = 0.442\text{V}$
$I_{D2} = I_{D2,0.558} + \Delta I_{D2} = 20e-6 + (\Delta V_o / R_o)$
$I_{D2} = 20e-6 + (0.442/200e3) = 22.2\mu\text{A}$

Sending Bias Currents around a Chip

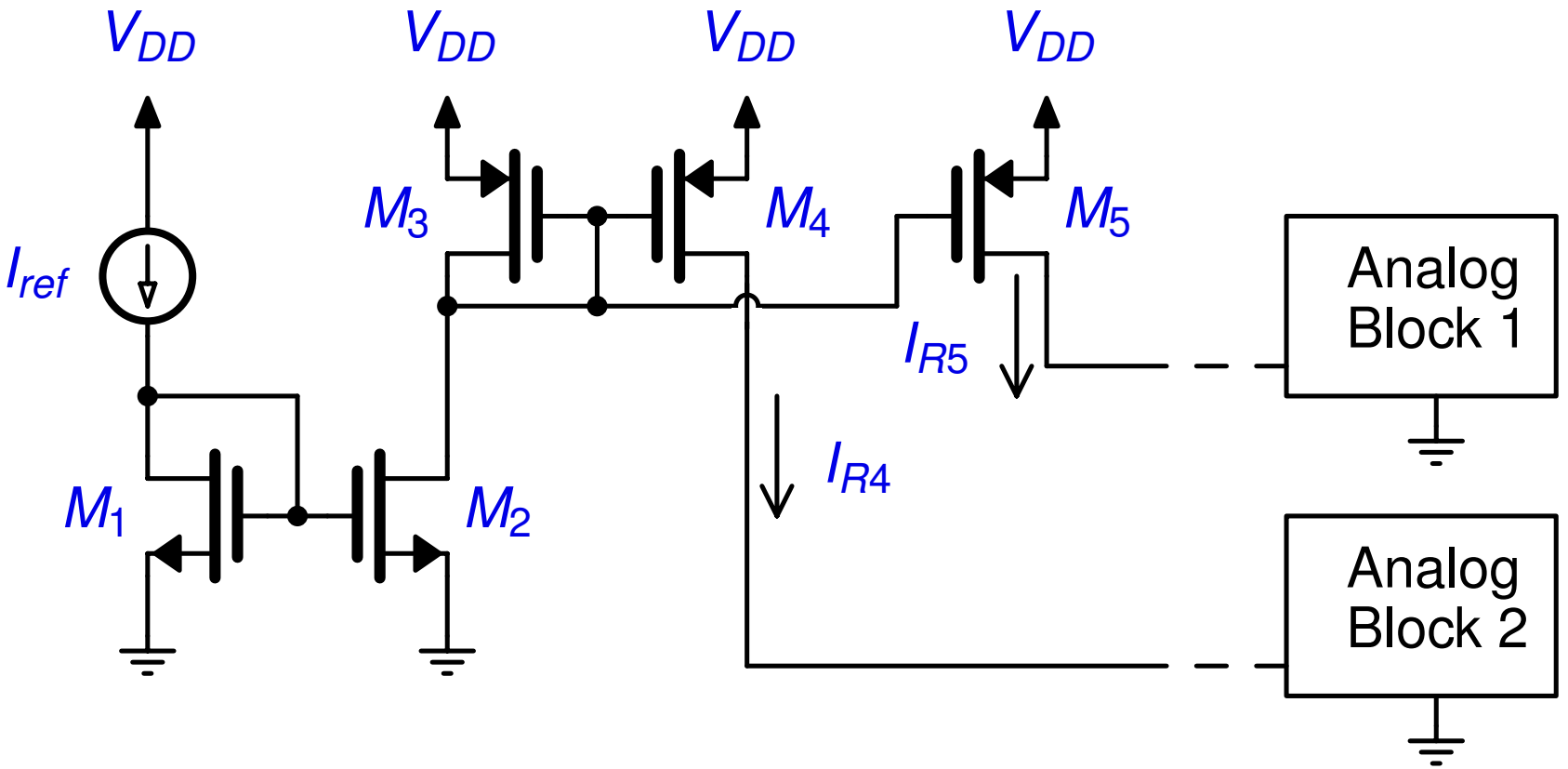
- It is common on an integrated circuit to have multiple analog circuit blocks far apart on the chip
  - Blocks such as analog-to-digital converters, digital-to-analog converters, RF circuits, phase-locked-loops for clocking, SERDES, etc...
- Normally one main bias block is used to generate a constant bias current, I_{ref}, and this current needs to be replicated in all the analog blocks in the chip
- The **WRONG** way to replicate I_{ref} is to send bias voltages to far away blocks
- The **CORRECT** way to replicate I_{ref} is to send bias currents to far away blocks

Sending Bias Currents around a Chip: WRONG way



- Wrong because the grounds at Analog Block 1/2 may be at a different voltage than main bias block
  - Ground wires have resistance and current flowing through ground causes a voltage drop
  - Not an issue when grounds are close to each other
  - Would result in incorrect bias currents AND the bias currents would depend on current through ground wire (noisey bias currents)

Sending Bias Currents around a Chip: CORRECT way



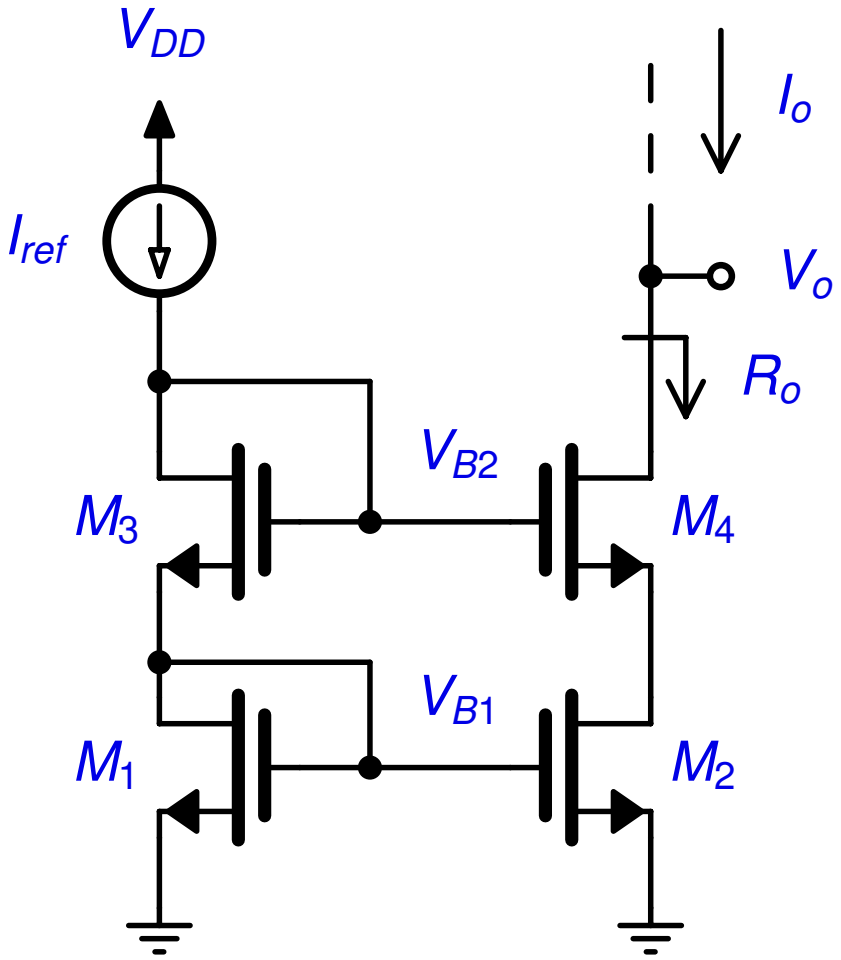
- Send a separate bias current to EACH analog block based on main bias block

Sending Bias Currents around a Chip: CORRECT way

- Matching requirements
  - M_1/M_2 matched (except for W)
  - $M_3/M_4/M_5$ matched (except for W)
  - No need to match NMOS with PMOS
- $I_{R4} = I_{ref} \times (W_2/W_1)(W_4/W_3)$
- $I_{R5} = I_{ref} \times (W_2/W_1)(W_5/W_3)$

Cascode Current Mirror

- To increase the output impedance of current mirror
  - Use cascode



Cascode Current Mirror

- The output impedance for this current mirror is R_o

  $R_o = r_{o4} + (1 + g_{m4} r_{o4}) r_{o2} \approx g_{m4} r_{o4} r_{o2}$
- It is at least $g_m r_o$ greater than just r_{o2}
- Normally, match M_1/M_2 and match M_3/M_4 (except for W)
- So $L_2 = L_1$ and $L_4 = L_3$
- Also make $W_4/W_3 = W_2/W_1$ resulting in

  $I_o = I_{ref} \times (W_2/W_1)$

- Problem with this circuit is V_{min} is too large

Cascode Current Mirror

- $V_{B1} = V_{ov1} + V_{tn}$
- $V_{B2} = V_{B1} + V_{ov2} + V_{tn} = V_{ov1} + V_{ov2} + 2V_{tn}$
- V_{min} occurs when drain of M_4 goes below the gate of M_4 minus one threshold voltage

  $$V_{min} = V_{B2} - V_{tn} = V_{ov1} + V_{ov2} + V_{tn}$$

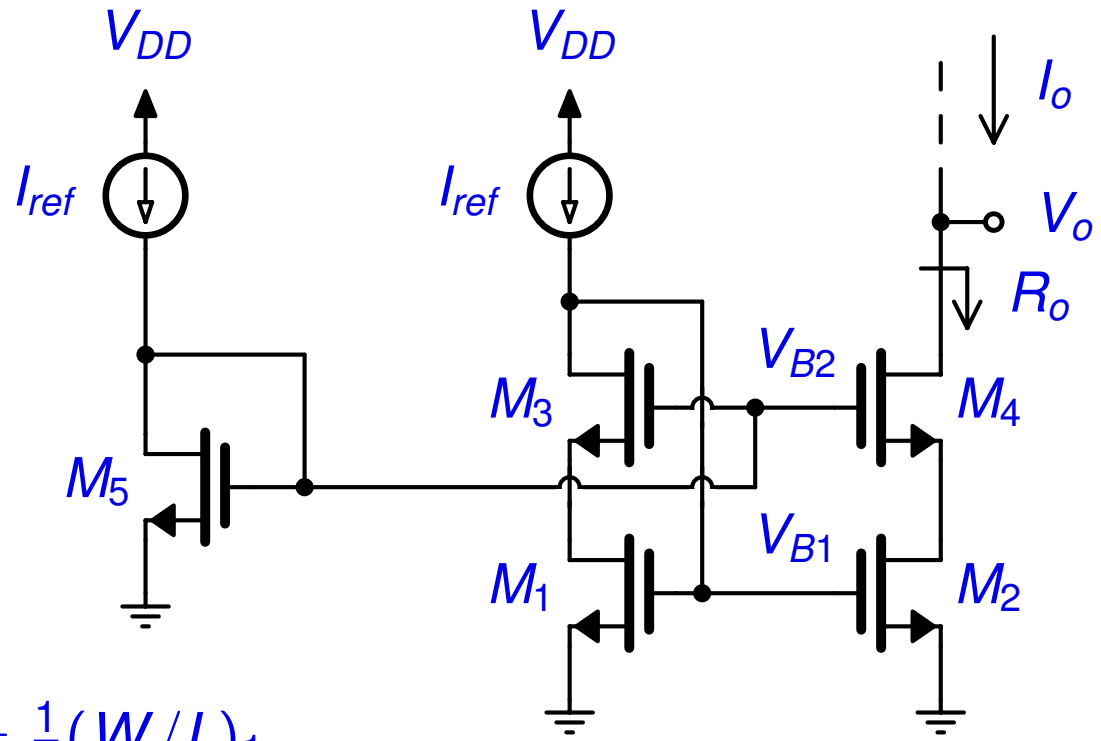
- So in case where $V_{ov} = 0.2\text{V}$ and $V_{tn} = 0.3\text{V}$

  $V_{min} = 0.2 + 0.2 + 0.3 = 0.7\text{V}$

- It turns out, there is a way to reduce V_{min}

Wide Swing Current Mirror

- A wide swing current mirror is a cascode current mirror with a lower V_{min}



$(W/L)_5 = \frac{1}{4}(W/L)_1$

Wide Swing Current Mirror

- To make things easier, assume M_3/M_1 matched including their W
- Since $I_{D3} = I_{D1}$, $V_{ov3} = V_{ov1}$ which we will define as V_{ov}
- First, we find V_{ov5} in terms of V_{ov}
  - $I_{D1} = 0.5\mu_n C_{ox}(W/L)_1 V_{ov}^2$
  - $I_{D5} = 0.5\mu_n C_{ox}(W/L)_5 V_{ov5}^2$
  - Divide the above 2 equations
  - $\frac{I_{D5}}{I_{D1}} = \frac{(W/L)_5 V_{ov5}^2}{(W/L)_1 V_{ov}^2}$
  - But $I_{D5} = I_{D1} = I_{ref}$
  - $V_{ov5} = \sqrt{\frac{(W/L)_1}{(W/L)_5}} \times V_{ov}$
  - If we choose $(W/L)_5 = \frac{1}{4}(W/L)_1$, then
  - $V_{ov5} = 2V_{ov}$

Wide Swing Current Mirror

- Now, we find V_{B2} so we can find V_{min}
  - $V_{B2} = V_{ov5} + V_{tn} = 2V_{ov} + V_{tn}$
- V_{min} occurs when M_4 goes into triode which occurs when its drain voltage is lower than the gate voltage minus V_{tn}
- $V_{min} = V_{B2} - V_{tn} = 2V_{ov}$
- So we have that $V_{min} = 2V_{ov}$ which is one V_{tn} lower than in the non-wide-swing current mirror
- For this reason, the wide-swing current mirror is used in the majority of cases on a chip.
- The downside is that it requires an extra I_{ref}
- In practice, $(W/L)_5 = (1/5) \times (W/L)_1$ to give some margin so that both M_1/M_2 remain in the active region

Wide Swing Current Mirror Example

- Assume a process with
  $L = 0.18\mu\text{m};\ V_{tn} = 0.4\text{V};\ \mu_n C_{ox} = 240\mu\text{A/V}^2;\ \lambda'_n = 50\text{nm/V}$
  (a) Design a wide-swing current mirror with $V_{min} = 0.3\text{V}$ and $100\mu\text{A}$ output current using 2 current references of $50\mu\text{A}$.
  (use a practical choice for $(W/L)_5$)
  Assume all $L = 0.18\mu\text{m}$
  (b) Find the output impedance.

Solution

(a) We first assume that $W_3 = W_1$ so that $V_{ov} \equiv V_{ov3} = V_{ov1}$
We find V_{ov} using
$V_{min} = 0.3 = 2V_{ov} \ \rightarrow\ V_{ov} = 0.15\text{V}$
Now we find W_1
$I_{D1} = 0.5\mu_n C_{ox}(W/L)_1 V_{ov}^2$
$50e-6 = 0.5(240e-6)(W_1/0.18)(0.15)^2$
$W_1 = 3.33\mu\text{m}$ and $W_3 = W_1 = 3.33\mu\text{m}$

Wide Swing Current Mirror Example

Solution

(a) continued

$W_5 = W_1/5 = 0.667\mu\text{m}$

Since we want $I_o = I_{D2} = 100\mu\text{A}$, we have

$I_o = W_2/W_1 \times I_{ref} \rightarrow 100 = W_2/(3.33) \times 50$

$W_2 = 2W_1 = 6.66\mu\text{m}$

Finally, since $W_3 = W_1$, then $W_4 = W_2 = 6.66\mu\text{m}$

(b) For the output impedance

$r_{o2} = r_{o4} = L/(\lambda'_n I_{D2})$

$r_{o2} = r_{o4} = (0.18e-6)/(50e-9 \times 100e-6) = 36\text{k}\Omega$

$g_{m2} = g_{m4} = 2I_{D2}/V_{ov2} = (2 \times 100e-6)/0.15 = 1.3\text{mA/V}$

$R_o = r_{o4} + (1 + g_{m4}r_{o4})r_{o2}$

$R_o = 36e3 + (1 + (1.3e-3)(36e3))(36e3) = 1.76\text{M}\Omega$

This is significantly higher than $36\text{k}\Omega$ that would have occurred if the current mirror was not cascoded.

Topics Covered

- Current source and specs
- Basic current mirror
- Sending bias currents around a chip
- Cascode current mirror
  - Higher output impedance (better accuracy)
  - Wide swing current mirror