Differential Amplifiers

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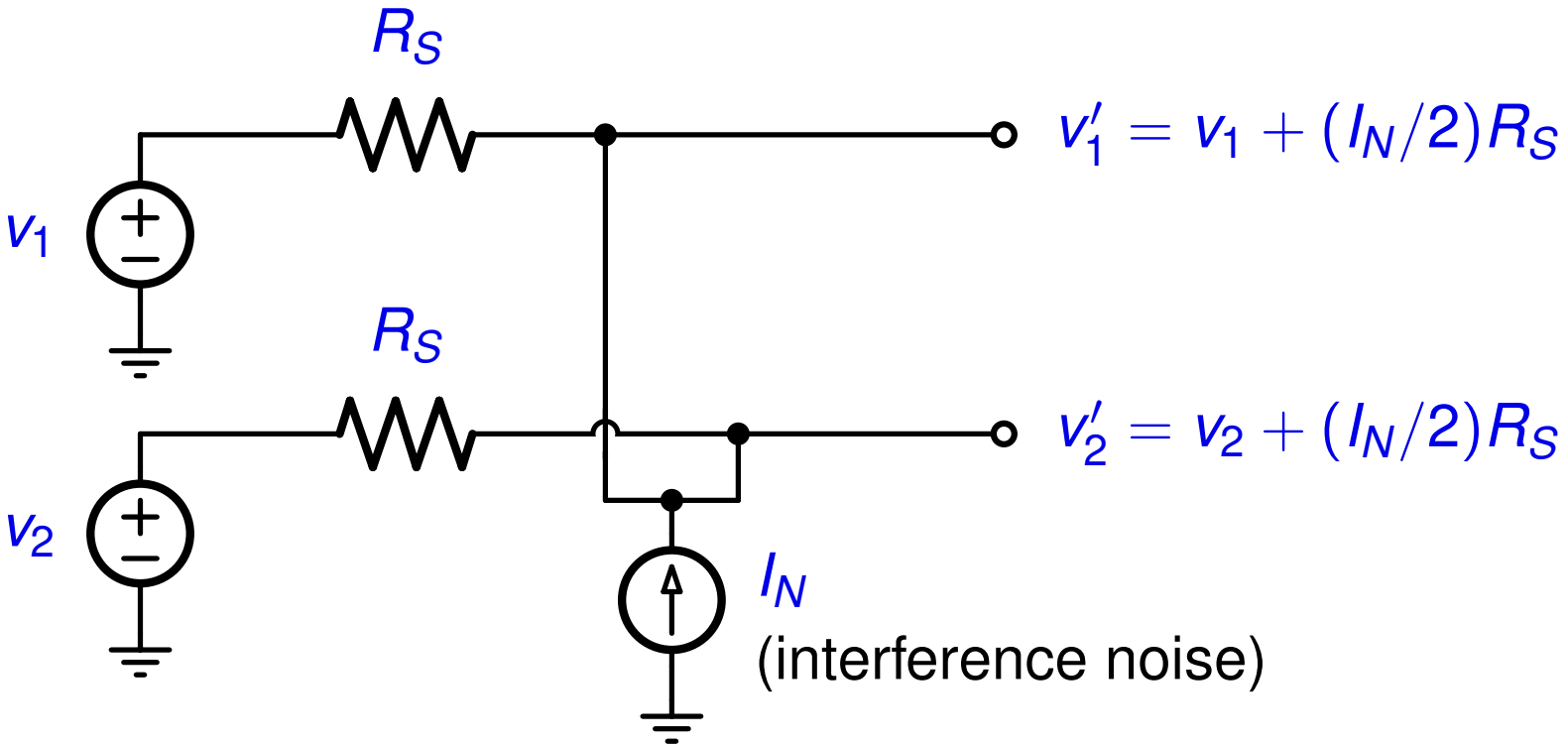
Differential Signals

- Many circuits make use of differential signals
  - ethernet, SATA, PCIe, memory interfaces, ADCs, DACs, ...
- Advantage of differential signalling
  - Rejection of common-mode noise
  - EMI (electromagnetic interference) reduction to other circuits



Differential Signals

- If the 2 signals are matched, the interference noise is the same on each wire so ...
- $v_2' - v_1' = v_2' - v_1$
- Taking the difference between the 2 wires cancels "common-mode" noise
- In general, define

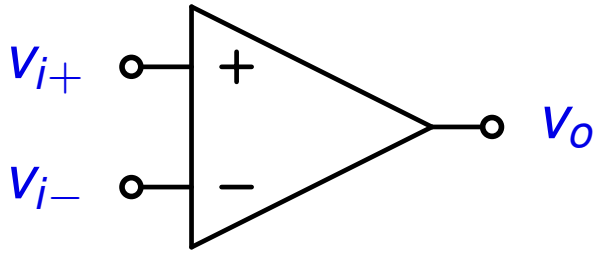
  $$v_2 = V_{CM} + v_{id}/2$$
  $$v_1 = V_{CM} - v_{id}/2$$
- Differential signal

  $$v_{id} = v_2 - v_1$$
  - Difference of 2 signals
- Common-mode signal

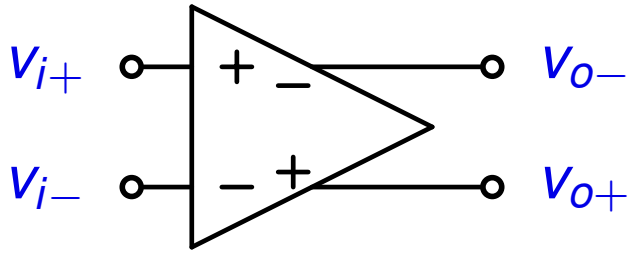
  $$V_{CM} = (v_2 + v_1)/2$$
  - Average of 2 signals

Differential Amplifiers

- Differential inputs used in opamps

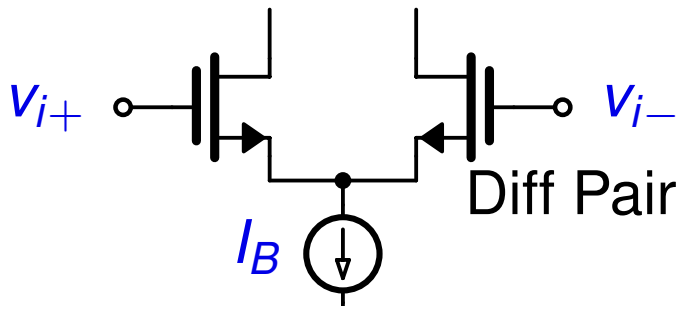


Opamp



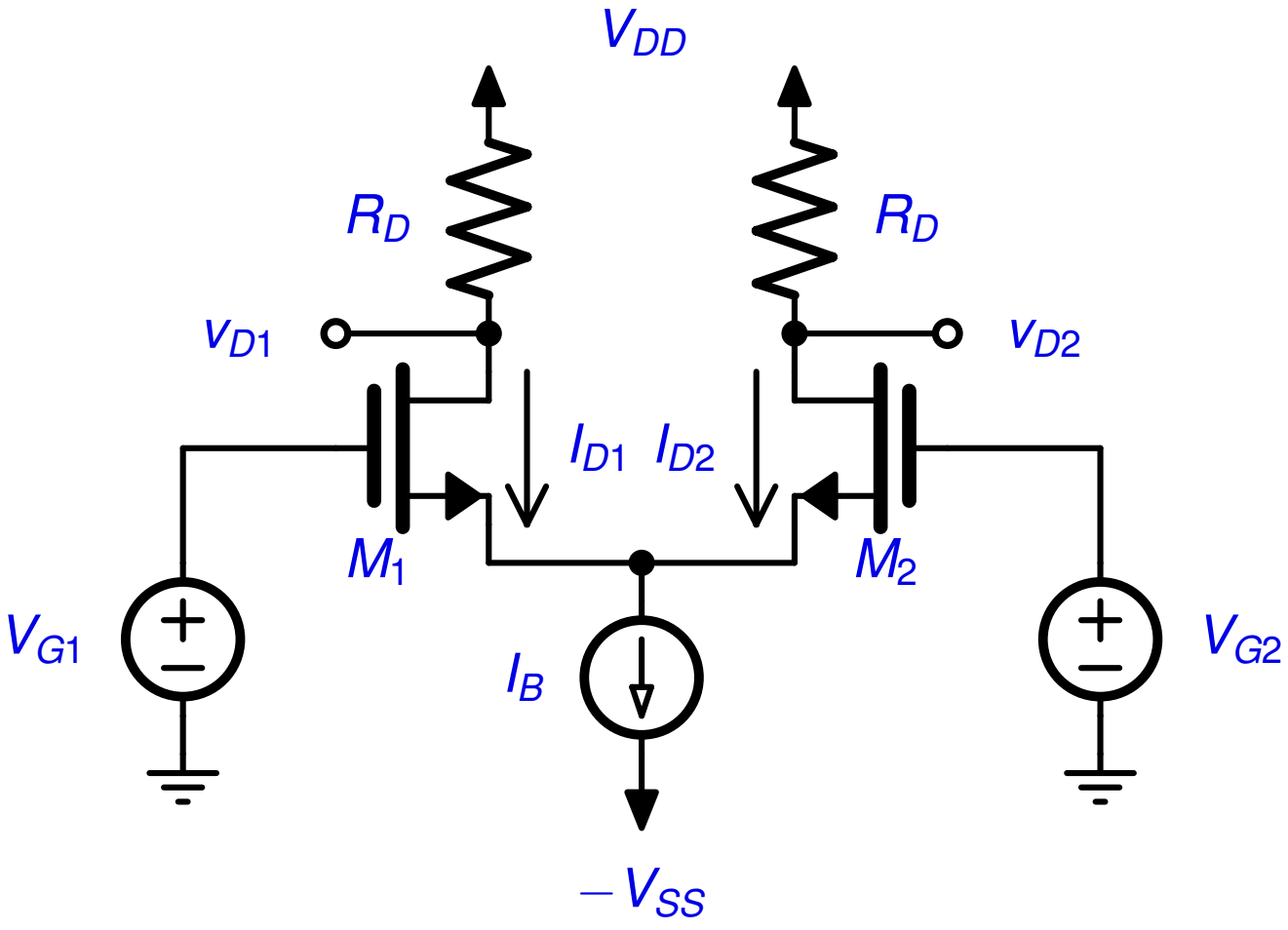
Fully Diff Opamp

- Opamp input stage: transistor differential pair



- Look at large-signal and small-signal for MOS diff pair

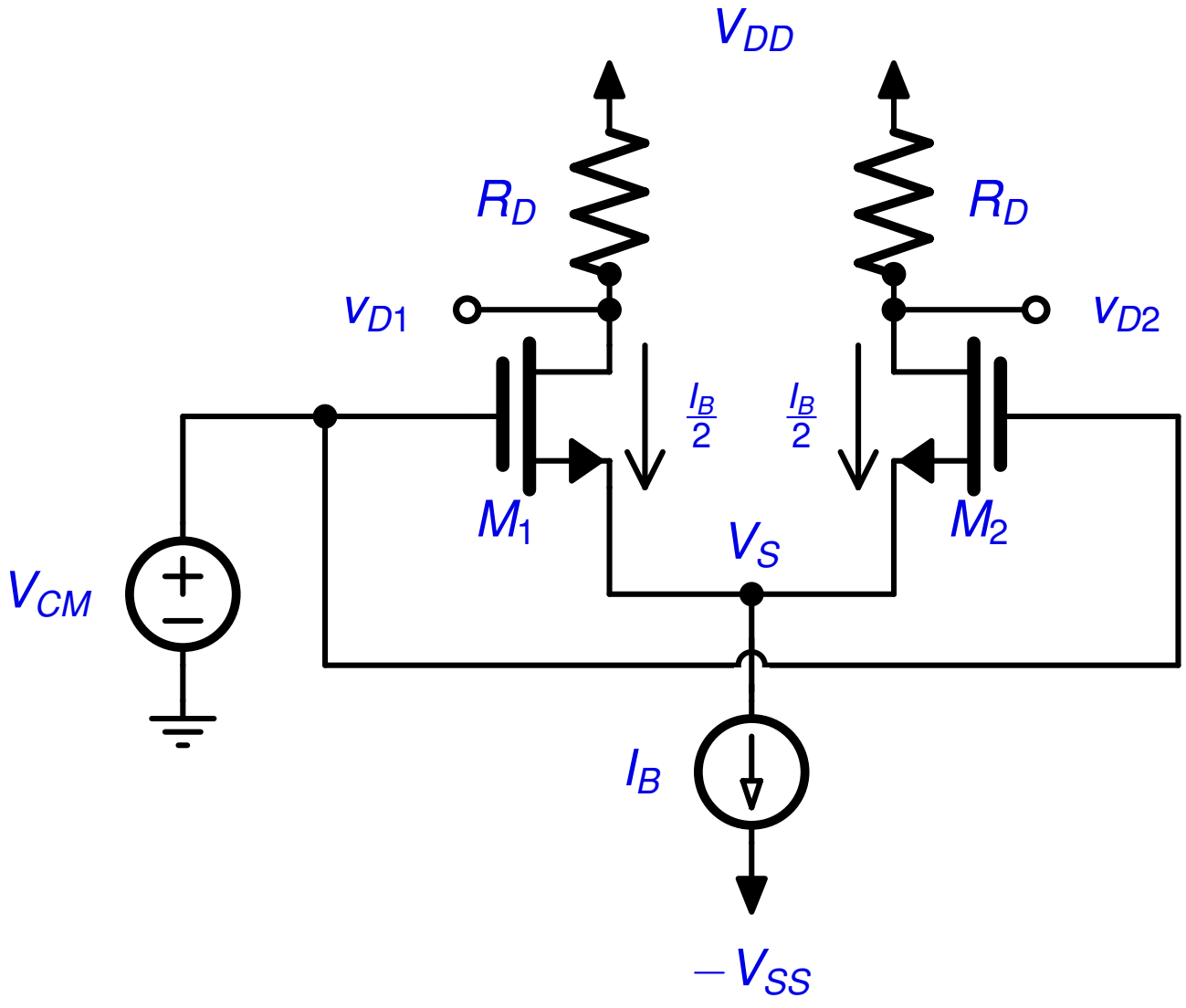
Diff Pair - Large Signal



Diff Pair - Large Signal

- M_1, M_2 are identical
- $i_{D1} + i_{D2} = I_B$
- If $V_{G1} = V_{G2}$
  - $i_{D1} = i_{D2} = I_B/2$
- If $V_{G1} > V_{G2}$
  - $i_{D1} > i_{D2}$
- If $V_{G1} < V_{G2}$
  - $i_{D1} < i_{D2}$
- Can use diff pair to ”steer” the current, I_B

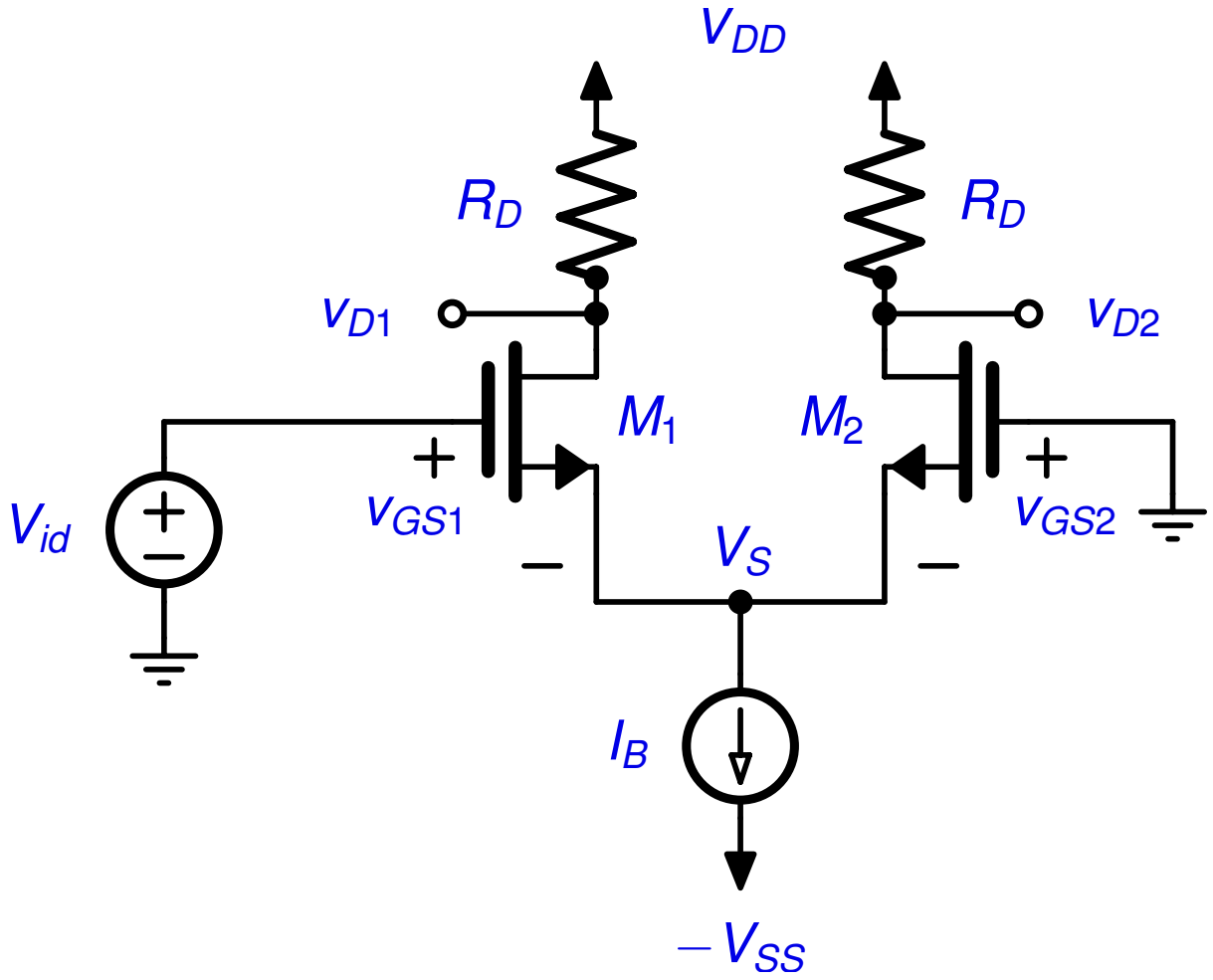
Diff Pair - Large Signal - Common-Mode Input



Diff Pair - Large Signal - Common-Mode Input

- Define V_{CS} be the min voltage required across I_B for it to operate correctly (i.e. be in the active region)
- If $V_S - V_{SS} \geq V_{CS}$ then
  - $V_{D1} = V_{D2} = V_{DD} - (\frac{I_B}{2})R_D$
- If M_1/M_2 both active
  - $I_{D1} = I_B/2 = 0.5\mu_n C_{ox}(W/L)V_{ov}^2$
  - $V_{ov} = \sqrt{I_B/(\mu_n C_{ox}(W/L))}$
- Maximum V_{CM}
  - Occurs when gate is V_t above drain voltage
  - $V_{CM,max} = V_t + V_{DD} - (\frac{I_B}{2})R_D$
- Minimum V_{CM}
  - Occurs when V_S is low enough that I_B does not have min voltage across it
  - Occurs when $V_S = -V_{SS} + V_{CS}$
  - $V_{CM,min} = -V_{SS} + V_{CS} + V_t + V_{ov}$

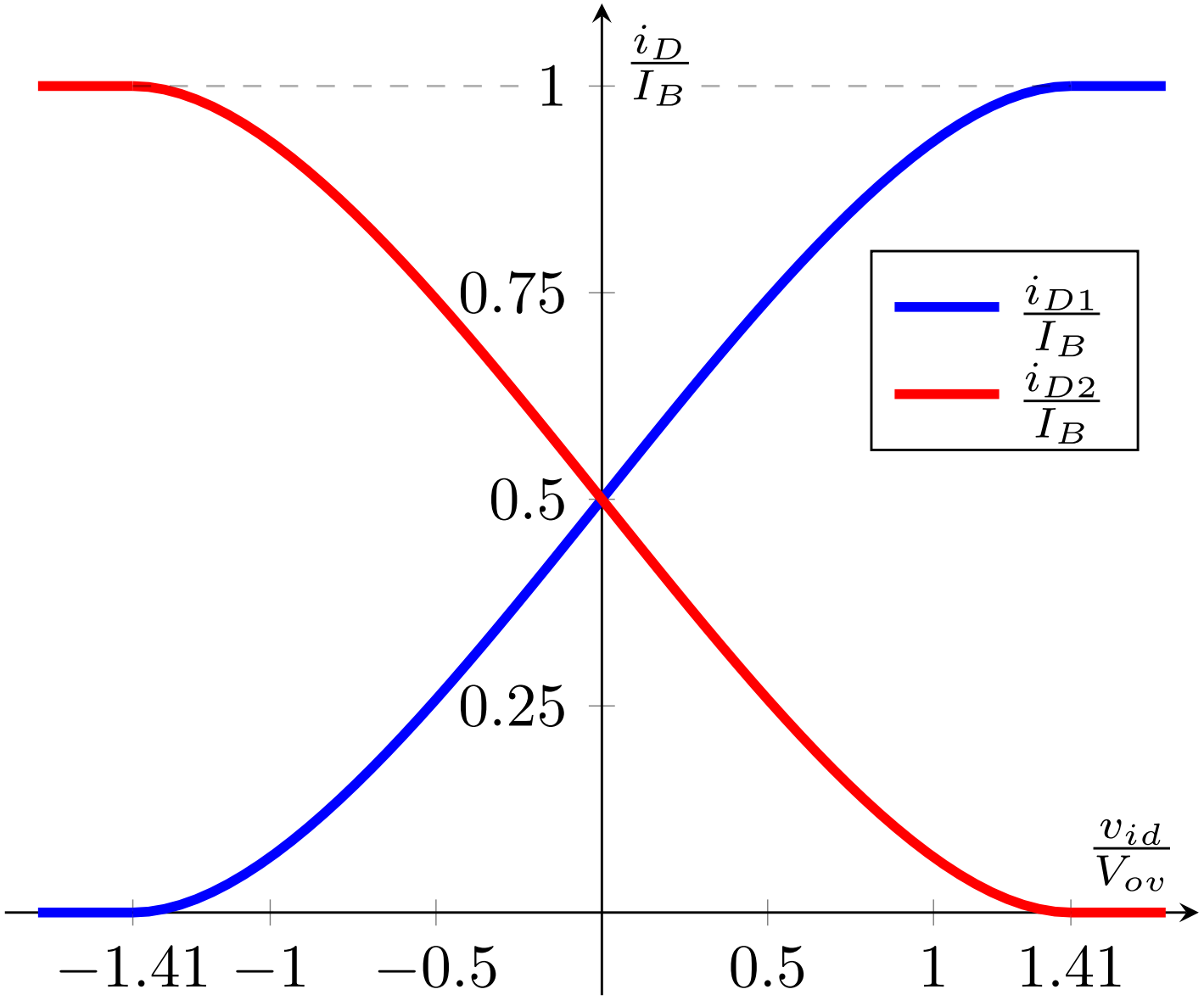
Diff Pair - Large Signal - Diff Input



Diff Pair - Large Signal - Diff Input

- if $v_{id} \gg 0$
  - All I_B flows through M_1
- if $v_{id} \ll 0$
  - All I_B flows through M_2
- At what v_{id} does M_2 "just" turn off
  - If $i_{D2} \approx 0$, $V_{GS2} = V_{tn}$ so $V_S = -V_{tn}$ since $V_{G2} = 0$
  - $V'_{GS1} = V_{tn} + V'_{ov}$ where V'_{ov} is overdrive voltage when $I_D = I_B$
  - V_{ov} is the overdrive voltage when $I_D = I_B/2$
  - $V'_{ov} = \sqrt{2I_B/(\mu_n C_{ox}(W/L))}$
  - $V'_{ov} = \sqrt{2}V_{ov}$
  - $v_{id} = V_S + v_{GS1}$
  - $v_{id,max} = -V_{tn} + V_{tn} + V'_{ov} = \sqrt{2}V_{ov}$
  - So $I_{D2} = 0$ for $v_{id} > v_{id,max}$
  - Similarily, $I_{D1} = 0$ for $v_{id} < -v_{id,max}$

Diff Pair - Large Signal - Diff Input



Diff Pair - Large Signal - Diff Input

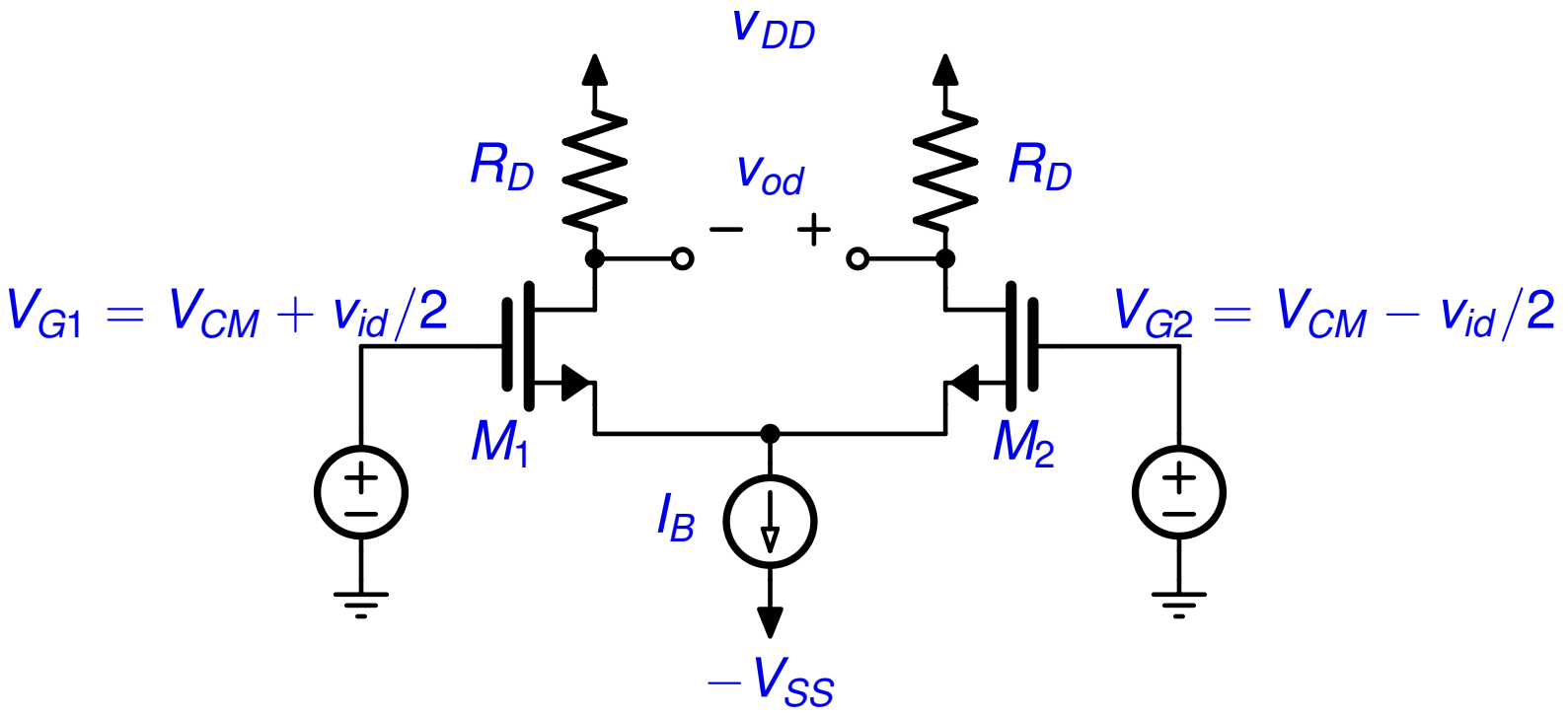
- Can show

$$i_{D1} = \frac{I_B}{2} + \left(\frac{I_B}{V_{ov}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{ov}}\right)^2}$$

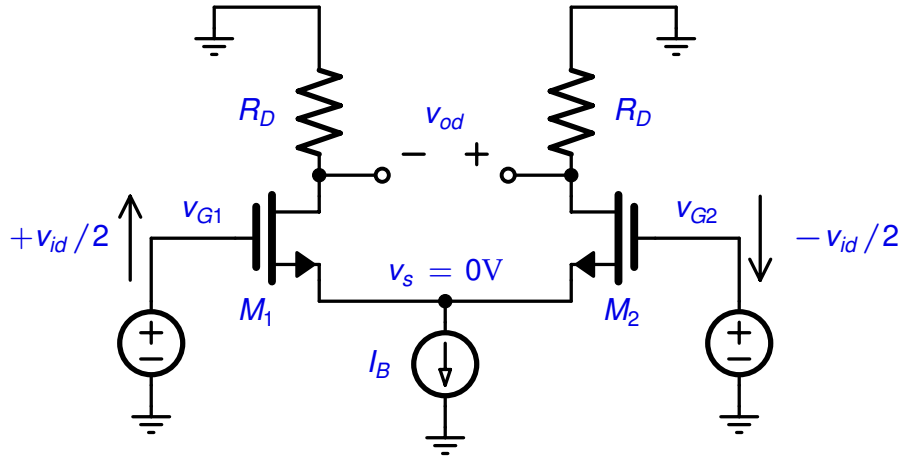
$$i_{D2} = \frac{I_B}{2} - \left(\frac{I_B}{V_{ov}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{ov}}\right)^2}$$

- For $v_{id} \approx 0$, i_d is roughly linear equation
- More non-linear as v_{id} increases

Diff Pair - Small-Signal

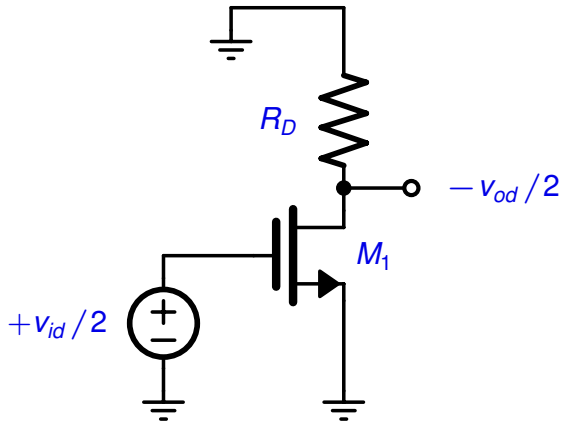


Small-Signal - Balanced



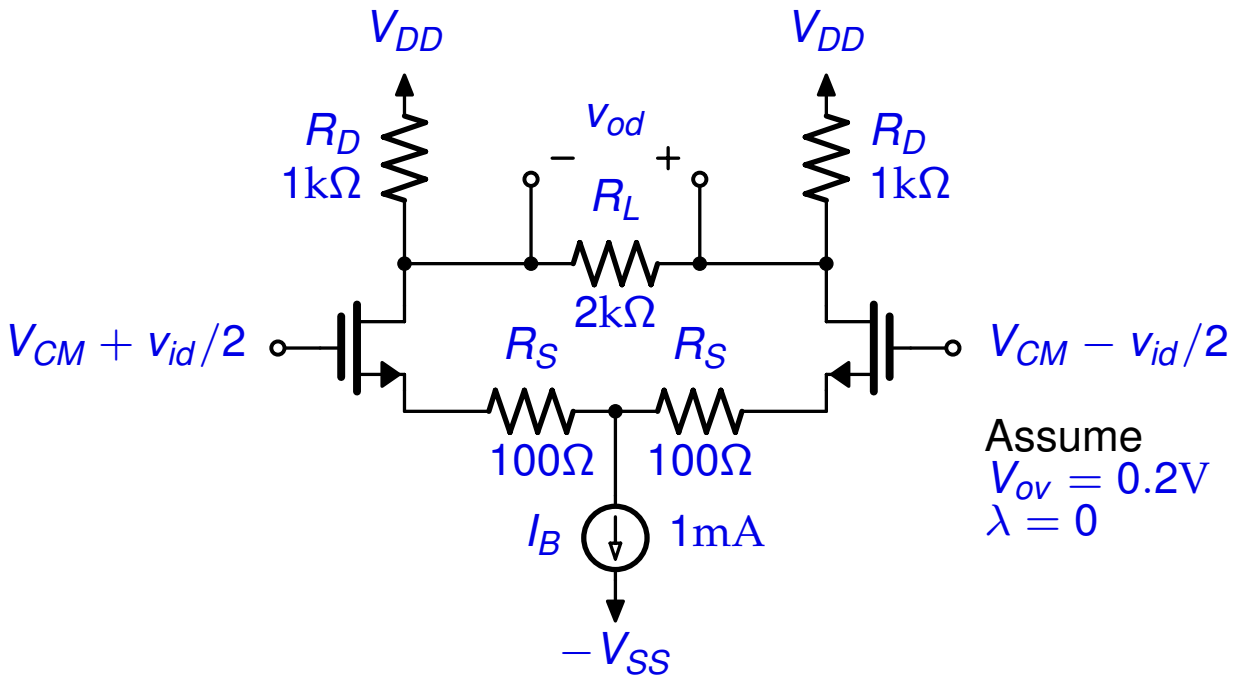
- IF circuit is **balanced**
- Diff input applied
  - v_{G1} goes up while v_{G2} goes down the same amount
  - Results in $v_s = 0\text{V}$
- Can do our analysis with half-circuit

Small-Signal - Balanced



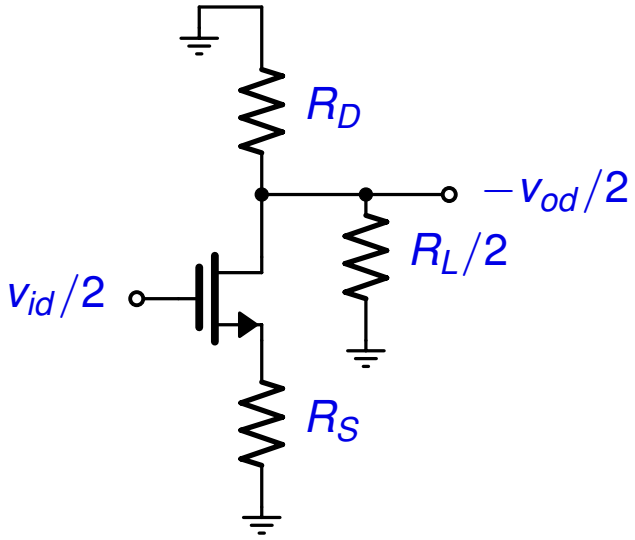
- Above is half circuit
- $-v_{od}/2 = -g_{m1}(r_{o1}||R_D)(v_{id}/2)$
- $v_{od}/v_{id} = g_{m1}(r_{o1}||R_D)$
- Recall that M_1/M_2 are matched
  - $g_{m1} = g_{m2}$ and $r_{o1} = r_{o2}$

Example - Balanced



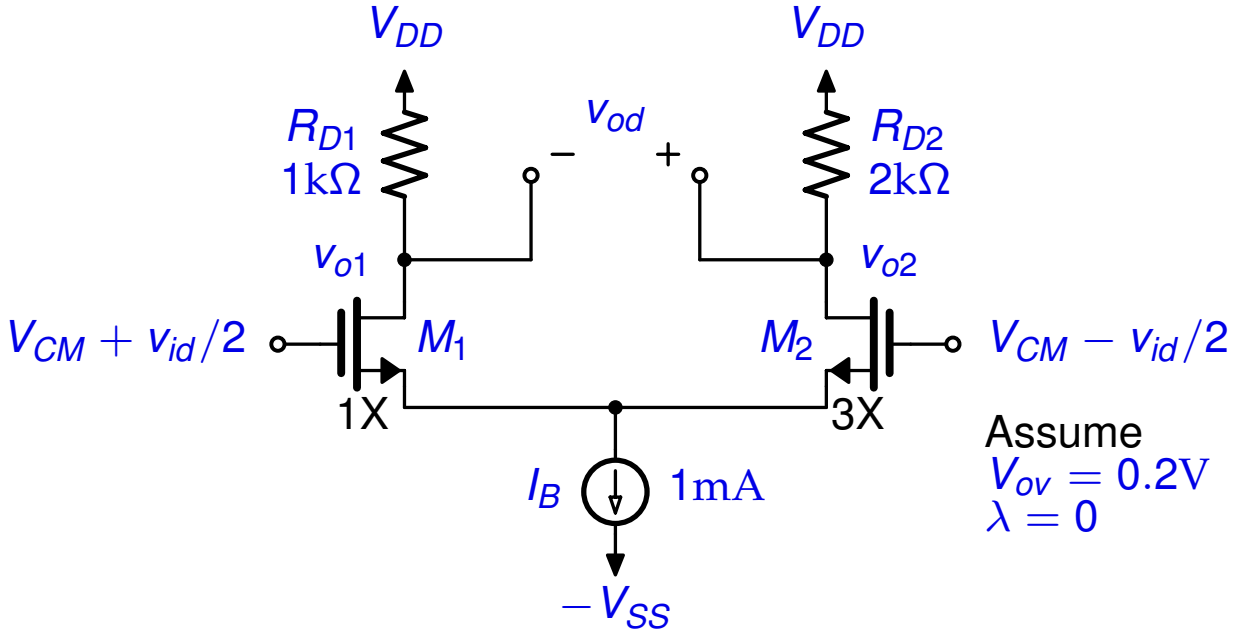
- $g_m = 2I_D/V_{ov} = 2(I_B/2)/V_{ov} = 5\text{mA/V}$
- $r_o \to \infty$
- For half circuit, split R_L into 2 $1\text{k}\Omega$

Example - Balanced



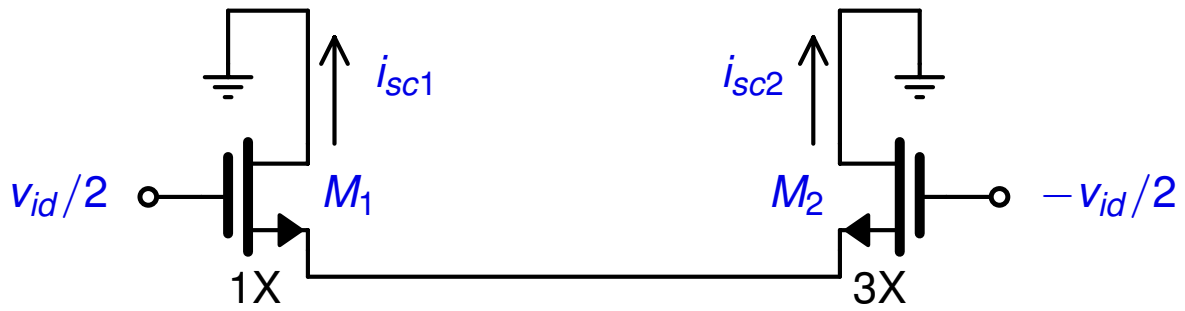
- $R_o = (R_L/2)||R_D = 500\ \Omega$
- $G_m = \frac{-1}{(1/g_m)+R_S} = \frac{-1}{300}\ \mathrm{A/V}$
- $(-v_{od}/2)/(v_{id}/2) = G_m R_o = -1.67\ \mathrm{V/V}$
- $v_{od}/v_{id} = 1.67\ \mathrm{V/V}$

Small-Signal - UnBalanced



- 3X implies M_2 is 3 times W/L compared to 1X M_1
- $I_{D2} = 3I_{D1}$ and $I_{D1} + I_{D2} = 1\text{mA}$
  - $I_{D2} = 0.75\text{mA},\ I_{D1} = 0.25\text{mA}$
  - $g_{m2} = 7.5\text{mA/V}$ and $g_{m1} = 2.5\text{mA/V}$
  - $r_o \to \infty$

Small-Signal - UnBalanced

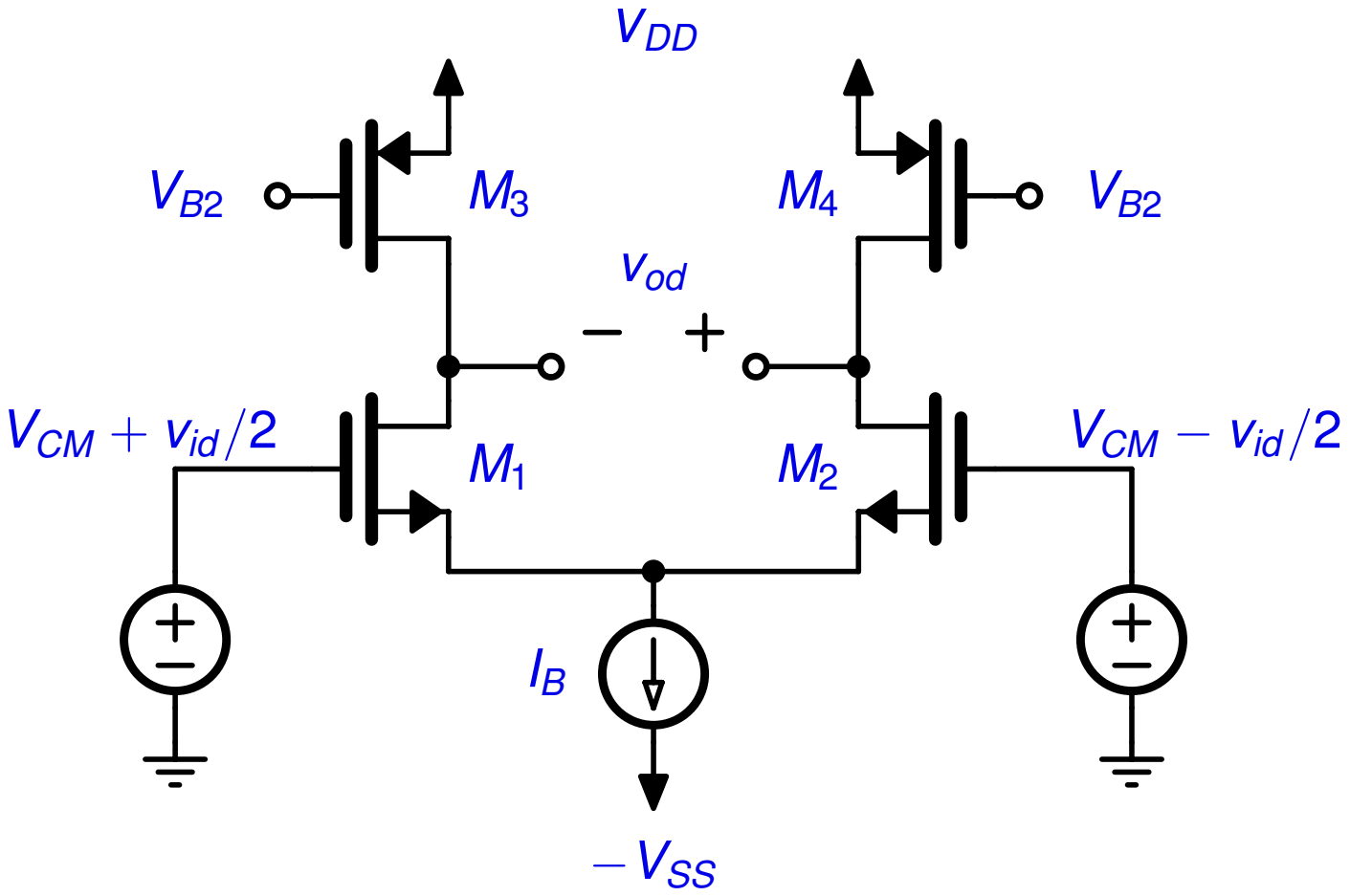


- Use superposition
  - Find i'_{sc1} and i'_{sc2} due to $v_{id}/2$ while $-v_{id}/2 = 0$
  - Find i''_{sc1} and i''_{sc2} due to $-v_{id}/2$ while $v_{id}/2 = 0$
  - $i_{sc1} = i'_{sc1} + i''_{sc1} \qquad i_{sc2} = i'_{sc2} + i''_{sc2}$
  - These 2 currents go into the 2 load resistors so ...
  - $v_{od} = i_{sc2} R_{D2} - i_{sc1} R_{D1}$

Small-Signal - UnBalanced

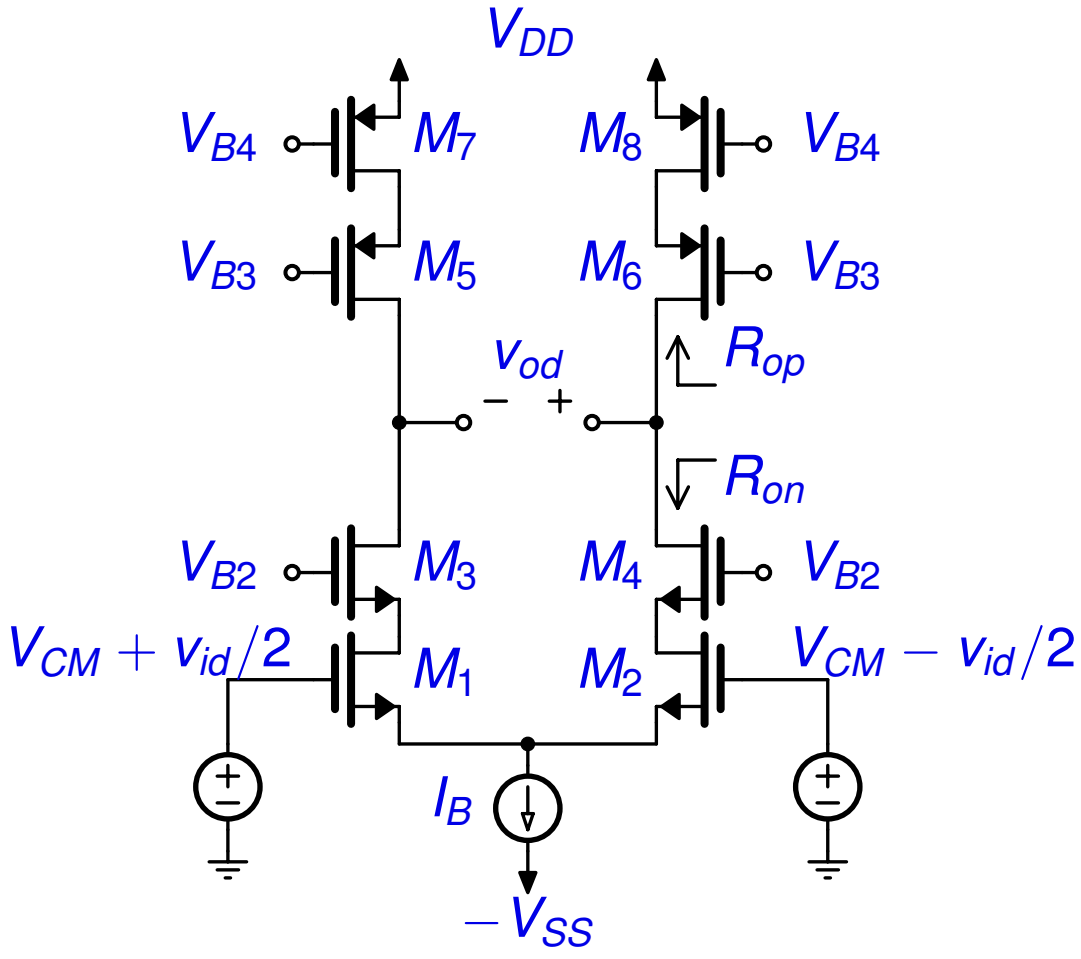
- $i'_{sc1} = \frac{-v_{id}/2}{1/g_{m1}+1/g_{m2}} = -i'_{sc2}$
- $i''_{sc2} = \frac{-(-v_{id}/2)}{1/g_{m1}+1/g_{m2}} = -i''_{sc1}$
- $i_{sc1} = \frac{-v_{id}}{1/g_{m1}+1/g_{m2}} = 1.875e-3(-v_{id})$
- $i_{sc2} = \frac{v_{id}}{1/g_{m1}+1/g_{m2}} = 1.875e-3(v_{id})$
- In general, with an unbalanced diff pair
  - $i_{sc1} = -i_{sc2} = \frac{-v_{id}}{1/g_{m1}+1/g_{m2}}$
- $v_{od} = i_{sc2}(2e3) - i_{sc1}(1e3) = 5.625 v_{id}$
- $v_{od}/v_{id} = 5.625\ \mathrm{V/V}$
- Note that this is a very unusual case as the voltage swing at v_{o2} is twice that at v_{o1} and this is generally undesirable.

Diff Pair - Current Source Loads



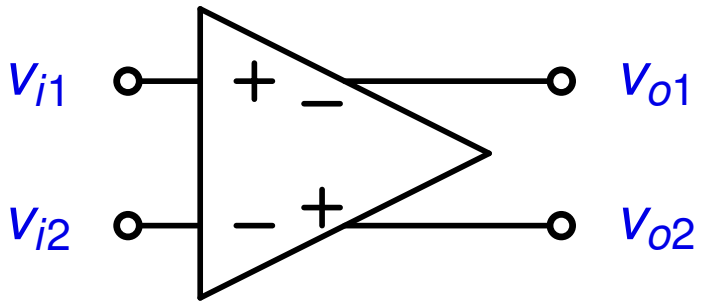
- $v_{od}/v_{id} = g_{m1}(r_{o1}||r_{o3})$

Diff Pair - Current Source Loads



- $v_{od}/v_{id} \approx g_{m1}(R_{op}||R_{on})$
- $R_{on} \approx (g_{m3}r_{o3})r_{o1}$ $\quad$ $R_{op} \approx (g_{m5}r_{o5})r_{o7}$

Diff Amp - Various Gains



Fully Diff Amplifier

$$v_{i1} = V_{CMi} + v_{id}/2$$
$$v_{i2} = V_{CMi} - v_{id}/2$$
$$v_{id} = v_{i1} - v_{i2}$$
$$V_{CMi} = \frac{v_{i1}+v_{i2}}{2}$$

$$v_{o1} = V_{CMo} - v_{od}/2$$
$$v_{o2} = V_{CMo} + v_{id}/2$$
$$v_{od} = v_{o2} - v_{o1}$$
$$V_{CMo} = \frac{v_{o1}+v_{o2}}{2}$$

- We can define 4 gains through the amplifier

Diff Amp - Various Gains

- Differential Gain
  $A_d \equiv \frac{v_{od}}{v_{id}}$
  - This is what we are **MOST** interested in
- Common-mode-to-differential gain
  $A_{CM} \equiv \frac{v_{od}}{v_{cmi}}$
  - Common-mode "signals" may convert to differential signal
    This would result in "noise" in the differential signal
- Common-mode-to-common-mode gain
  - $A_{cm-cm} \equiv \frac{v_{cmo}}{v_{cmi}}$
  - Generally not too critical but we want it less than 1 so we do not amplify common-mode signals
- Differential-to-common-mode gain
  - $A_{d-cm} \equiv \frac{v_{cmo}}{v_{id}}$
  - Generally not an issue to worry about so generally not looked at

Diff Amp - Various Gains

- Most important are A_d and A_{CM}
- Want $A_d \gg A_{CM}$
  - So common-mode signals are rejected relative to diff signals
- Define common-mode rejection ratio (CMRR)

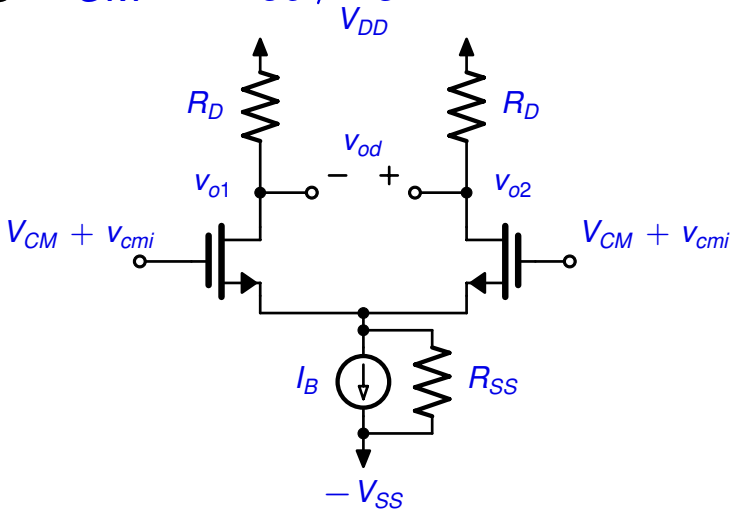
  $CMRR \equiv \frac{|A_d|}{|A_{CM}|}$

  or in dB form

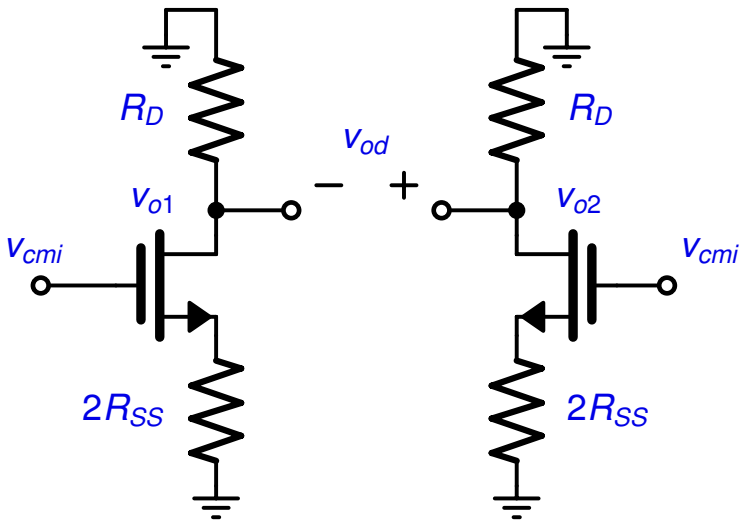
  $CMRR_{dB} \equiv 20log(\frac{|A_d|}{|A_{CM}|})$
- Want a high $CMRR$ value

Common-mode to Diff Gain - A_{CM}

- Circuit for finding $A_{CM} \equiv v_{od}/v_{cmi}$



- Half circuits

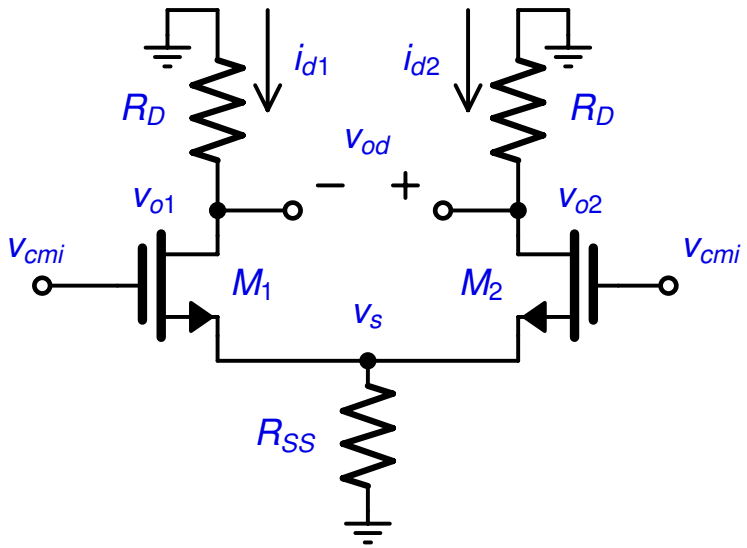


Common-mode to Diff Gain - A_{CM}

- Let $\lambda \to \infty$
- Recall $A_d = v_{od}/v_{id} = g_m R_D$
- $\frac{v_{o1}}{v_{cmi}} = \frac{v_{o2}}{v_{cmi}} = \frac{-R_D}{(1/g_m)+2R_{SS}}$
- If perfectly matched
  - $v_{od} = v_{o2} - v_{o1} = 0 \quad \Rightarrow \quad A_{CM} = 0$
- Resistors mismatched by ΔR_D
  - We can still used the half circuit here since the lower half of the circuit is still perfectly matched (only R_D are mismatched)
  - $R_{D1} = R_D \qquad R_{D2} = R_D + \Delta R_D$
  - $\frac{v_{o1}}{v_{cmi}} = \frac{-R_D}{(1/g_m)+2R_{SS}} \qquad \frac{v_{o2}}{v_{cmi}} = \frac{-(R_D+\Delta R_D)}{(1/g_m)+2R_{SS}}$
  - $A_{CM} = \frac{v_{o2}-v_{o1}}{v_{cmi}} = \frac{-\Delta R_D}{(1/g_m)+2R_{SS}}$
  - $A_{CM} = -\left(\frac{g_m R_D}{1+2g_m R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right)$
  - $CMRR_R = \frac{(1+2g_m R_{SS})}{(\Delta R_D/R_D)}$
  - To increase CMRR, increase g_m or R_{SS} or reduce ΔR_D

Common-mode to Diff Gain - A_{CM}

- Transistors g_m mismatched by Δg_m
- We can not use half circuits as the circuit is no longer balanced
- $g_{m1} = g_m + \Delta g_m/2 \qquad g_{m2} = g_m - \Delta g_m/2$



- $v_s = \frac{R_{SS}}{R_{SS}+1/(2g_m)} v_{cmi} \qquad i_{d1} + i_{d2} = v_s/R_{SS} = \frac{v_{cmi}}{R_{SS}+1/(2g_m)}$

Common-mode to Diff Gain - A_{CM}

- $i_{d1} = g_{m1} v_{gs1} \qquad i_{d2} = g_{m2} v_{gs2}$
- Since $v_{gs1} = v_{gs2}$, we have

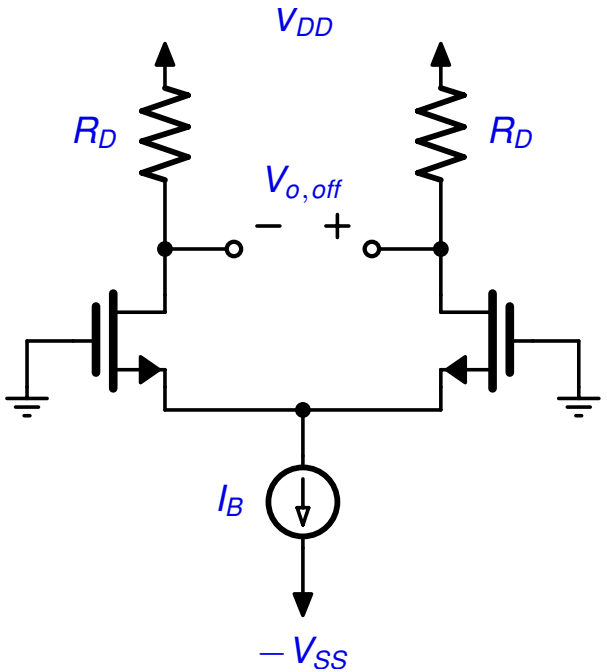
  $\frac{i_{d1}}{i_{d2}} = \frac{g_{m1}}{g_{m2}}$
- Combining the above equations, we have
- $i_{d1} = \frac{g_{m1} v_{cmi}}{1+2g_m R_{SS}} \qquad i_{d2} = \frac{g_{m2} v_{cmi}}{1+2g_m R_{SS}}$
- $v_{od} = v_{o2} - v_{o1} = -i_{d2} R_D - (-i_{d1} R_D) = \frac{(g_{m1}-g_{m2}) R_D v_{cmi}}{1+2g_m R_{SS}}$
- $A_{CM} = v_{od}/v_{cmi} = \frac{\Delta g_m R_D}{1+2g_m R_{SS}} = \left(\frac{g_m R_D}{1+2g_m R_{SS}}\right)\left(\frac{\Delta g_m}{g_m}\right)$
- $CMRR_{gm} = \frac{(1+2g_m R_{SS})}{(\Delta g_m/g_m)}$
- To increase CMRR, increase g_m or R_{SS} or reduce Δg_m

Common-mode to common-mode Gain - A_{CM-CM}

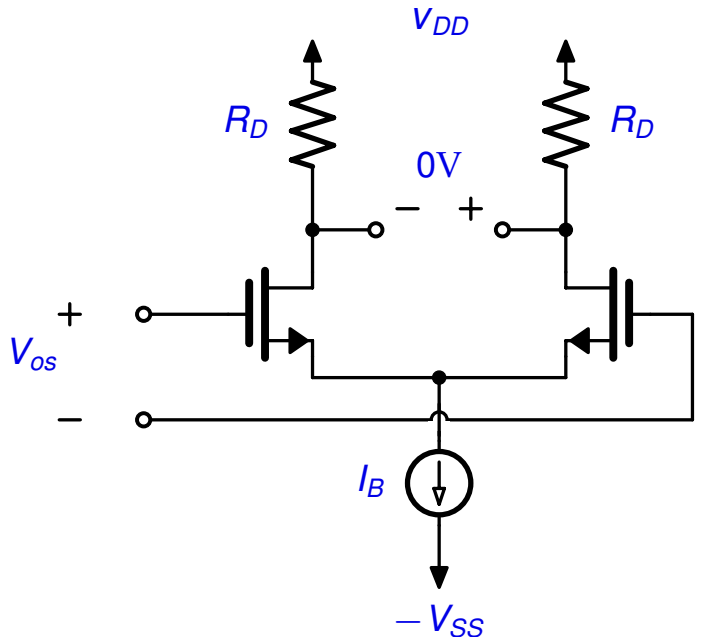
- From our original half circuit, we found
- $\frac{v_{o1}}{v_{cmi}} = \frac{v_{o2}}{v_{cmi}} = \frac{-R_D}{(1/g_m)+2R_{SS}}$
- This is also our common-mode to common-mode gain so
- $A_{CM-CM} = \frac{-R_D}{(1/g_m)+2R_{SS}}$
- To reduce our common-mode to common-mode gain, we can increase R_{SS} or decrease g_m or R_D
  - Increasing R_{SS} is a better choice as it helps with the CMRR
  - Decreasing g_m or R_D also decreases our diff gain

Input Offset of Amp with Diff Input

- The input offset is the dc voltage value, V_{os}, that when applied to the input of an amplifier will result in the output voltage being zero.
- V_{os} input offset for $V_o = 0$
- $V_{o,off}$ is the output offset for $v_{id} = 0$
- If in the linear range of the amp
  - $V_{os} = V_{o,off}/A_d$ where A_d is the gain of the amp



Input Offset of Diff Pair



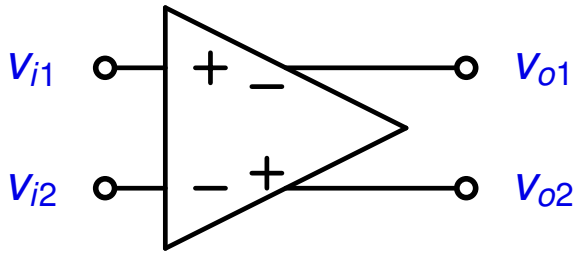
- Offset due to mismatch for $R_D, (W/L), V_{tn}$
- Without showing the derivation, the input offset is ...

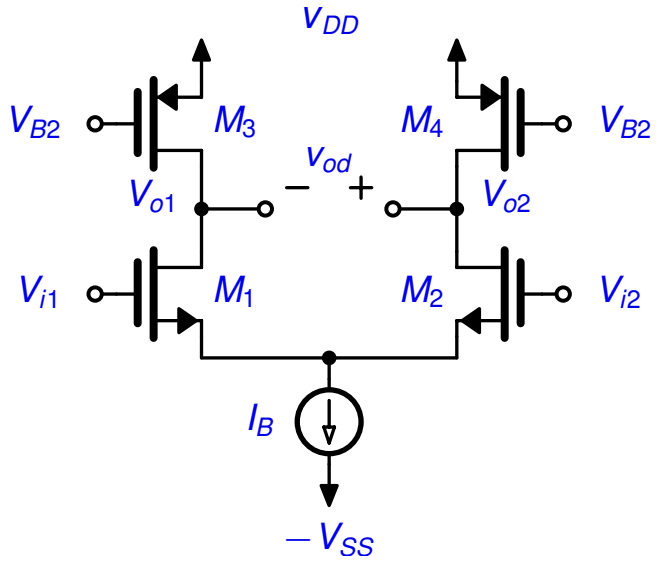
Input Offset of Diff Pair

- For ΔV_{tn}
  - Usually ΔV_{tn} is the dominant cause for offset
  - $V_{os} = \Delta V_{tn}$
  - Typical values for ΔV_{tn} from $1 \rightarrow 10\ \mathrm{mV}$
- For ΔR_D
  - $V_{os} = \left(\frac{V_{ov}}{2}\right)\left(\frac{\Delta R_D}{R_D}\right)$
- For $\Delta(W/L)$
  - $V_{os} = \left(\frac{V_{ov}}{2}\right)\left(\frac{\Delta(W/L)}{(W/L)}\right)$

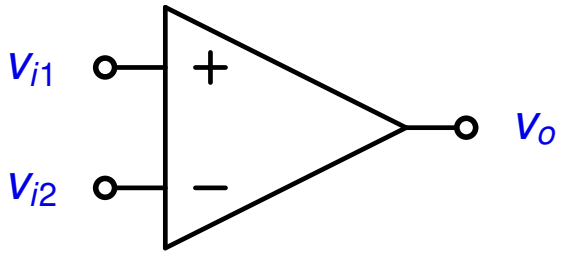
Amplifiers (First Stage)

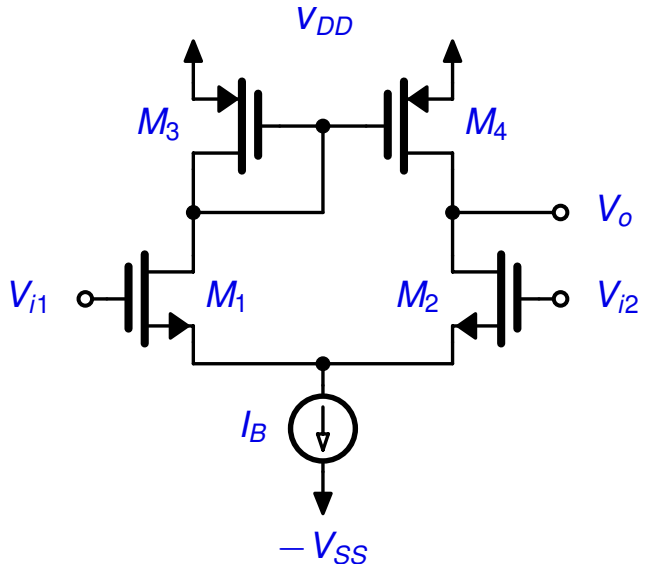
- Diff-Diff Amplifier (fully differential)





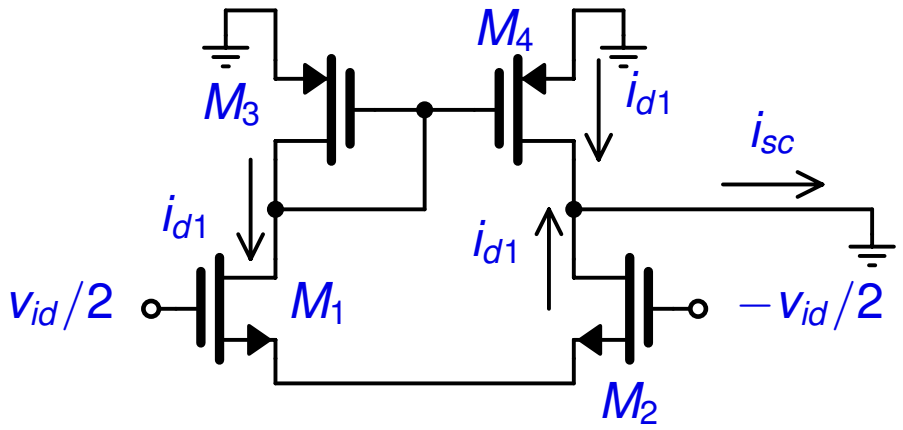
- Diff-Single Ended Amplifier





Diff-Single Ended Amplifier (First Stage)

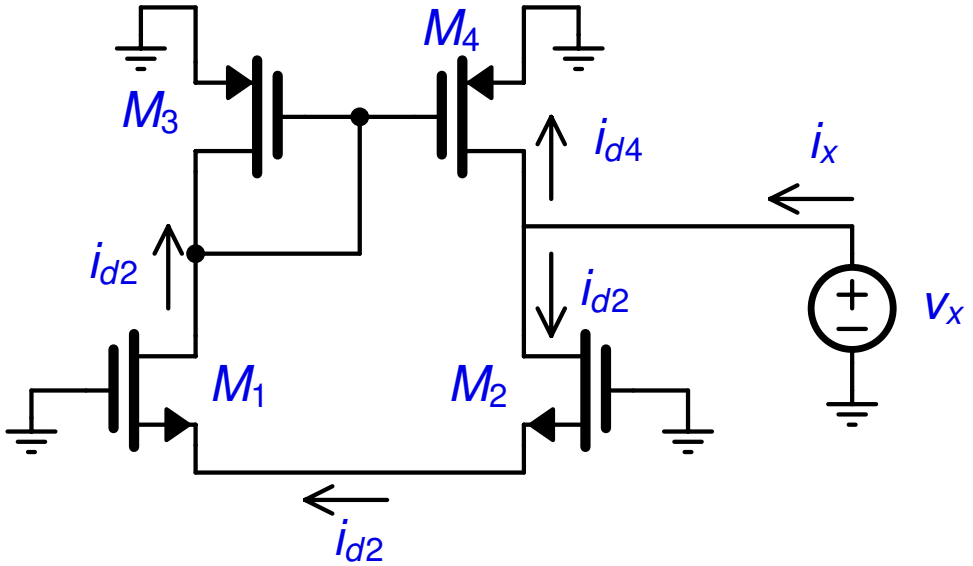
- To find gain of first stage - find G_m and R_o
- For G_m



- $i_{d1} = g_{m1}(v_{id}/2)$
- $i_{sc} = 2i_{d1} = g_{m1}v_{id}$

Diff-Single Ended Amplifier (First Stage)

- For R_o



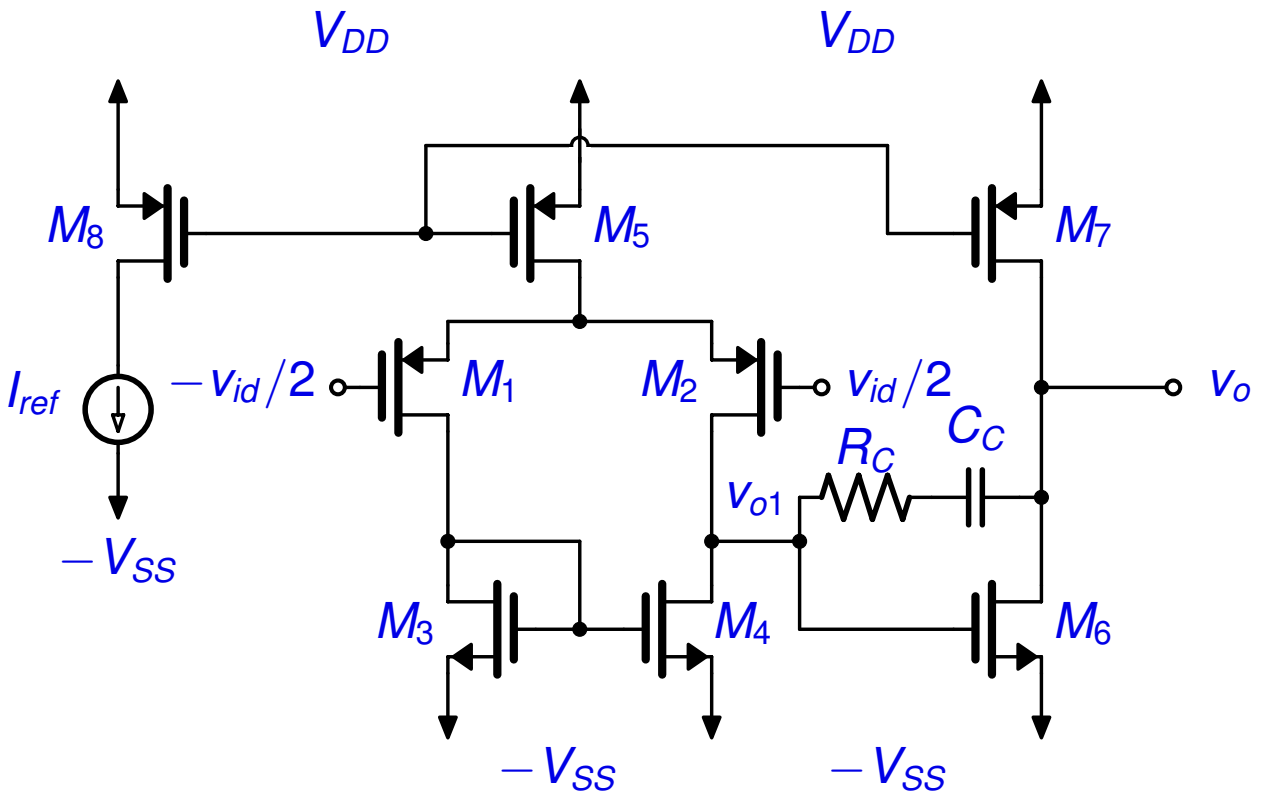
- Due to the current mirror
- $i_{d4} = v_x / r_{o4} + i_{d2}$
- $i_{d2} = v_x / R_{d2}$

Diff-Single Ended Amplifier (First Stage)

- Impedance $R_{d2} = 2r_{o2}$ is found by ...
  - Impedance of diode connected M_3 is approx $1/g_{m3}$
  - $R_{s1} \approx (1/g_{m1}) + (1/g_{m3})/(g_{m1}r_{o1}) \approx 1/g_{m1}$
  - $R_{d2} \approx (1 + g_{m2}R_{s2})r_{o2} \approx (1 + \frac{g_{m2}}{g_{m1}})r_{o2} \approx 2r_{o2}$
- $i_x = i_{d4} + i_{d2} = v_x/r_{o4} + v_x/(2r_{o2}) + v_x/(2r_{o2})$
- $i_x = v_x/r_{o4} + v_x/r_{o2}$
- $R_o = v_x/i_x = r_{o2}||r_{o4}$
- So the gain is

  $v_o/v_{id} = g_{m1}(r_{o2}||r_{o4})$ where $v_{id} = v_{i1} - v_{i2}$

2 Stage CMOS Opamp



- R_C and C_C are used for stability when feedback is used
  - For low freq gain, we assume C_C is an open circuit
- $A_1 = v_{o1}/v_{id} = -g_{m1}(r_{o2}||r_{o4})$ $\quad A_2 = v_o/v_{o1} = -g_{m6}(r_{o6}||r_{07})$
- Overall gain: $v_o/v_{id} = A_1 A_2$

2 Stage CMOS Opamp

- Random dc offset
  - Random offset will result in approx $1 - 10\ \mathrm{mV}$ of input offset
- Systematic dc offset
  - Even if all transistors are matched, systematic offset may occur depending on bias currents
  - For ZERO systematic offset

$$\frac{(W/L)_6}{(W/L)_3} = 2\frac{(W/L)_7}{(W/L)_5} \tag{1}$$

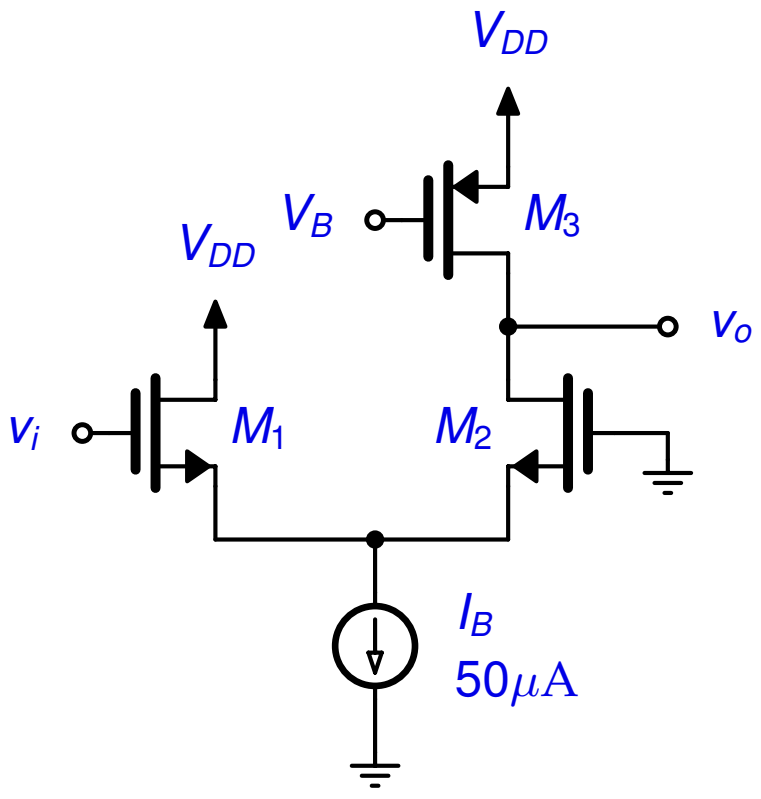
- Proof:
  - Let $V_{id} = 0$
  - $I_{D3} = I_{D4} = I_{D5}/2$ and since $V_{GS3} = V_{GS4}$, then $V_{DS4} = V_{DS3} = V_{GS6}$
  - $V_{GS6} = V_{GS3}$ means that I_{D6} is a current mirror of the current I_{D3}

2 Stage CMOS Opamp

- $I_{D6} = (W/L)_6/(W/L)_3 \times (I_{D5}/2)$
- For no systematic offset, $I_{D7} = I_{D6}$
- $I_{D7} = (W/L)_7/(W/L)_5 \times I_{D5}$
- Combining the above, we have
- $I_{D7} = I_{D6}$
- $(W/L)_7/(W/L)_5 \times I_{D5} = (W/L)_6/(W/L)_3 \times (I_{D5}/2)$
- Dividing both sides by I_{D5} we have
- $2(W/L)_7/(W/L)_5 = (W/L)_6/(W/L)_3$

- For good current matching
  - the lengths of $M_5/M_7/M_8$ should be the same
  - the lengths of $M_3/M_4/M_6$ should be the same

Diff Amp Example



$\mu_n C_{ox} = 240\mu\text{A/V}^2$
$V_{tn} = 0.3\text{V}$
$\mu_p C_{ox} = 60\mu\text{A/V}^2$
$\lambda' = 100\text{nm/V}$
$W_1 = 2\mu\text{m}$
$W_2 = 1\mu\text{m}$
$W_3 = 2\mu\text{m}$
All $L = 200\text{nm}$
V_B chosen so $I_{D3} = I_{D2}$

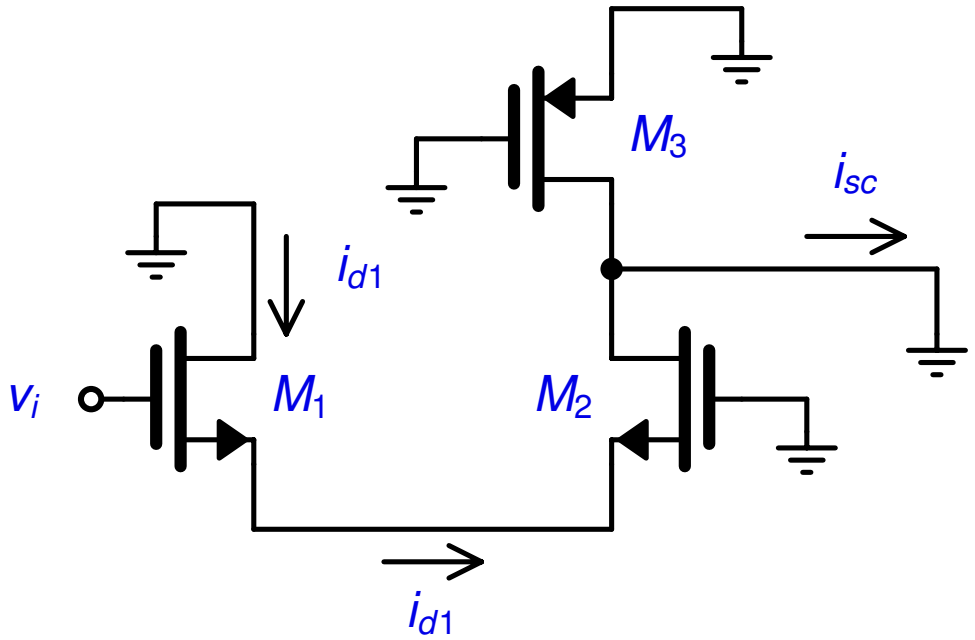
- Find v_o/v_i and R_{out}
  - For i_{sc}, make the approximation that all $r_o \to \infty$

Diff Amp Example

- First we do dc analysis
  - $I_{D1} = 2I_{D2}$ $\quad I_{D1} + I_{D2} = I_B = 50\mu\text{A}$
  - Combining, we have
  - $I_{D2} = I_B/3 = 16.67\mu\text{A}$ $\quad I_{D1} = 2I_{D2} = 33.33\mu\text{A}$
  - $I_{D3} = I_{D2} = 16.67\mu\text{A}$
  - $g_{m1} = \sqrt{2\mu_n C_{ox}(W_1/L)I_{D1}} = 400\mu\text{A/V}$
  - $r_{o1} = L/(\lambda' I_{D1}) = 60\text{k}\Omega$
  - $g_{m2} = \sqrt{2\mu_n C_{ox}(W_2/L)I_{D2}} = 200\mu\text{A/V}$
  - $r_{o2} = L/(\lambda' I_{D2}) = 120\text{k}\Omega$
  - $r_{o3} = L/(\lambda' I_{D3}) = 120\text{k}\Omega$

Diff Amp Example

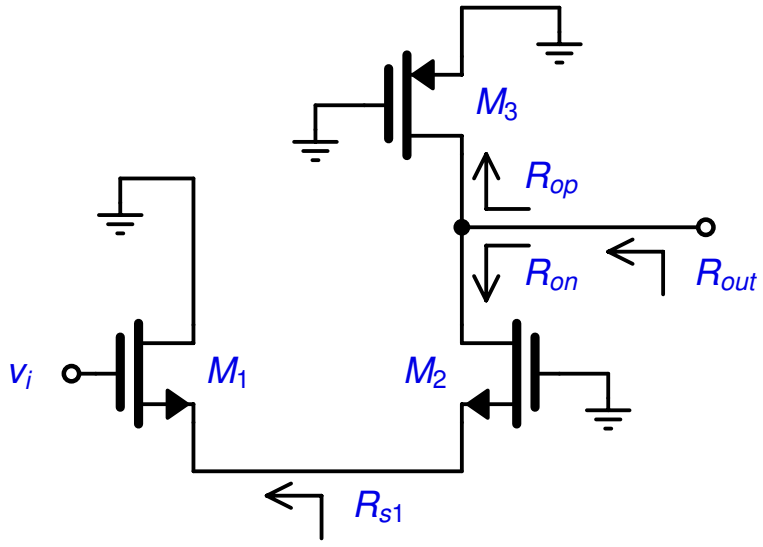
- For i_{sc}, we have the following circuit



  - $i_{sc} = i_{d1} = G_m v_i$
  - $G_m = \frac{1}{(1/g_{m1})+(1/g_{m2})} = 133.3\mu\text{A/V}$

Diff Amp Example

- For R_{out}, we have the following circuit



  - $R_{s1} = ((1/g_{m1})||r_{o1}) = 2.4\text{k}\Omega$
  - $R_{on} = r_{o2} + (1 + g_{m2}r_{o2})R_{s1} = 180\text{k}\Omega$
  - $R_{op} = r_{o3} = 120\text{k}\Omega$
  - $R_{out} = R_{on}||R_{op} = 72\text{k}\Omega$
  - $v_o/v_i = G_m R_{out} = 9.6\text{V/V}$

Topics Covered

- Differential signals
- Diff amps
- Diff pair
  - Large signal
  - Small signal (balanced and unbalanced)
- Diff pair current source loads
- Diff amps - 4 gains through amp
- Input offset
- 2 stage CMOS opamp