MOSFET Caps and Miller's Theorem

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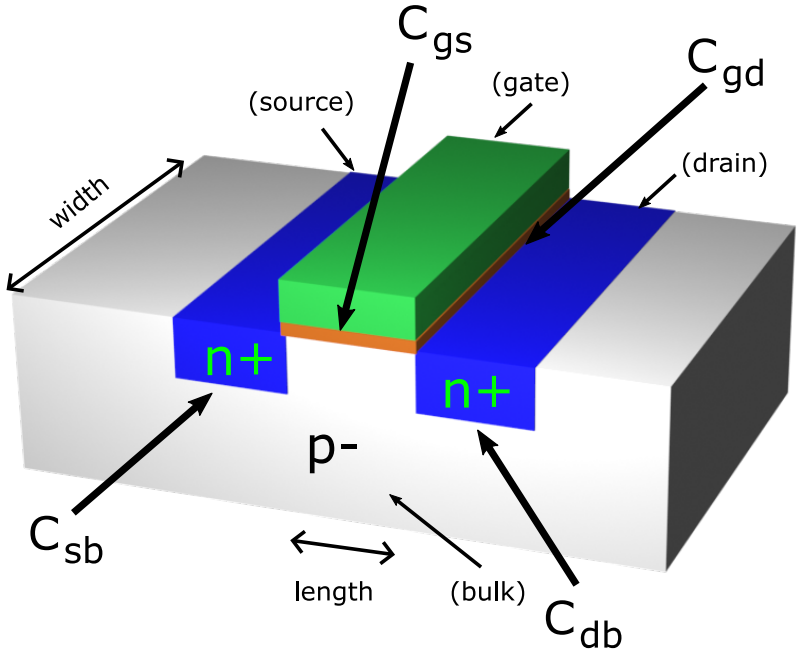
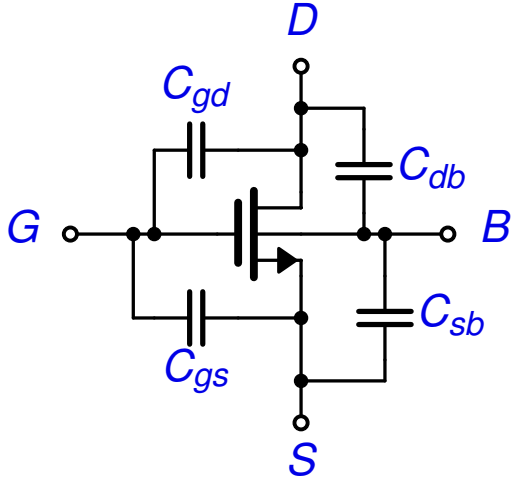
High Frequency Cutoff

- For HF cutoff
  - Some capacitors might be added to reduce bandwidth (say, for noise reduction)
  - However, there are also **parasitic** capacitors that always occur that limits high freq bandwith
  - There is also parasitic inductances but these are generally small enough to be ignored in many circuits
- Parasitic capacitor examples
  - Wiring capacitances
    (there is capacitance between any 2 conductors)
  - Transistor internal capacitances
- MOSFET transistor parasitic capacitances
  - C_{gs}, C_{gd}: they are inherent to the operation of the transistor
    Not possible to ever be zero
  - C_{db}, C_{sb}: depend on the drain/source region area

MOSFET Capacitor Model





MOSFET Capacitor Model

- **ACTIVE REGION**

$$C_{gs} = \left(\frac{2}{3}\right) WLC_{ox} + WL_{ov}C_{ox} \tag{1}$$

$$C_{gd} = WL_{ov}C_{ox} \tag{2}$$

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + (V_{db}/V_0)}} \qquad C_{sb} = \frac{C_{sb0}}{\sqrt{1 + (V_{sb}/V_0)}} \tag{3}$$

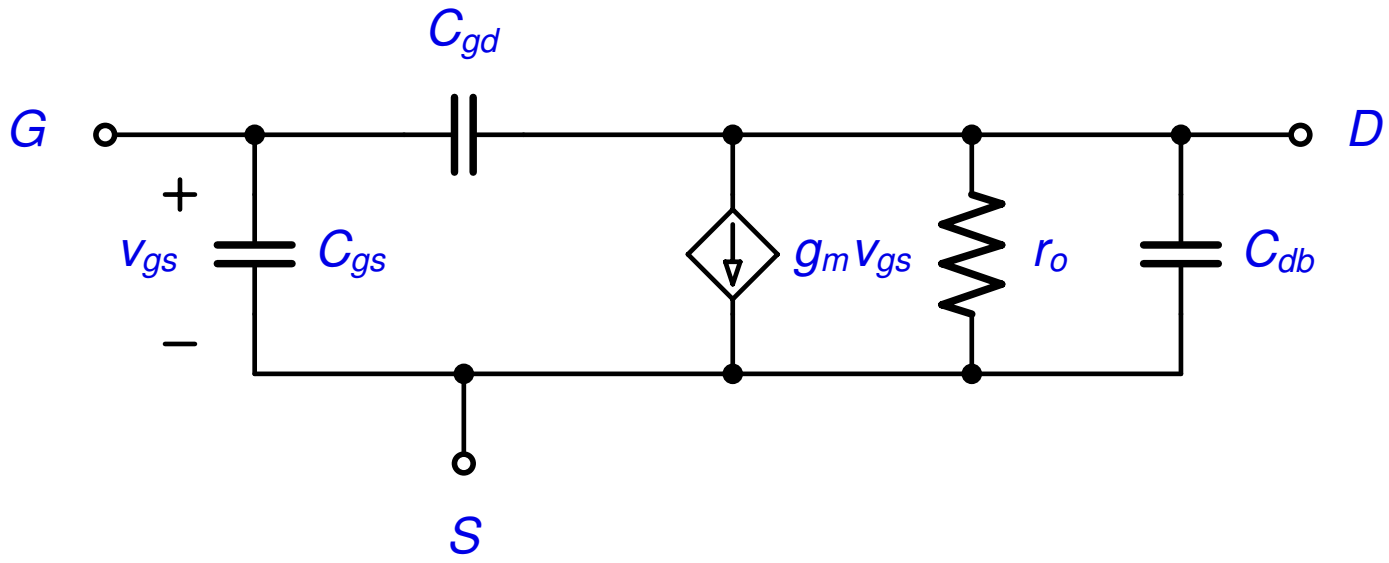
- C_{ox} is the gate capacitance per unit area
- $\left(\frac{2}{3}\right) WLC_{ox}$ is capacitance under the gate to the channel which is connected to the source when in the active region
- $\left(\frac{2}{3}\right)$ is due the shape of the channel when in the active region (a triangle shape)
- L_{ov} is the overlap length of the gate extending over the drain/source regions

MOSFET Capacitor Model

- $WL_{ov}C_{ox}$ is the overlap capacitance
- C_{db0} is the drain to body capacitance when $V_{db} = 0$
  This value depends on the total junction surface area
- V_{db} is the reverse bias diode voltage of drain to bulk
- V_0 is the diode built-in voltage ($V_0 \approx 0.7\text{V}$)
- C_{db} value depends on the reverse bias voltage
- Similar descriptions for C_{sb}
- **TRIODE REGION**
  - C_{gd}, C_{db}, C_{sb} all the same
  - However, $C_{gs} = WLC_{ox} + WL_{ov}C_{ox}$
    since channel is now rectangular shaped

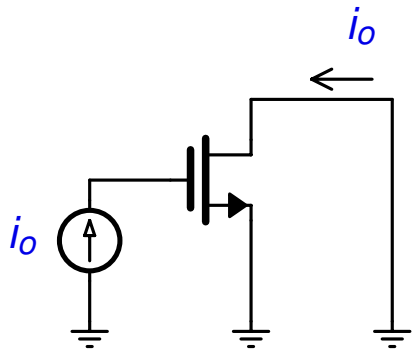
Active Region Small Signal Model with Caps

- Assuming $V_{sb} = 0$ (bulk tied to source)



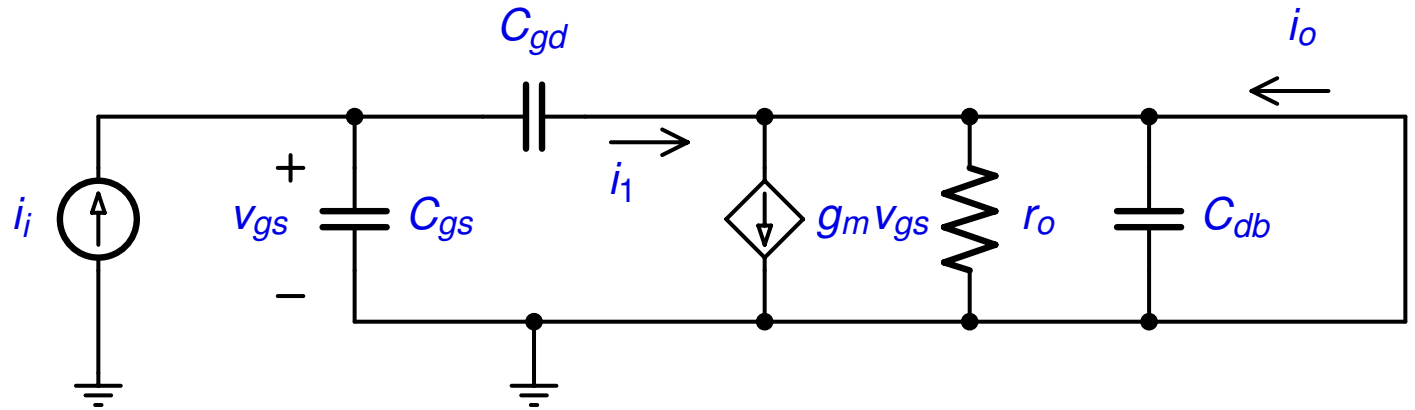
- Would like a figure of merit for transistor speed
- **Unity-Gain Frequency** (f_T)
  - Where the short circuit current gain = 1
    Recall $\omega_T = 2\pi f_T$ (can be in Hz or rad/s)

MOSFET Unity Gain Freq



- By definition for ω_T ...

$$\left| \frac{i_o}{i_i}(j\omega_T) \right| = 1 \tag{4}$$



MOSFET Unity Gain Freq

- $i_{r_o} = 0$ and $i_{C_{db}} = 0$ since they both have zero volts across them

$$v_{gs} = i_i \left(\frac{1}{s(C_{gs} + C_{gd})} \right) \tag{5}$$

$$i_1 = \frac{v_{gs}}{\left(\frac{1}{sC_{gd}} \right)} = sC_{gd} v_{gs} \tag{6}$$

$$i_o = g_m v_{gs} - i_1 = g_m v_{gs} - sC_{gd} v_{gs} \tag{7}$$

$$i_o = (g_m - sC_{gd}) v_{gs} \tag{8}$$

- combining (5) with (8)

$$\frac{i_o}{i_i}(s) = \frac{g_m - sC_{gd}}{s(C_{gs} + C_{gd})} \tag{9}$$

MOSFET Unity Gain Freq

- Using the definition in (4)

$$\left| \frac{g_m - j\omega_T C_{gd}}{(j\omega_T)(C_{gs} + C_{gd})} \right| = 1 \tag{10}$$

$$\left| \left(\frac{g_m}{(j\omega_T)(C_{gs} + C_{gd})} \right) - \left(\frac{C_{gd}}{(C_{gs} + C_{gd})} \right) \right| = 1 \tag{11}$$

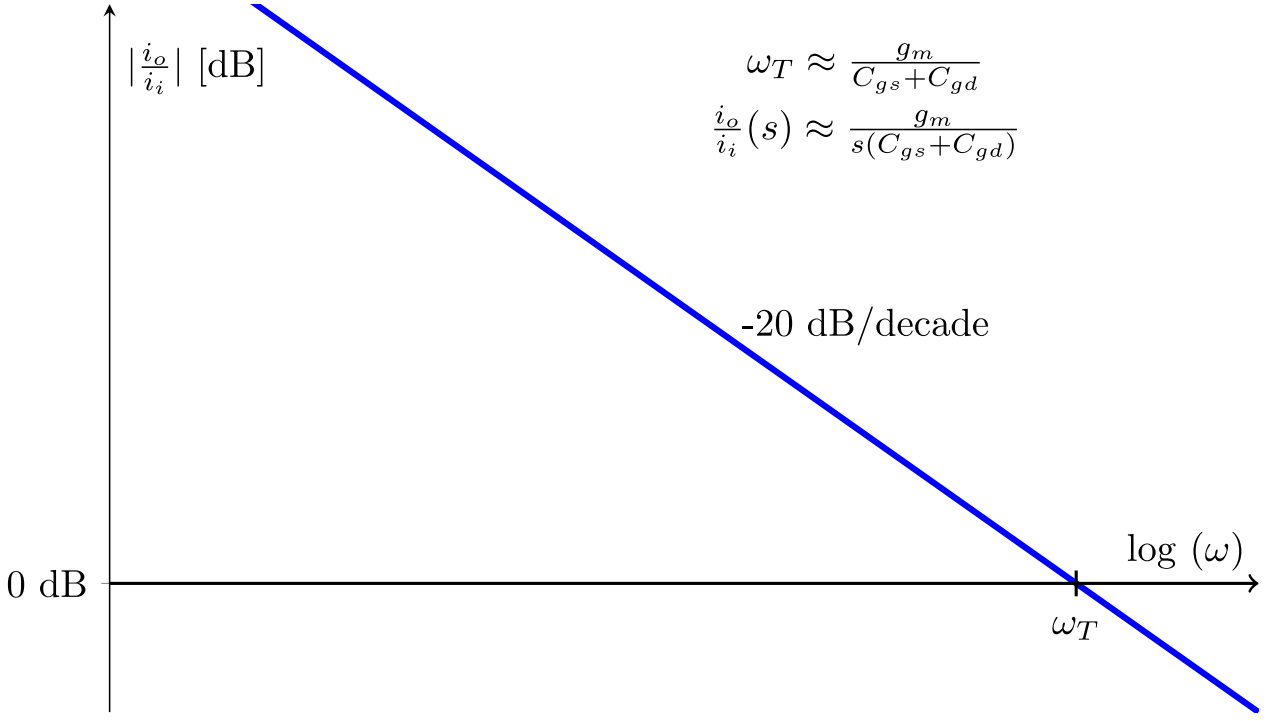
- In most technologies, $C_{gd} \ll C_{gs}$ so if we ignore the term $C_{gd}/(C_{gs} + C_{gd})$

$$\left| \left(\frac{g_m}{(j\omega_T)(C_{gs} + C_{gd})} \right) \right| \approx 1 \tag{12}$$

- solving for ω_T, we have

$$\omega_T \approx \frac{g_m}{C_{gs} + C_{gd}} \qquad f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{13}$$

MOSFET Unity Gain Freq



- How does f_T change with technology or circuit choices?
- Recall

$$g_m = \mu_n C_{ox}(W/L)V_{ov} \tag{14}$$

$$C_{gs} \approx \frac{2}{3}WLC_{ox} \tag{15}$$

MOSFET Unity Gain Freq

- If we assume $C_{gd} \ll C_{gs}$

$$f_T \approx \frac{g_m}{2\pi C_{gs}} = \frac{\mu_n C_{ox}(W/L)V_{ov}}{2\pi \frac{2}{3} WLC_{ox}} \tag{16}$$

$$\boxed{f_T \approx \frac{3\mu_n V_{ov}}{4\pi L^2}} \tag{17}$$

- f_T is ...
  - independent of W
  - proportional to $1/L^2$ and V_{ov} and μ_n
- Circuit designers can choose W, L, V_{ov} while μ_n is given for a technology

MOSFET Unity Gain Freq

- Why does the definition of f_T use current gain instead of voltage gain?
  - If an ideal voltage source drives the gate, at high frequencies, the input impedance goes to zero (due to C_{gs}) and therefore the input current would need to go to ∞
  - Also, at very high freq, the output gain would be a voltage divider between C_{gd} and C_{db}
  - It also turns out that f_T is a good estimate of the voltage gain when a transistor single transistor drives another transistor of the same size and bias conditions.
- Generally, circuits are designed to operate up to about $f_T/10$ or lower
  - So f_T is an important parameter to know when designing circuits

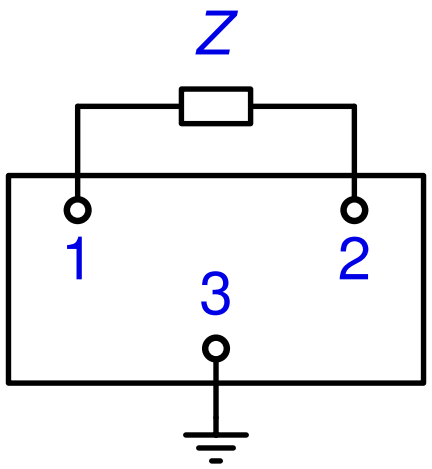
Miller's Theorem

- In many amplifiers, there is an impedance between the input and output of the amplifier which complicates analysis
- Miller's Theorem can be used to modify the circuit to simplify the analysis
- A common example is C_{gd} in a transistor amplifier
  - Miller's theorem can be used to replace C_{gd} with 2 grounded capacitors ...
    one at the gate and one at the drain

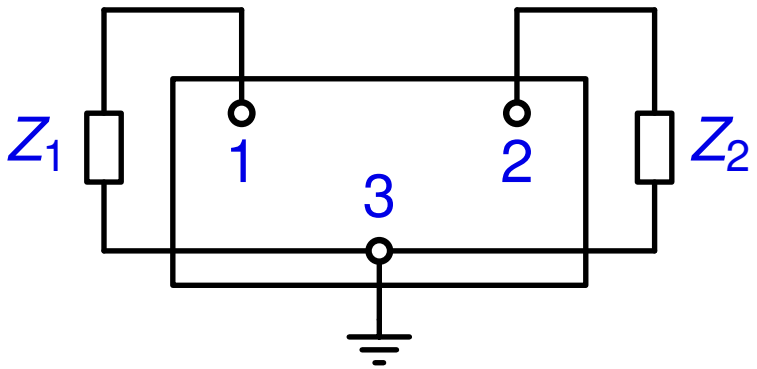
Miller's Theorem

- Given a circuit where $V_2 = KV_1$ and Z is connected between nodes V_1 and V_2, Z can be replaced by 2 grounded impedances where

$$Z_1 = \frac{Z}{1-K} \qquad Z_2 = \frac{Z}{1-\frac{1}{K}} \tag{18}$$

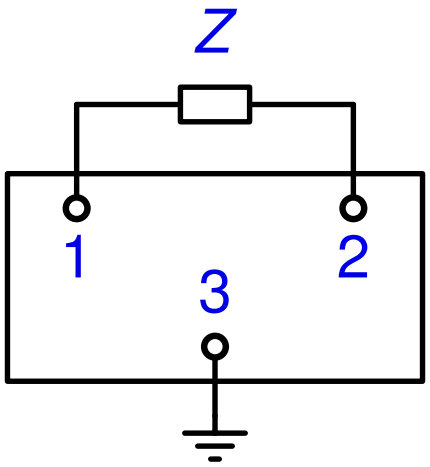


Original Circuit

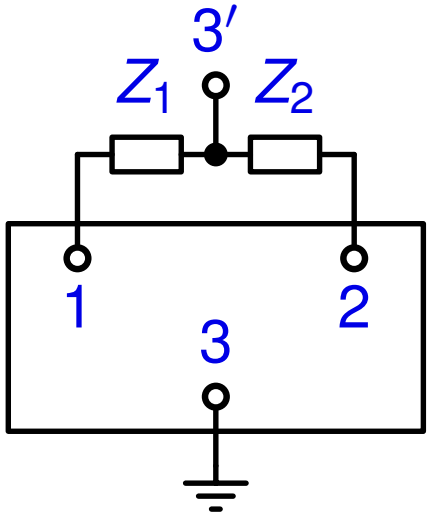


Miller Equivalent

Miller's Theorem Proof



Original Circuit



Equivalent Circuit

- Define

$$K \equiv \frac{V_2}{V_1} \tag{19}$$

- Break Z into Z_1 and Z_2
- Find Z_1, Z_2 such that the following 2 equations hold

$$Z_1 + Z_2 = Z \tag{20}$$

$$V_{3'} = V_3 = 0 \tag{21}$$

Miller's Theorem Proof

$$V_{3'} = V_1 + Z_1 \left(\frac{V_2 - V_1}{Z_1 + Z_2} \right) \tag{22}$$

- Combining (19) - (22), we find

$$Z_1 = \frac{Z}{1 - K} \qquad Z_2 = \frac{Z}{1 - \frac{1}{K}} \tag{23}$$

- We can now attach $V_{3'}$ to V_3 since both are at the same voltage
  - no extra current flows in or out of V_3 since the current through Z_1 equals the negative value of the current through Z_2

[Davidovic, IEEE Trans. on Ed, 1999]

Miller's Theorem

- Note that for $Z > 0$
  - For $K < 0$, both Z_1 and Z_2 will be positive
  - For $K > 0$, one of Z_1, Z_2 will be negative
  - For $K = 1$, both Z_1, Z_2 go to ∞
- For $Z = R$

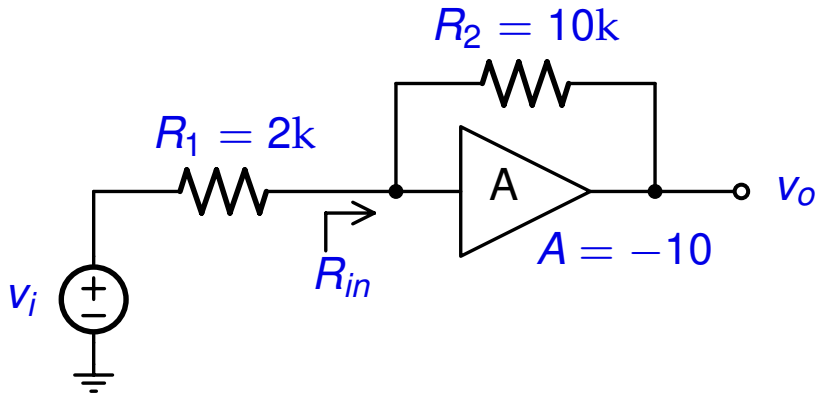
$$R_1 = \frac{R}{1-K} \qquad R_2 = \frac{R}{1-\frac{1}{K}} \tag{24}$$

- For $Z = \frac{1}{sC}$

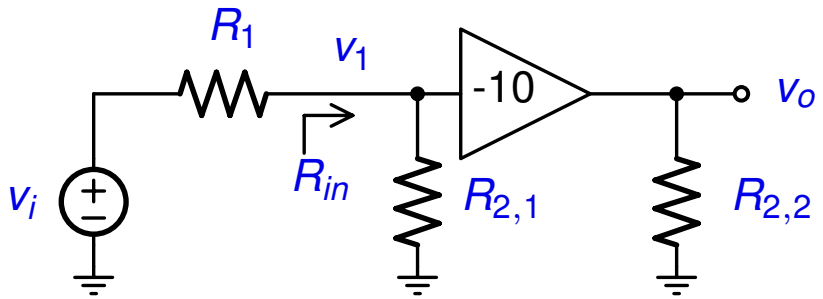
$$C_1 = C(1-K) \qquad C_2 = C(1-\frac{1}{K}) \tag{25}$$

Miller's Theorem Example

- Find R_{in} and v_o/v_i in the circuit below where the amplifier is ideal and has a gain of -10.



- We can use Miller's Theorem to find the equiv circuit



Miller's Theorem Example

$$R_{2,1} = \frac{R_2}{1 - A} = \frac{10\text{k}}{11} = 909.1\Omega \tag{26}$$

$$R_{2,2} = \frac{R_2}{1 - (1/A)} = \frac{10\text{k}}{1.1} = 9.1\Omega \tag{27}$$

- Here, we see that $R_{in} = R_{2,1} = 909.1\Omega$
- We can find v_1/v_i as ...

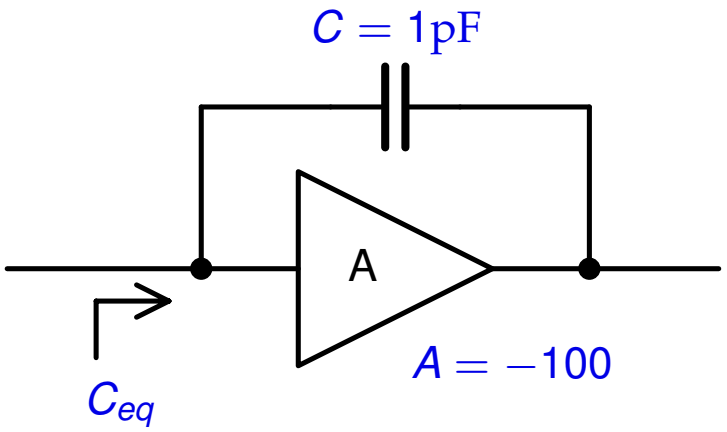
$$\frac{v_1}{v_i} = \frac{R_{in}}{R_{in} + R_1} = \frac{909.1}{909.1 + 2\text{k}} = 0.3125\ \text{V/V} \tag{28}$$

- And since $v_o = -10v_1$, we have

$$v_o/v_i = \frac{v_1}{v_i} \times \frac{v_o}{v_1} = 0.3125 \times -10 = -3.125\ \text{V/V} \tag{29}$$

Miller's Theorem Example

- Find the input capacitance of the following circuit where the amplifier is ideal.

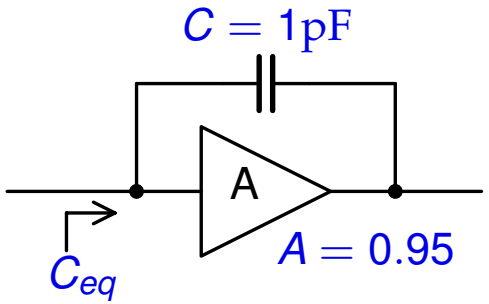


- Using Miller's Theorem

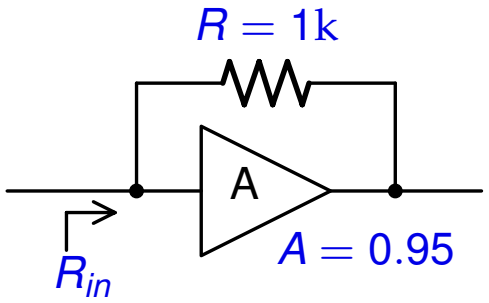
$$C_{eq} = C(1 - A) = 101C = 101\text{pF} \tag{30}$$

Miller's Theorem Example - Bootstrapping

- When the amplifier is slightly less than 1, the input capacitance can be reduced while the input resistance is increased.



$$C_{eq} = C(1 - A) = 0.05C = 50\text{fF} \tag{31}$$



$$R_{in} = \frac{R}{1 - A} = \frac{1\text{k}}{0.05} = 20\text{k}\Omega \tag{32}$$

Topics Covered

- High freq cutoff
  - Mosfet cap modelling
  - Mosfet unity gain freq
  - Miller's theorem