Mosfet Transistors

Large Signal Modeling and DC Analysis

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When studying transistors, there are 2 main analysis methods used:

(1) Large signal analysis
(2) Small signal analysis

Large signal analysis is used when the voltage/current values changes are large such that the non-linear behavior of the transistor must be accounted for. Large signal analysis is mainly used for finding the bias conditions of a circuit. The bias condition of a circuit is the set of voltage/current values that occur in a circuit when all input signals are set to a fixed dc value. For example, if the circuit is a microphone amplifier, then the dc bias conditions for that amplifier is the set of voltage/current values for that amplifier when there is no audio signal on the microphone.

Small signal analysis is used when one wants to ignore the non-linear behaviour of the transistor and instead look at variations in the voltage/current values from their bias conditions. As an example, this is useful when looking at how a microphone amplifier responds to a small audio signal.

This summary will go over the large signal models that are used for large signal analysis for Mosfet transistors as well as dc bias analysis.

NMOS and PMOS Mosfet transistors

Mosfet transistor are 4 terminal devices. Their terminals are

- Drain (D)
- Gate (G)
- Source (S)
- Bulk (B)

The bulk terminal is also referred to as the substrate terminal.

While Mosfet transistors have 4 terminals, in this summary, we will assume the bulk and source terminals are connected together so that we can treat the transistor as a 3 terminal device: Drain, Gate and Source.

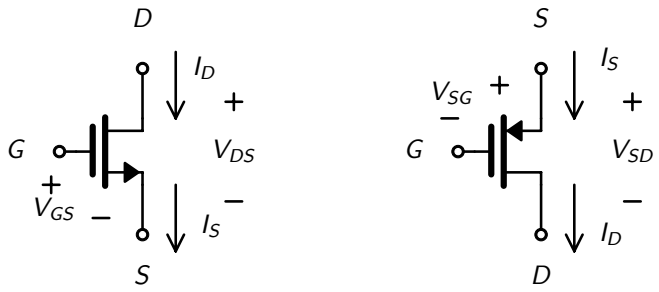
There are 2 main types of Mosfet transistors - NMOS and PMOS.

For both NMOS and PMOS transistors, the drain/source terminals are built the same way and which terminal is the source is determined by the voltage potential. For NMOS transistors, the source is the drain/source terminal with the lower voltage. For PMOS transistors, the source is the drain/source terminal with the higher voltage.

NMOS transistors turn on when the gate-source voltage is higher than the NMOS positive threshold voltage.

On the other hand, PMOS transistors turn on when the gate-source voltage is more negative than the PMOS negative threshold voltage.

Below is the symbols for NMOS and PMOS transistors (recall the bulk is connected to the source so the bulk terminal is not shown)



Note that we have shown the NMOS source terminal to be at the bottom (since it is the lower voltage of the drain/source terminals) while the PMOS source terminal is shown at the top (since it is the higher voltage of the drain/source terminals). In this way, the drain current, I_D, is positive and the drain current flows into the drain for an NMOS transistor while the drain current flows out of the drain for a PMOS transistor.

For the NMOS transistor, V_{GS} is generally positive while V_{DS} is always positive (since we have defined the source to be the drain/source terminal with the lower voltage).

For the PMOS transistor, V_{SG} is used and it is usually positive while V_{SD} is always positive (since we have defined the source to be the drain/source terminal with the higher voltage).

For both NMOS and PMOS transistors, the gate is insulated from the channel of the transistor resulting in the current going into the gate, $I_G = 0$

$$I_G = 0$$

Since the gate current equals zero, the source current equals the gate current so we have

$$I_D = I_S$$

Mosfet Parameters

- V_{tn}: NMOS threshold voltage. $V_{tn} > 0$
- V_{tn}: PMOS threshold voltage. $V_{tp} < 0$
- μ_n, μ_p: electron mobility and hole mobility
- C_{ox}: gate capacitance per unit area (typically the same for NMOS and PMOS transistors)
- W: width of the transistor
- L: length of the transistor
- λ_n: NMOS channel length modulation parameter. $\lambda_n > 0$
- λ_p: PMOS channel length modulation parameter. $\lambda_p < 0$

In an ideal transistor, $\lambda = 0$ so that the drain current is not a function of V_{DS} when the transistor is in the active region.

NMOS Large Signal Model

The overdrive voltage, V_{ov}, is defined to be the amount of voltage that V_{GS} is above the threshold voltage, V_{tn}. It is a useful value as it makes the equations slightly simpler and it gives an indication of how strongly the transistor is switched on.

$$V_{ov} \equiv V_{GS} - V_{tn}$$

Cutoff Region (NMOS)

Condition: $V_{GS} \leq V_{tn}$

$$I_D = 0$$

Triode Region (NMOS)

Conditions: $V_{GS} \geq V_{tn}$, $V_{DS} \leq V_{ov}$

$$I_D = \mu_n C_{ox}(W/L)(V_{ov} - V_{DS}/2)V_{DS}$$

Note that $I_D \geq 0$

Active Region (Saturation Region) (NMOS)

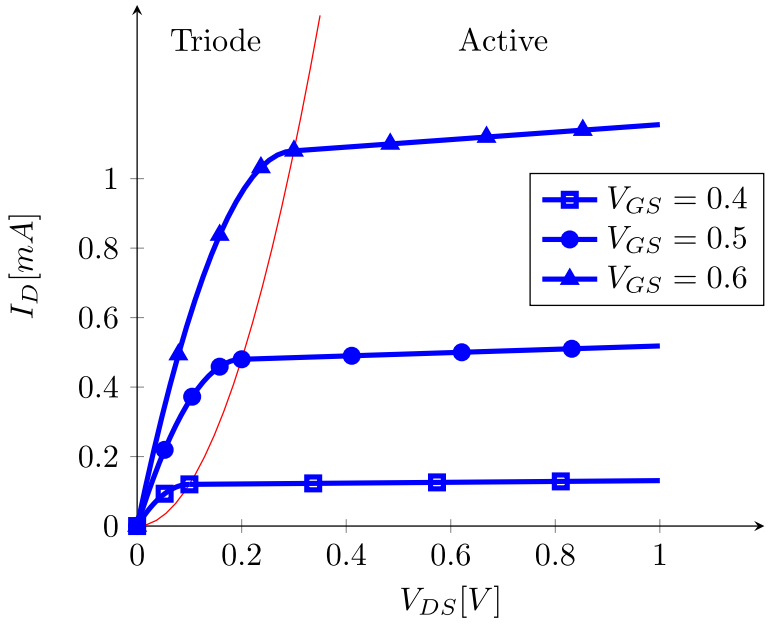
Conditions: $V_{GS} \geq V_{tn}$, $V_{DS} \geq V_{ov}$

$$I_D = \left(\frac{\mu_n C_{ox}}{2}\right)\left(\frac{W}{L}\right) V_{ov}^2(1 + \lambda_n V'_{DS}) \quad (V'_{DS} = V_{DS} - V_{ov})$$

Note that $I_D \geq 0$

A plot of I_D vs V_{DS} for various V_{GS} values is shown below when the transistor is in triode and active regions.

For this example: $V_{tn} = 0.3V$; $\mu_n C_{ox} = 240\mu A/V^2$; $W/L = 100$; $\lambda_n = 0.1mA/V$



PMOS Large Signal Model

It is possible to use negative voltages such as V_{GS} and V_{DS} for PMOS transistors but the approach taken here is to use positive voltages so that the equations operate similar to those for an NMOS transistor.

The overdrive voltage, V_{ov}, is defined to be the amount of voltage that V_{SG} is above the magnitude of the threshold voltage, $|V_{tp}|$.

$$V_{ov} \equiv V_{SG} - |V_{tp}|$$

Cutoff Region (PMOS)

Condition: $V_{SG} \leq |V_{tp}|$

$$I_D = 0$$

Triode Region (PMOS)

Conditions: $V_{SG} \geq |V_{tp}|$, $V_{SD} \leq V_{ov}$

$$I_D = \mu_p C_{ox}(W/L)(V_{ov} - V_{SD}/2)V_{SD}$$

Note that $I_D \geq 0$

Active Region (Saturation Region) (PMOS)

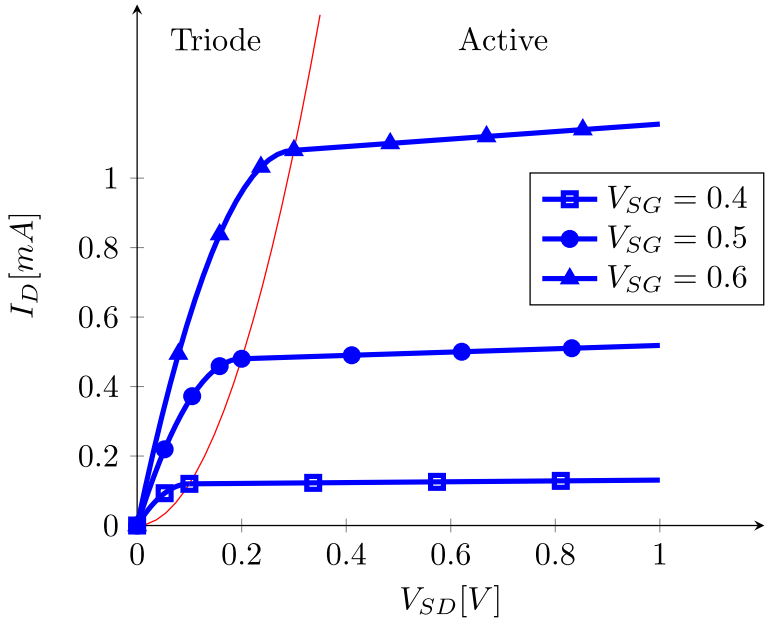
Conditions: $V_{SG} \geq |V_{tn}|$, $V_{SD} \geq V_{ov}$

$$I_D = \left(\frac{\mu_p C_{ox}}{2}\right)\left(\frac{W}{L}\right) V_{ov}^2(1 + |\lambda_p| V'_{SD}) \quad (V'_{SD} = V_{SD} - V_{ov})$$

Note that $I_D \geq 0$

A plot of I_D vs V_{SD} looks the same as the NMOS plot except that the horizontal axis becomes V_{SD} and various V_{SG} values are plotted as shown below.

For this example: $V_{tp} = -0.3V$; $\mu_p C_{ox} = 240\mu A/V^2$; $W/L = 100$; $\lambda_p = -0.1mA/V$



Finding the DC operating point

Finding the DC operation point is done quite differently between software simulation (like spice) and hand analysis.

In a simulation, roots are found for non-linear equations that model the transistor over all the regions of operation. The simulator will take an iterative approach to find the roots.

With hand analysis, we have different equations depending on what region of operation the transistor is in: cutoff, triode or active. So we need to know what operationg region the transistor is in but we don't know which region the transistor is in until we do our analysis. The solution to this small paradox is to GUESS a region of operation, do hand analysis and see if the results are consistent with the transistor being in that operating region. So our approach is

1. Guess a set of operating regions for each transistor

2. Perform hand analysis

3. Check to see if results agree that the transistors are in the guessed operating regions.

4. If the results do not agree, guess another set of operating regions for each transistor.

Fortunately, for most analog circuits, the operating region of the transistors are usually in either the cutoff or active region. As a result, we normally make our first guess that the transistor is in the active region, and our second guess is the cutoff region. If both fail to give consistent results, we move on to the triode region.

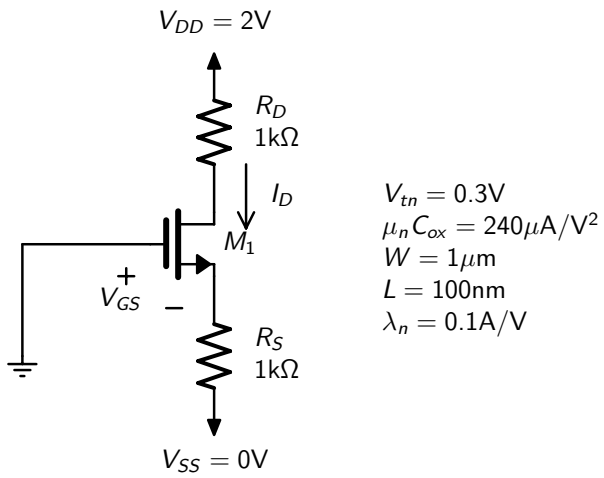
Often set $\lambda = 0$ for DC bias hand analysis

When performing hand analysis (as opposed to simulation), it is common practice to set $\lambda = 0$ when finding the DC bias conditions. By setting $\lambda = 0$, the analysis is significantly simplfied and the error is generally small. However, during small-signal analysis, it is generally important to not make this simplification as there are many cases where this simplification will lead to gross errors.

In general, for dc bias analysis, one should assume $\lambda = 0$ unless there is a reason not to do. One example might be when one is interested in the matching accuracy between the 2 currents from 2 different transisitors.

DC bias example 1

Find V_S, V_{GS}, V_{DS} and I_D for the circuit below.



Assume the transistor is in the active region. To be in the active region, $V_{GS} \geq 0.3$V. Since the gate is at 0V (due to the ground connection), the source must be below 0V which means the current through R_S is flowing up to the source resulting in $I_S < 0$. However, for the transistor to be in the active region, $I_D \geq 0$ and also $I_D = I_S$ all the time for a Mosfet transistor. I_S can not be both greater than 0 and less than zero, so we have a contradiction and the transistor is NOT in the active region.

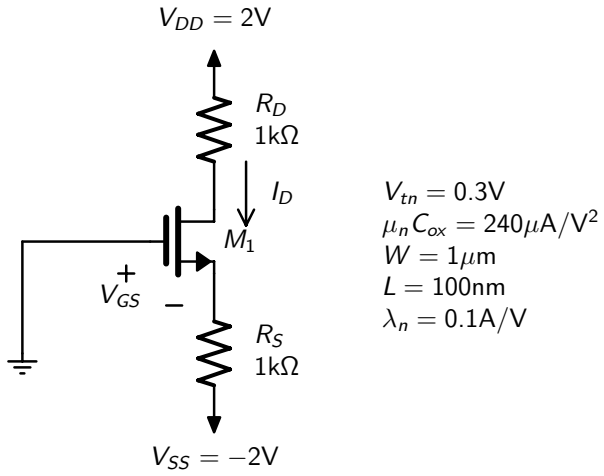
Assume the transistor is in the cutoff region which means $I_D = 0$. Since $I_D = I_S = 0$, then $V_S = 0$V, $V_D = 2$V, and $V_{GS} = 0$V. There is no contradiction here, so our assumption that the transistor is in cutoff is

correct. The final results are...

$V_S = 0\text{V}$, $V_{GS} = 0\text{V}$, $V_{DS} = 2\text{V}$ and $I_D = 0A$.

DC bias example 2

Find V_S, V_{GS}, V_{DS} and I_D for the circuit below.



Assume the transistor is in the active region and also let $\lambda_n = 0$ as discussed above. Recall $V_{GS} = V_{ov} + V_{tn}$. We have 2 equations

$$I_S = \frac{-(V_{ov} + V_{tn}) - (V_{SS})}{R_S}$$

$$I_S = I_D = 0.5\mu_n C_{ox}(W/L)(V_{ov})^2$$

Putting in values, we have

$$I_S = 0.0017 - 0.001 V_{ov}$$

$$I_S = 0.0012 V_{ov}^2$$

and combining the above 2 equations and rearranging we have

$$V_{ov}^2 + 0.8333 V_{ov} - 1.4167 = 0$$

The above is a quadratic equation of the form $ax^2 + bx + c = 0$. The roots of a quadratic equation are found to be

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

Using the above quadratic equation solution results in 2 values for V_{ov}: 0.8444V and -1.678V. However, we know that $V_{ov} > 0$ so the solution is $V_{ov} = 0.8444\text{V}$.

$V_{GS} = V_{ov} + V_{tn} = (0.8444) + (0.3) = 1.144\text{V}$

$I_D = k3 * (V_{ov})^2 = (1.2e-3) * ((0.8444))^2 = 855.6\mu\text{A}$

Now we need to check that $V_{DS} \geq V_{ov}$ to ensure the device is in the active region.

$V_S = -V_{GS} = -(1.144) = -1.144\text{V}$

$V_D = V_{DD} - I_D * R_D = (2) - (855.6e-6) * (1e3) = 1.144\text{V}$

$V_{DS} = V_D - V_S = (1.144) - (-1.144) = 2.289\text{V}$

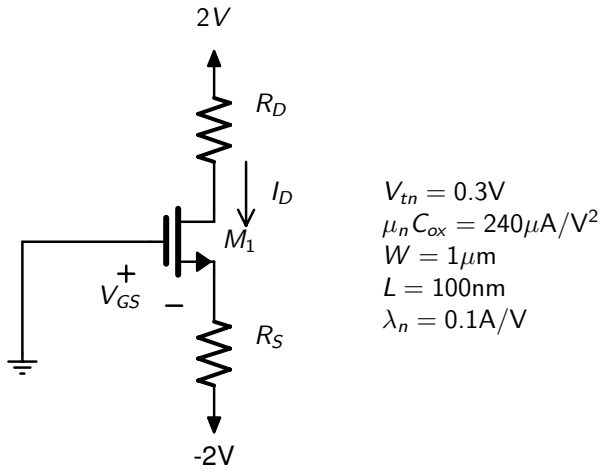
So $V_{DS} = 2.289\text{V}$ is indeed greater than $V_{ov} = 0.8444\text{V}$

So everything is consistent with M_1 being in the active region and the final results are:

$V_S = -1.144\text{V}$, $V_{GS} = 1.144\text{V}$, $V_{DS} = 2.289\text{V}$ and $I_D = 855.6\mu\text{A}$.

DC bias example 3

For the circuit below, choose values for R_D and R_S such that $I_D = 1\text{mA}$ and $V_D = 1\text{V}$



Since $V_D = 1\text{V}$ and $I_D = 1\text{mA}$, we can find the value of R_D from

$I_D = (V_{DD} - V_D)/R_D$

$R_D = (V_{DD} - V_D)/I_D = ((2) - (1))/(1e-3) = 1\text{k}\Omega$

To find R_S, we first find V_{ov} from the equation (assume $\lambda_n = 0$ as discussed above)

$I_D = 0.5\mu_n C_{ox}(W/L)(V_{ov})^2$

$1\text{mA} = 0.0012V_{ov}^2$

$V_{ov} = \sqrt{1\text{mA}/1.2e-3} = 0.9129\text{V}$

(We take the positive root since $V_{ov} \geq 0$)

$V_{GS} = V_{ov} + V_{tn} = (0.9129) + (0.3) = 1.213\text{V}$

and since $V_G = 0$ then $V_S = -1.213\text{V}$

So now we can find R_S from

$I_S = I_D = (V_S - V_{SS})/R_S$

$R_S = (V_S - V_{SS})/I_D = ((-1.213) - (-2))/(1e-3) = 787.1\Omega$

and find V_{DS}

$V_{DS} = V_D - V_S = (1) - (-1.213) = 2.213\text{V}$

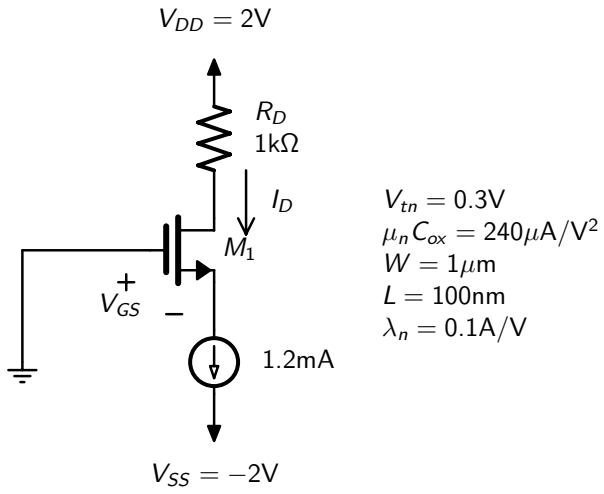
As a final check, we find $V_{DS} = 2.213\text{V}$ and $V_{ov} = 0.9129\text{V}$. Since $V_{DS} \geq V_{ov}$, the transistor is in the active region as was assumed so there is no contradiction.

The final results are $R_D = 1\text{k}\Omega$ and $R_S = 787.1\Omega$

We see here that this analysis was somewhat easier than example 2 since we did not have to solve a quadratic equation. The challenge with example 2 is that we had to solve for I_D and V_{ov} at the same time while in example 3, I_D was given so finding V_{ov} is straightforward.

DC bias example 4

Find V_S, V_{GS}, V_{DS} and I_D for the circuit below.



Since we see $I_S = 1.2\text{mA}$, and $I_D = I_S$, we have $I_D = 1.2\text{mA}$.

Now assuming the transistor is in the active region, we can write

$I_D = 0.5\mu_n C_{ox}(W/L)(V_{ov})^2$

we can write

$1.2\text{mA} = 0.0012V_{ov}^2$

$V_{ov} = \sqrt{1.2\text{mA}/1.2e-3} = 1\text{V}$

$V_{GS} = V_{ov} + V_{tn} = (1) + (0.3) = 1.3\text{V}$

and since $V_G = 0$ then $V_S = -1.3\text{V}$

To find V_D, we have

$V_D = V_{DD} - I_D R_D$

$V_D = V_{DD} - I_D * R_D = (2) - (1.2e-3) * (1e3) = 0.8\text{V}$

resulting in

$V_{DS} = V_D - V_S = (0.8) - (-1.3) = 2.1\text{V}$

Now we see that $V_{DS} > V_{ov}$ so everything is consistent with M_1 being in the active region and the final results are:

$V_S = -1.3\text{V}$, $V_{GS} = 1.3\text{V}$, $V_{DS} = 2.1\text{V}$ and $I_D = 1.2\text{mA}$.