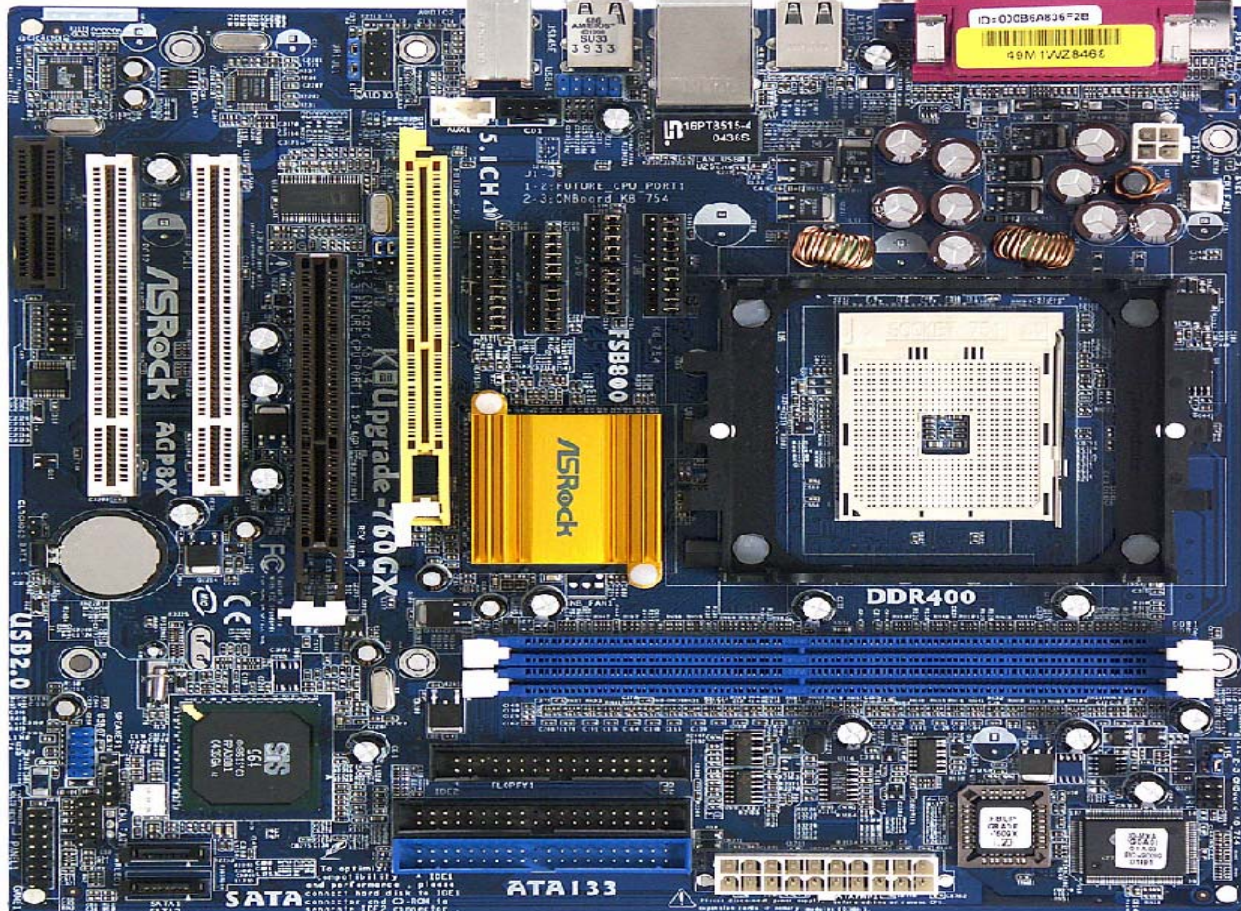
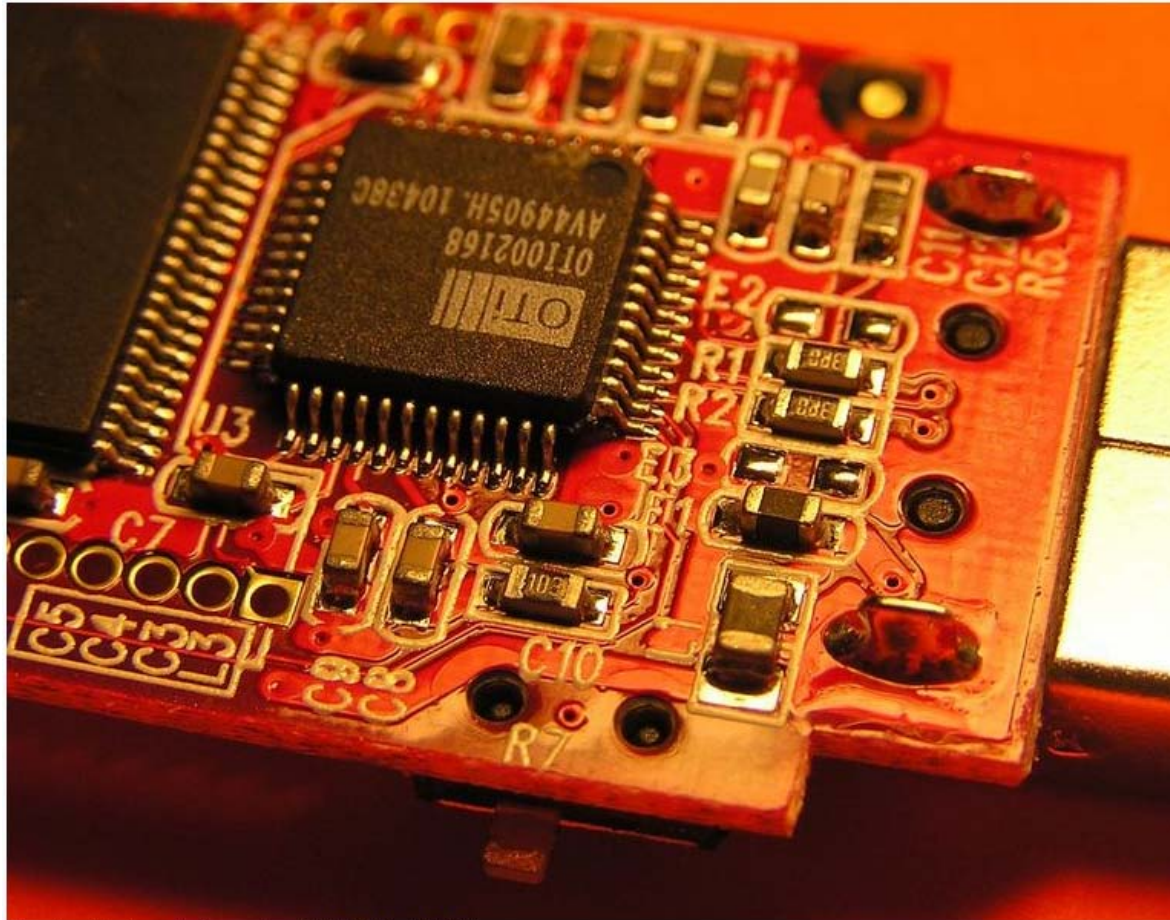


Motherboard PCB

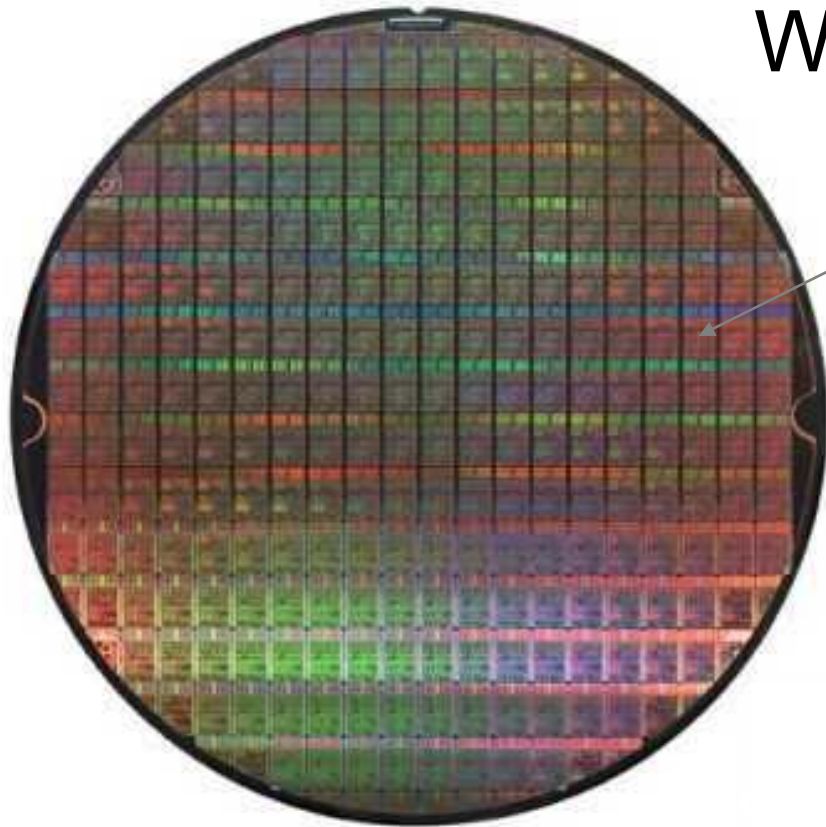


Surface Mount PCB



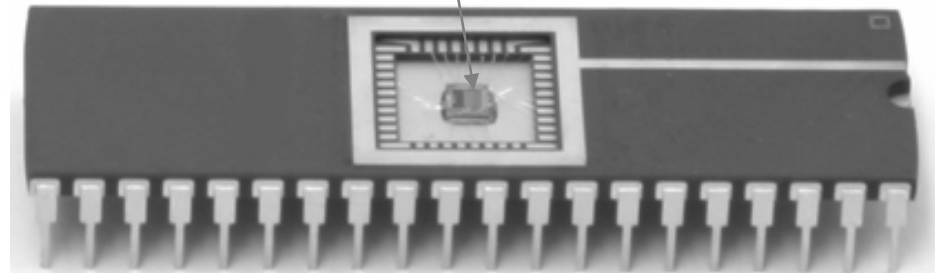
Downloaded from <http://www.seas.upenn.edu/~kshen> (4004:4000 - 4001:4000)

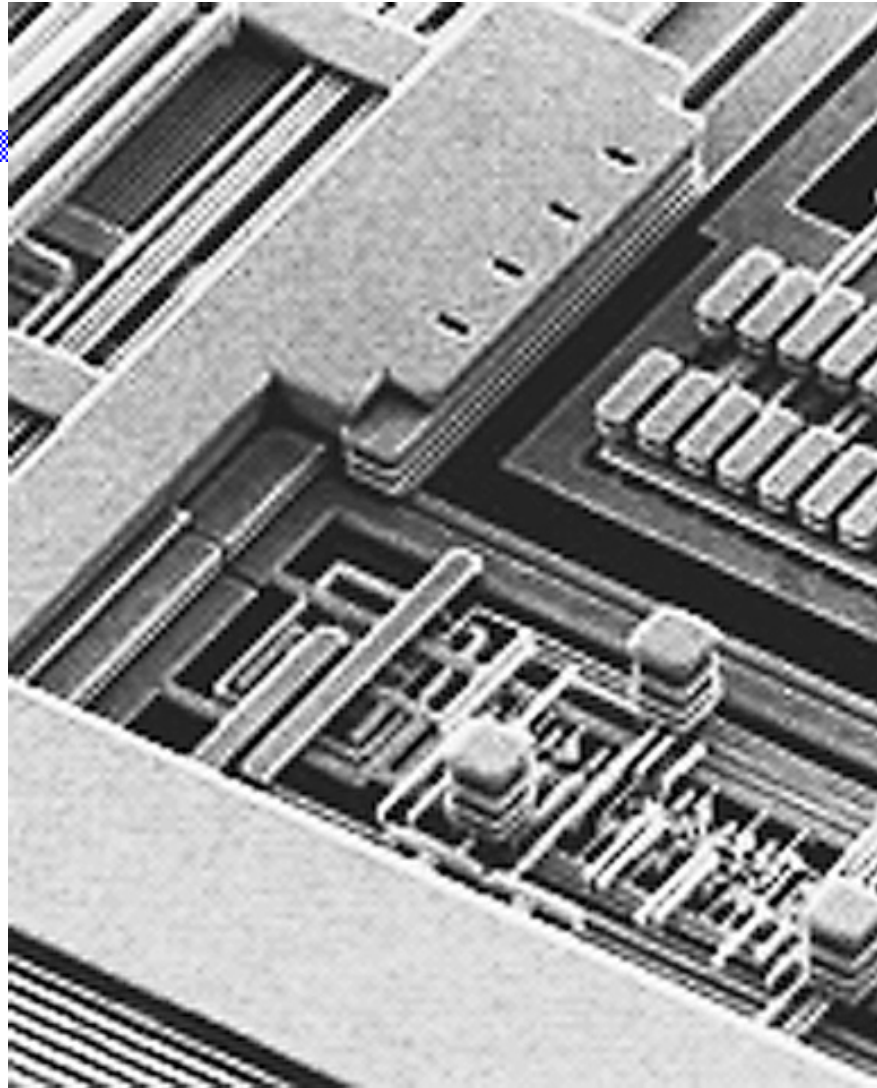
Chip Manufacturing



Wafer

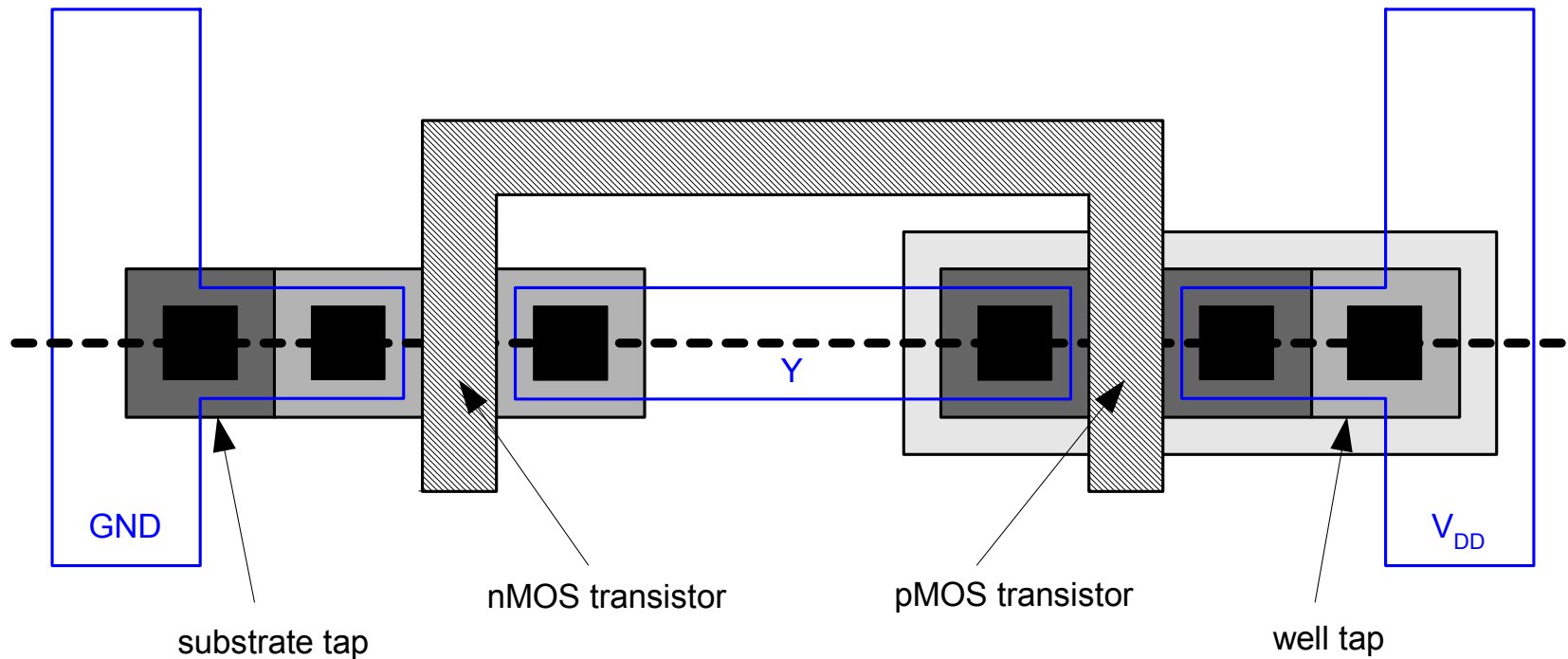
Single die





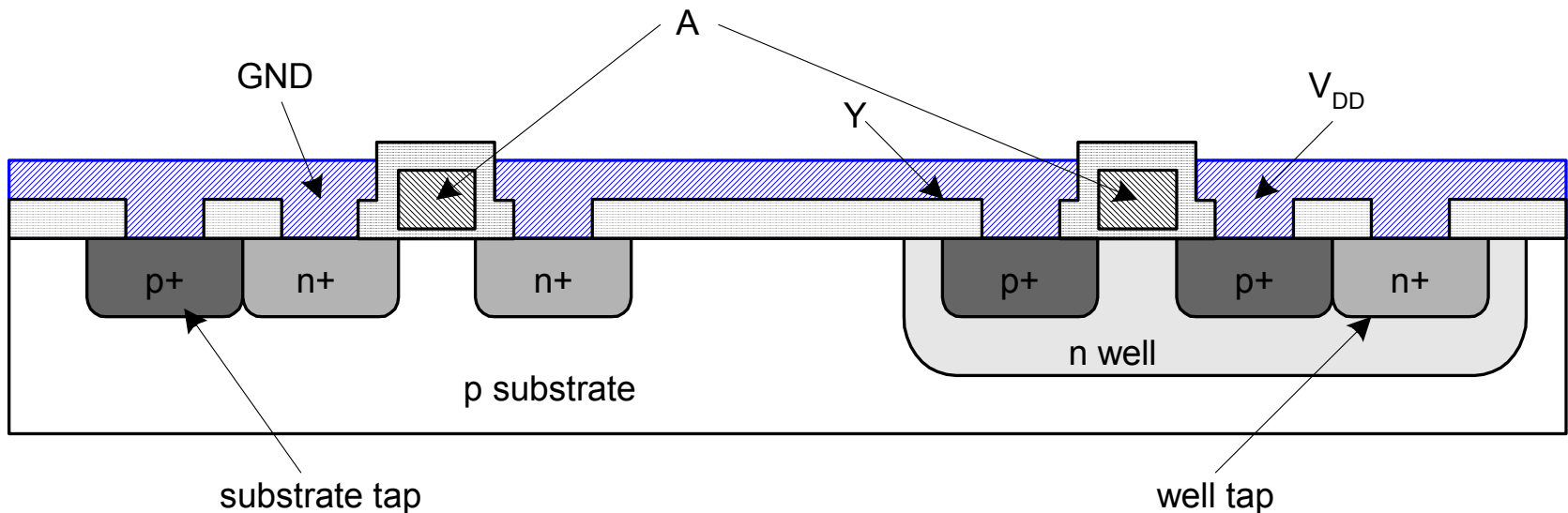
Inverter Mask Set

- ❑ Transistors and wires are defined by *masks*
- ❑ Cross-section taken along dashed line



Inverter Cross Section

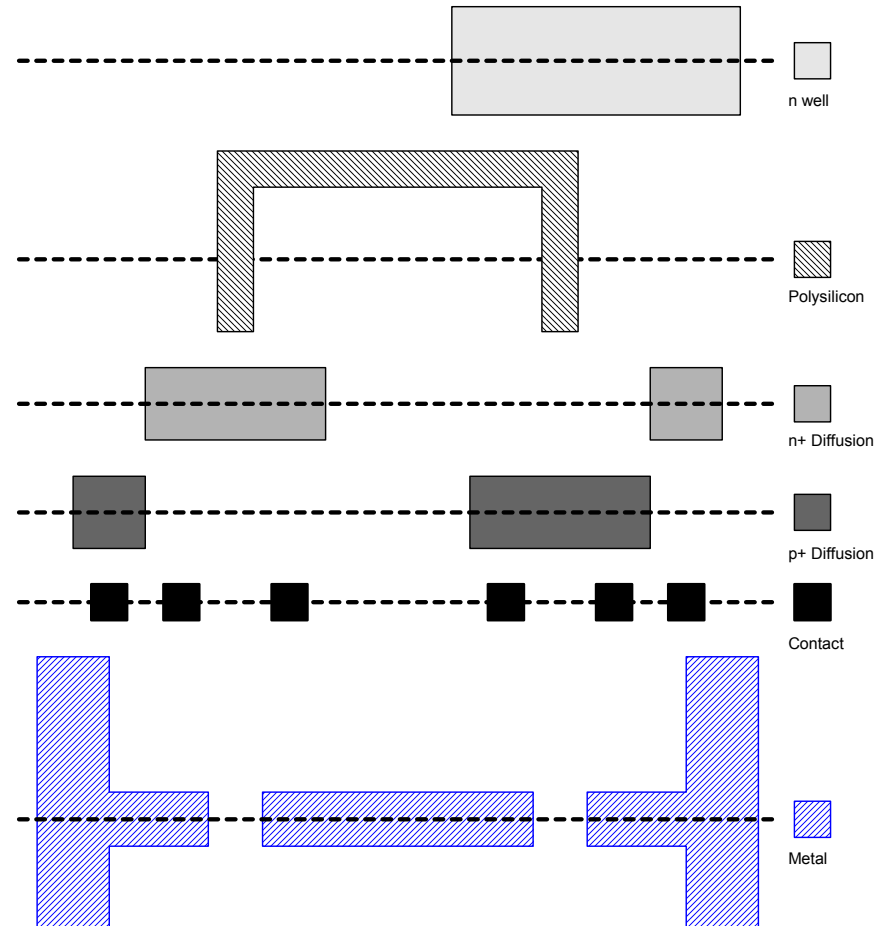
- ❑ Substrate must be tied to GND and n-well to V_{DD}
- ❑ Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- ❑ Use heavily doped well and substrate contacts / taps



Detailed Mask Views

□ Six masks

- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal

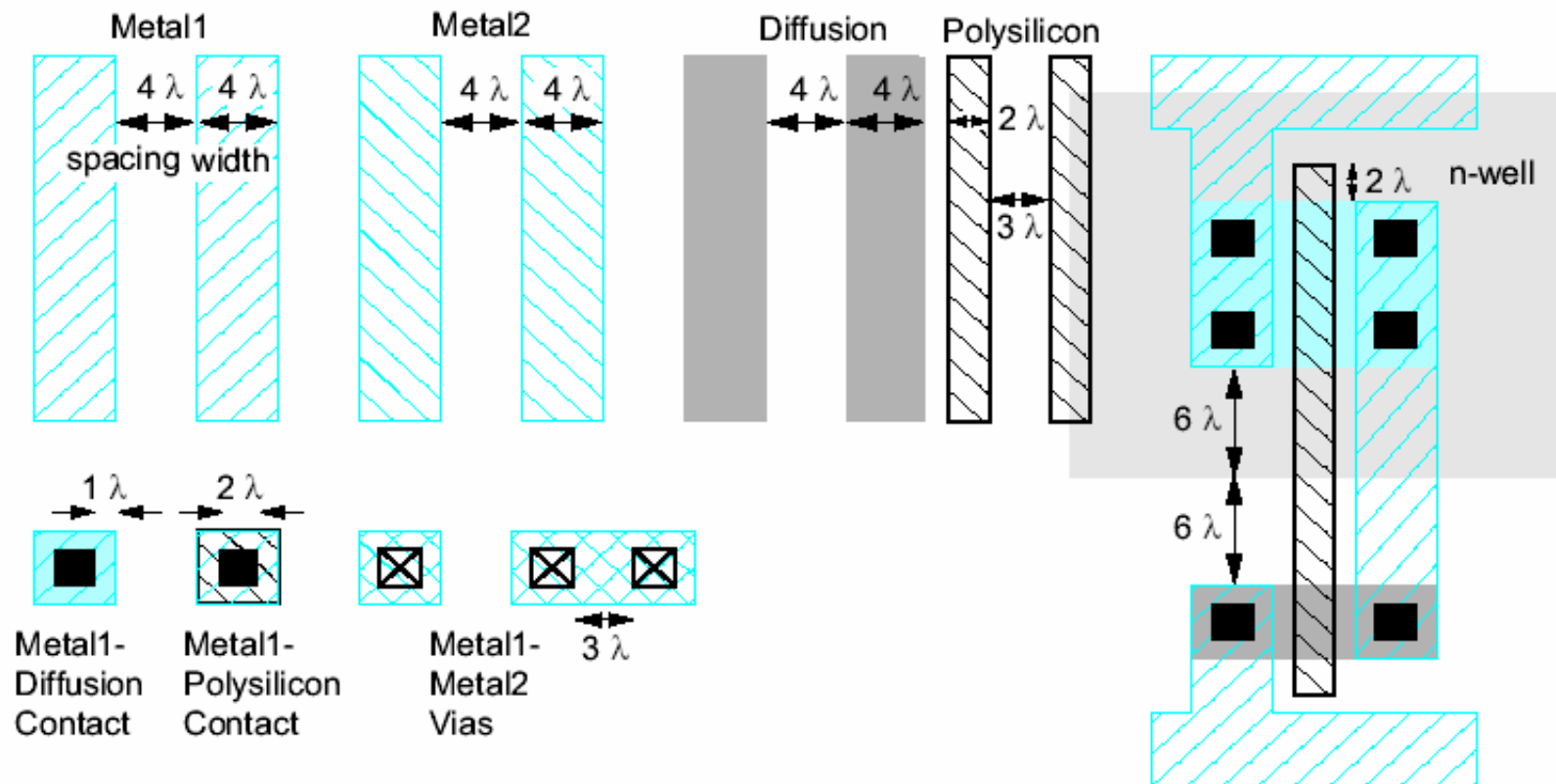


Layout

- ❑ Chips are specified with set of masks
- ❑ Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- ❑ Feature size f = distance between source and drain
 - Set by minimum width of polysilicon
- ❑ Feature size improves 30% every 3 years or so
- ❑ Normalize for feature size when describing design rules
- ❑ Express rules in terms of $\lambda = f/2$
 - E.g. $\lambda = 0.3 \mu\text{m}$ in $0.6 \mu\text{m}$ process

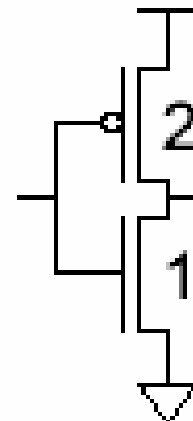
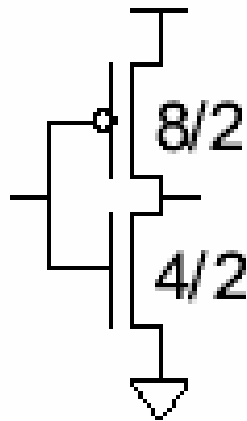
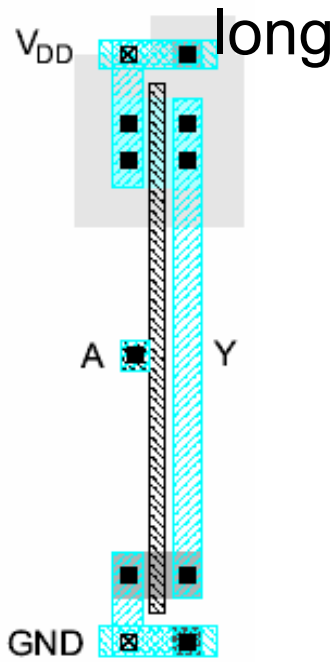
Simplified Design Rules

- ❑ Conservative rules to get you started

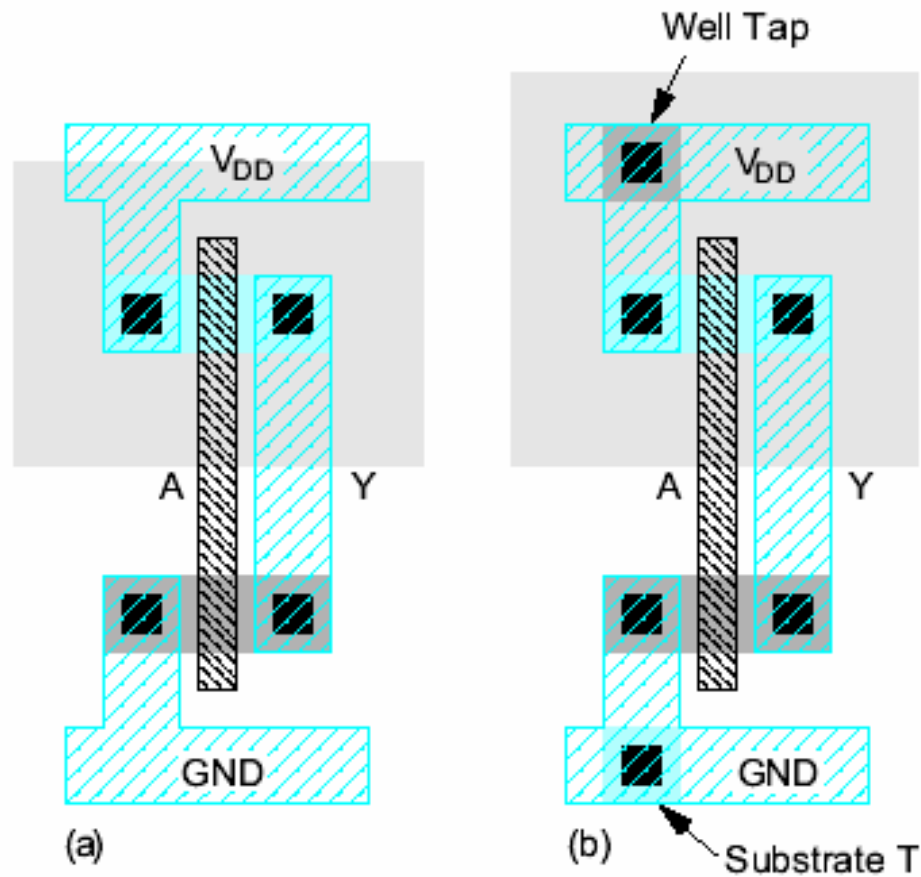


Inverter Layout

- ❑ Transistor dimensions specified as Width / Length
 - Minimum size is $4\lambda / 2\lambda$, sometimes called 1 unit
 - In $f = 0.6 \mu\text{m}$ process, this is $1.2 \mu\text{m}$ wide, $0.6 \mu\text{m}$ long

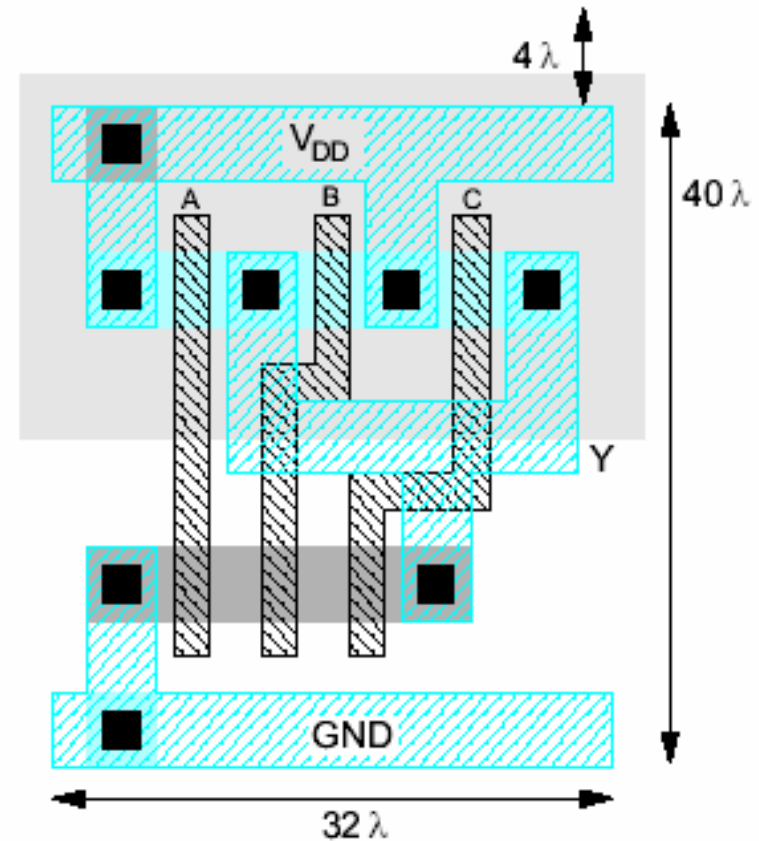


Inverter (2nd example)



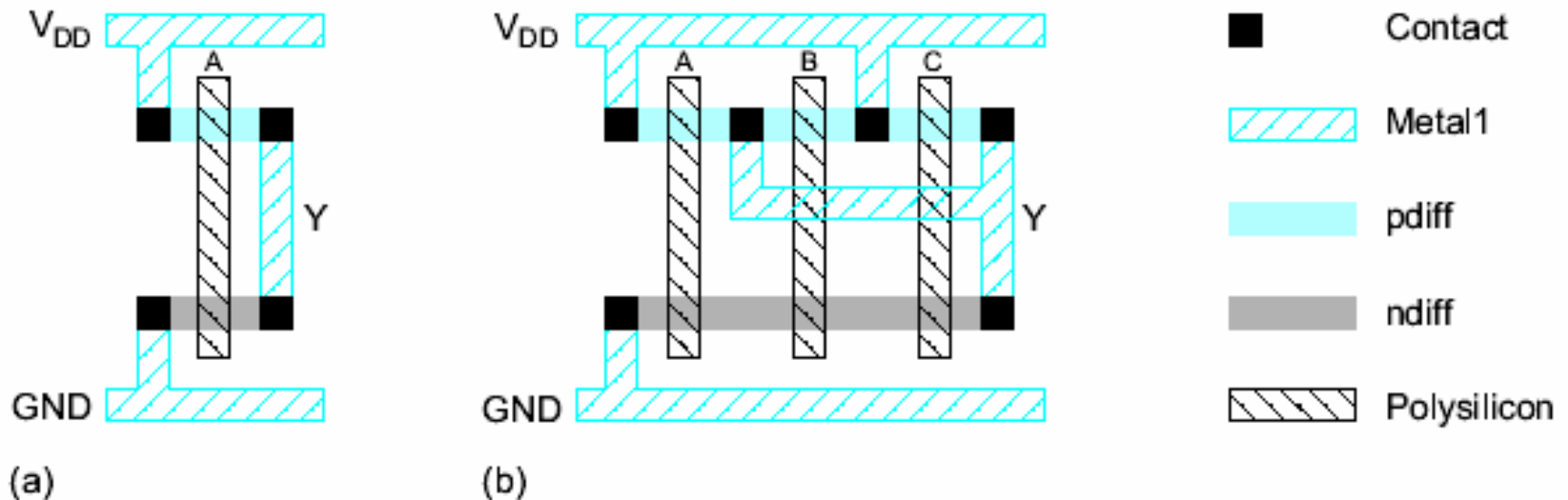
Example: NAND3

- ❑ Horizontal N-diffusion and p-diffusion strips
- ❑ Vertical polysilicon gates
- ❑ Metal1 V_{DD} rail at top
- ❑ Metal1 GND rail at bottom
- ❑ 32λ by 40λ



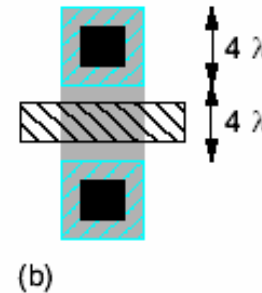
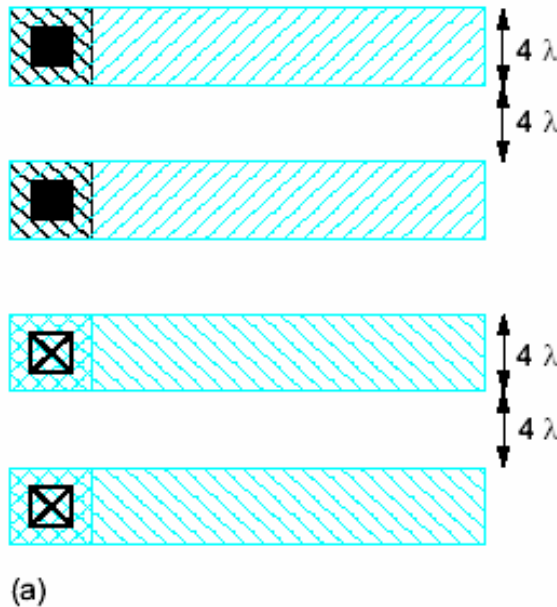
Stick Diagrams

- *Stick diagrams* help plan layout quickly
 - Need not be to scale
 - Draw with color pencils or dry-erase markers



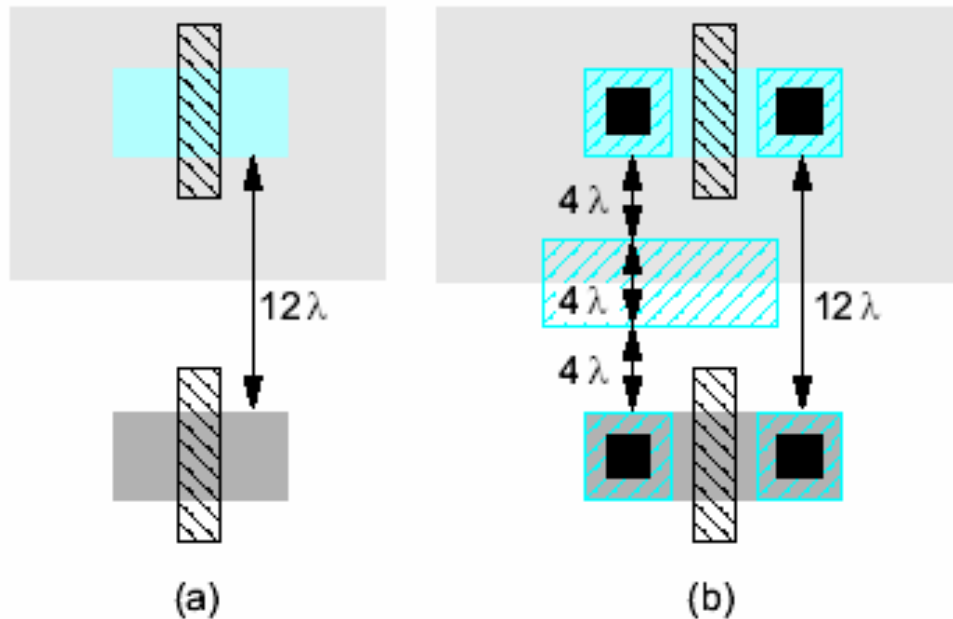
Wiring Tracks

- A *wiring track* is the space required for a wire
 - 4λ width, 4λ spacing from neighbor = 8λ pitch
- Transistors also consume one wiring track



Well spacing

- ❑ Wells must surround transistors by 6λ
 - Implies 12λ between opposite transistor flavors
 - Leaves room for one wire track



Example: O3AI

□ Sketch a stick diagram for O3AI

$$- Y = \overline{(A + B + C)} \square D$$

