MEMORY CIRCUITS

ROM =) READ ONLY MEMORY

RAM =) RANDOM ACCESS MEMORY

SRAM =) STATIC RAM

DRAM =) DYNAMIC RAM

EPROM =) ERASABLE PROGRAMMABLE ROM

EEPROM =) ELECTRICALLY EPROM (E₂PROM)

FLASH =) A TYPE OF EEPROM BUT
LARGE BLOCKS ARE ERASED AT
A TIME SO HIGHER DENSITY

VOLATILE =) LOSES MEMORY WHEN POWER
TURNED OFF

NON-VOLATILE =) RETAINS INFORMATION EVEN
WITH NO POWER

CAM =) CONTENT ADDRESSABLE MEMORY
- DETERMINE WHICH ADDRESS(ES)
CONTAIN DATA THAT MATCHES
A GIVEN KEY
CLASSIFICATION OF MEMORY

1) VOLATILE READ/WRITE MEMORY
   RANDOM = SRAM, DRAM
   NON-RANDOM = FIFO, LIFO, SHIFT REGISTERS, ETC.

2) NON-VOLATILE READ/WRITE MEMORY
   EPROM, EEPROM, FLASH

3) ROM (ALWAYS NON-VOLATILE)
   - MASK PROGRAMMABLE
   - PROM - PROGRAM ONCE BY BLOWING
     SMALL "FUSES"
RANDOM MEMORY ARCHITECTURE.

WOULD LIKE AN N-WORD MEMORY WHERE EACH WORD IS M-BITS WIDE.

M TYPICALLY 1, 4 OR 8

N IS POWER OF 2 USUALLY

Example: \( N = 10^6 \) Actually \( N = 1024 \times 1024 \)
\[ = 1,048,576 \]
\[ = 2^{20} \]

20 BITS \( \Rightarrow \) 1M BYTES.

CONCEPTUAL

K = \( \log_2 N \)

In selecting \( S_i \), LINE GOES HIGH

TO READ OR WRITE WORD \( i \)
IF \( N = 2^m \) and \( M = \) THEN poor aspect ratio and long vertical wires and high capacitive loading \( \Rightarrow \) slow design.

Need a relatively square design.

Recall \( R = \log_2 N \)

Only 1 word line is high depending on \( A_L \to A_{K-1} \) (all rest low)

\( M \) input/output lines connected to 1 of \( 2^{K-1} \) groups depending on \( A_0 \to A_{L-1} \).
Example \( M = 2 \) \( R = 3 \) \( \Rightarrow N = 8 \) words

\( L = 1 \)

Diagram of a memory layout with WL0 through WL3, BL0 through BL3, and A0, A1, A2, and R/W line.
Example want $2^8$ 8-bit words

Store using $L = 8 + 4 \Rightarrow R - L = 12$

8-bit column decode → 256 columns each 8 bits wide
12-bit row decode → 4,096 rows

Bits

$4,096 \times (256 \times 8) = 4,096 \times 2048$

Can further partition memory for even larger sizes & have multiple sense x driver cells.

Example

4 times memory size

4 x 2 8-bit words
MOS DECODERS

Only one of \( S_i \) HIGH according to address bits \( A_2 A_1 A_0 \)

\[
\begin{array}{c}
A_2 \quad \overline{A_2} \quad A_1 \quad \overline{A_1} \quad A_0 \quad \overline{A_0} \\
S_0 \quad S_1 \quad S_2 \quad S_7
\end{array}
\]
However if large number of address lines, then NAND gate would have large number of inputs and be too slow.

Break into precode & decode

Ex 6 address lines

Too slow

Precode stage

Decode stage
EXAMPLE
4 BIT ADDRESS WITH PRECODE

A_3\ A_2
\{ A_3 A_2 \}

A_1\ A_0
\{ A_1 A_0 \}

A_3\ A_2
\{ A_3 A_2 \}
\{ A_1 \ A_0 \}
\{ \bar{A}_1 A_0 \}
\{ A_3 \bar{A}_2 \}
\{ \bar{A}_3 A_2 \}
\{ A_1 A_0 \}
\{ \bar{A}_1 A_0 \}
\{ \bar{A}_3 \bar{A}_2 \}

S_{15}\ S_{14}\ S_{13}\ S_3\ S_2\ S_1\ S_0
SRAM

Word lines (WL) remain single-ended.

Bit lines (BL) (or column lines) are differential BL and BL̅.

6-Transistor SRAM
SRAM Capacitance

\[ \text{CWL\_CELL} = C_{G3} + C_{G4} + \text{CWL\_WIRE\_CELL} \]

\[ \text{CWL} = \text{CWL\_CELL} \times \text{NUMBER OF CELLS IN ROW} \]

\[ \text{CBL\_CELL} = C_{dB4} + \text{CBL\_WIRE\_CELL} \]

\[ \text{CBL} = \text{CBL\_CELL} \times \text{NUMBER OF CELLS IN COLUMN} \]
1) **Precharge** BL and BL both **HIGH**
   then release.

2) Raise WL **HIGH**

3) Wait to see which of BL, BL gets **PULLED** low

4) Clock sense amplifier (attached to BL + BL) to regenerate small AV voltage difference between BL + BL
$\phi_1$  

$WLO$  

$BL, \overline{BL}$  

$\phi_2$  

- $\Delta V$ might be only 200 mV

- Reason for sense amp/regeneration is that $C_{BL}$ large compared to size of transistors in cell so it would take a long time for one of $BL, \overline{BL}$ to be pulled low
Typical Sense Amp

\( \phi_2 \) Low \( \Rightarrow \) Sense/\overline{Sense} Both Pulled High
Via \( BL \) and \( \overline{BL} \)

\( \phi_2 \) High \( \Rightarrow \) regeneration mode