SRAM READ

TRANSISTOR SIZING (FOR NO ERROR)

SINCE CELL IS SYMMETRICAL ONLY NEED TO SIZE M1, M3, M5

\( \overline{BL}, BL \) BOTH PULLED HIGH

DON'T WANT TO CHANGE CELL VALUE
- ONLY READ IT.

CASE 1: \( VA = 0 \) \( VB = VDD \)

WHEN \( M3 + M4 \) TURNED ON, DON'T WANT TO PULL \( VA \) HIGHER THAN VEN2 (OTHERWISE \( M2 \) STARTS TURNING ON)

\[ \begin{align*}
    & CBL \quad VA \quad M3 \\
    & \quad I_{O3} \quad I_{O1} \\
    & \quad M1 \quad AVDD \\
    & \quad VDD \\
    \end{align*} \]

M3 ACTIVE

M1 TRIODE
\[ I_{D3} = \frac{MN \cos \left( \frac{W}{L} \right)}{2} \left( V_{00} - V_A - V_{tn3} \right)^2 \]

\[ I_{D1} = MN \cos \left( \frac{W}{L} \right) \left[ (V_{00} - V_{tn1}) V_A - \frac{V_A^2}{2} \right] \]

Assuming all \( L = L_{min} \)

\( V_{tn} \equiv V_{tn1} = V_{tn2} = V_{tn3} \)

\( \Omega = (\Omega) \Rightarrow \)

\[ \frac{W_2}{2} \left( V_{00} - V_A - V_{tn} \right)^2 = W_1 \left[ (V_{00} - V_{tn}) V_A - \frac{V_A^2}{2} \right] \]

\[ \frac{W_1}{W_3} = \frac{\left( V_{00} - V_A - V_{tn} \right)^2}{2 \left[ (V_{00} - V_{tn}) V_A - \frac{V_A^2}{2} \right]} \]
**Example**

1) \( V_{00} = 2.5V \quad V_{tn} = 0.5V \quad V_A = 0.5V \)

\[
\frac{W_1}{W_3} = \frac{(2.5 - 0.5 - 0.5)^2}{2[(2.5 - 0.5)0.5 - \frac{0.5^2}{2}]} = 1.3
\]

2) \( V_{00} = 1.0V \quad V_{tn} = 0.2V \quad V_A = 0.2V \)

\[
\frac{W_1}{W_3} = 1.3
\]

3) \( V_{00} = V_{00} \quad V_{tn} = \frac{V_{00}}{5} \quad V_A = V_{tn} \)

\[
\frac{W_1}{W_3} = 1.3
\]
SRAM READ

TRANSISTOR SIZING (FOR SPEED)

\[ q = CV \]
\[ I = C \frac{\Delta V}{\Delta t} \]

\[ I_{CELL} = \frac{MN(C_{ox})(W_3/L)}{2}(V_{DD} - 2V_{tn})^2 \]

REQUIRE \( V_{BL} \) TO DROP FROM \( V_{DD} \) TO
\( V_{DD} - \Delta V_{BL} \)

\[ \Delta V_{BL} = \frac{I_{CELL} \Delta t}{C_{BL}} \]
**Example**

**Given**

\[ V_{th} = 0.5 \text{V} \]
\[ V_{dd} = 2.5 \text{V} \]
\[ L_{min} = 0.25 \mu\text{m} \]
\[ C_{BL} = 1 \text{pF} \]

**Find** sizes of \( M_1 \) and \( M_2 \) such that \( \Delta V_{BL} = 0.5 \text{V} \) in \( 1 \text{ms} \)

\[
I_{CELL} = \frac{\Delta V_{BL}}{C_{BL}} \cdot \frac{1}{\Delta t} = \frac{(0.5) (1.0 \times 10^{-12})}{1.0 \times 10^{-9}}
\]

\[ = 0.5 \text{mA} \]

\[ 0.5 \text{mA} = \left( \frac{200 \times 10^{-6}}{2} \right) \left( \frac{W_3}{L_{min}} \right) \left( 2.5 - 1 \right) \]

\[ \frac{W_3}{L_{min}} = 2.2 \Rightarrow W_3 = 0.55 \mu\text{m} \]

\[ W_1 = \frac{1.3 \times 0.55}{A} = 0.72 \mu\text{m} \]

(from no error transistor)

(sizing)
SRAM WRITE

Assume cell has stored \( V_A = V_{DD} \)  
\( V_B = 0 \)

4. Want to write opposite

1) Force \( \overline{V_{BL}} = 0 \)  +  \( V_{BL} = V_{DD} \)

2) Take WL high to \( V_{DD} \)

3) \( V_A \) goes low & turns off \( M_2 \)
   so that \( V_B \) goes high

(Note: We have designed \( M_2 \) & \( M_4 \)
so that \( V_B \) will stay below \( V_{EN} \) unless \( V_A \) goes low
want to size $M_3$ & $M_5$

such that $V_A \approx V_{EN}$ to turn $M_2$ off (overkill but gives a safety margin)

$M_5 \leq$ edge of active/triode

$M_3 \leq$ triode

$I_{D5} = \frac{\mu p \cdot C_0 \cdot (W_5)}{2} \left( \frac{W_5}{L} \right) \left( -V_{DD} - V_{TP} \right)^2$

$I_{D3} = \mu n \cdot C_0 \cdot \left( \frac{W_3}{L} \right) \left[ (V_{DD} - V_{EN})V_A - \frac{V_A^2}{2} \right]$

$I_{D5} = I_{D3}$
\[
\frac{W_3}{W_5} = \frac{M_P (V_{DD} + V_{TP})^2}{2MN \left[ (V_{DD} - V_{TN}) VA - \frac{V_{A}^2}{2} \right]}
\]

\[
\frac{W_3}{W_5} = \frac{M_P (V_{DD} + V_{TP})^2}{2MN \left[ (V_{DD} - V_{TN}) VA - \frac{V_{A}^2}{2} \right]}
\]

**Example**

\[
\frac{M_N}{M_P} = 4 \quad V_{DD} = 2.5 \text{ V} \quad V_{TN} = V_{TP} = 0.5 \text{ V}
\]

Want \( VA = V_{TN} = 0.5 \text{ V} \)

\[
\frac{W_3}{W_5} = \frac{(2.5 - 0.5)^2}{2(4)(2.5 - 0.5)0.5 - \frac{0.5^2}{2}}
\]

\[
\geq 0.57
\]

So if \( W_3 = 0.55 \text{ mm} \)

\( W_5 \leq 0.96 \text{ mm} \Rightarrow \) choose \( W_5 = W_{MIN} \) (say \( 0.5 \text{ mm} \))
BIT LINE TWISTS

\[
\begin{array}{cccccccc}
\overline{BL}_0 & \overline{BL}_0 & \overline{BL}_1 & \overline{BL}_4 & \overline{BL}_2 & \overline{BL}_2 & \overline{BL}_3 & \overline{BL}_3 \\
\uparrow & \uparrow & \uparrow & \uparrow & \uparrow & \uparrow & \uparrow & \uparrow \\
\text{CELLS} & \text{CELLS} & 000 & 000
\end{array}
\]

CAPACITIVE COUPLING INTO \overline{BL}_0 \text{ AND } \overline{BL}_3 \text{ IS MADE EQUAL, SO CAUSES LESS PROBLEM FOR DIFFERENTIAL SENSE AMP.}

NOTE THAT SOME CELLS ARE "INVERTED" BUT SINCE WRITE AND READ ARE BOTH INVERTED, AUTOMATICALLY CORRECT.
DRAM (ONE TRANSISTOR) (ONE CAPACITOR)

CELL

WL

M1

CS < CELL CAPACITANCE

BL

VBIAS

CS SHOULD BE LARGE AS POSSIBLE

WITH MINIMUM AREA

TRENCH CAPACITORS (SPECIALIZED PROCESS)

BL

WL

n+

n+

M1

OXIDE

P+ SUBSTRATE

CS

POLYSILICON PLUG
\[ C_S \approx 30 \text{ fF} \]
\[ C_{BL} \approx 300 \text{ fF} \]

Charge sharing between \( C_S \) and \( C_{BL} \)

BL precharged to \( \frac{V_{DD}}{2} \)

"0" case: \( V_C = 0 \), \( V_{BL} = \frac{V_{DD}}{2} \)

\[ WL = 0 \quad Q_{\text{initial}} = \frac{V_{DD}}{2} C_{BL} + (0 - V_{BIAS}) C_S \]

\[ WL = 1 \quad Q_{\text{final}} = V_0 C_{BL} + (V_0 - V_{BIAS}) C_S \]

\[ Q_{\text{initial}} = Q_{\text{final}} \]

\[ \Rightarrow \frac{V_{DD}}{2} C_{BL} - V_{BIAS} C_S = V_0 C_{BL} + V_0 C_S - V_{BIAS} C_S \]
\[ V_o = \frac{V_{dd}}{2} \left( \frac{C_{BL}}{C_{BL} + C_S} \right) \]

INDEPENDENT OF VBIAS

\[ V_o = \frac{V_{dd}}{2} - \left( \frac{C_S}{C_{BL} + C_S} \right) \left( \frac{V_{dd}}{2} \right) \]

\[ V_o = \frac{V_{dd}}{2} - \left( \frac{C_S}{C_{BL} + C_S} \right) \left( \frac{V_{dd}}{2} \right) \]

\[ V_o = \frac{V_{dd}}{2} - \Delta V \]

\[ V_o = \frac{V_{dd}}{2} - \Delta V \]

\[ V_i = \frac{V_{dd}}{2} + \left( \frac{C_S}{C_{BL} + C_S} \right) \left( \frac{V_{dd}}{2} \right) \]

Define \( \Delta V = \left( \frac{C_S}{C_{BL} + C_S} \right) \left( \frac{V_{dd}}{2} \right) \)

\[ V_o = \frac{V_{dd}}{2} - \Delta V \]

\[ V_i = \frac{V_{dd}}{2} + \Delta V \]
WHAT TO CHOOSE FOR $V_{\text{bias}}$?

=) WANT TRENCH CAPACITOR OXIDE AS THIN AS POSSIBLE TO MAX CAPACITANCE

=) THIN OXIDE MEANS WANT MIN VOLTAGE ACROSS CAPACITOR.

CHOOSE $V_{\text{bias}} = \frac{V_{00}}{2}$ SO MAX VOLTAGE ACROSS TRENCH CAP IS $\frac{V_{00}}{2}$
DRAM BIT LINES ARE NOT DIFFERENTIAL

BUT SENSE AMPS ARE DIFFERENTIAL

OPEN-BIT LINE ARCHITECTURE

\[ \text{WL0} \quad \text{WL2} \quad \text{WL4} \]

\[ \text{WL5} \quad \text{WL3} \quad \text{WL1} \]

\[ \text{BL0} \quad \text{BL1} \quad \text{BL2} \]

\[ \text{BLO} \quad \text{BL1} \quad \text{BL2} \]

\[ \text{SA} \quad \text{SA} \quad \text{SA} \]

\[ \text{WL} \]

\[ \text{SENSE AMPS} \]

ONLY 1 WL GOES HIGH

(SAY WL0) THEN \( \overline{\text{BL0}} \quad \overline{\text{BL1}} \quad \text{BL2} \)

ARE REFERENCE VOLTAGES FOR SENSE AMPS

- HOWEVER, LOCAL NOISE NOT SAME ON \( \text{BL} \quad \text{BL} \quad = \) GO TO FOLDED ARCH.
**Folded-Bit Line Arch**

- Better noise rejection
- Also twist bit lines (as SRAM case)

**Sense Amp**
NOTE NO ISOLATION TRANSISTORS
SO SENSE AMP ALSO DRIVES
BIT LINE CAPACITANCE AS WELL
AS CELL BEING READ
SO A READ ALSO DOES A
REFRESH OF ALL CELLS ON
WORD LINE.
READ SEQUENCE

1) ALL BL & B'L PRECHARGED TO \( \frac{V_{DD}}{2} \)
   THEN RELEASED

2) ONE WL IS SELECTED
   (OTHERS REMAIN LOW)

3) \( V_{BL} \) (OR \( V_{B'L} \)) WILL GO TO
   \[ \frac{V_{DD}}{2} + \Delta V \] OR \[ \frac{V_{DD}}{2} - \Delta V \] DEPENDING
   ON DATA STORED, \( V_{BL} \) (OR \( V_{B'L} \))
   REMAINS AT \( \frac{V_{DD}}{2} \) AS REFERENCE SIGNAL

4) \( \phi_2 \) GOES HIGH DRIVING BL & B'L
   TO EITHER "0" OR "VDD"

5) SINCE WL STILL HIGH, DATA IS
   WRITTEN BACK INTO THE CELLS ON
   THAT WORD LINE
WRITE SEQUENCE

1) READ ENTIRE ROW

2) MODIFY CONTENT OF ONE (OR MORE) READ REGISTERS

3) WRITE BACK ALL BL & BL

THIS PERFORMS A REFRESH OF ROW

REFRESH SEQUENCE

1) READ ONE ROW AT A TIME

2) REPEAT WHEN YOU GET TO LAST ROW

REFRESH INTERVAL 8 FEW MILLISECONDS FOR ENTIRE MEMORY