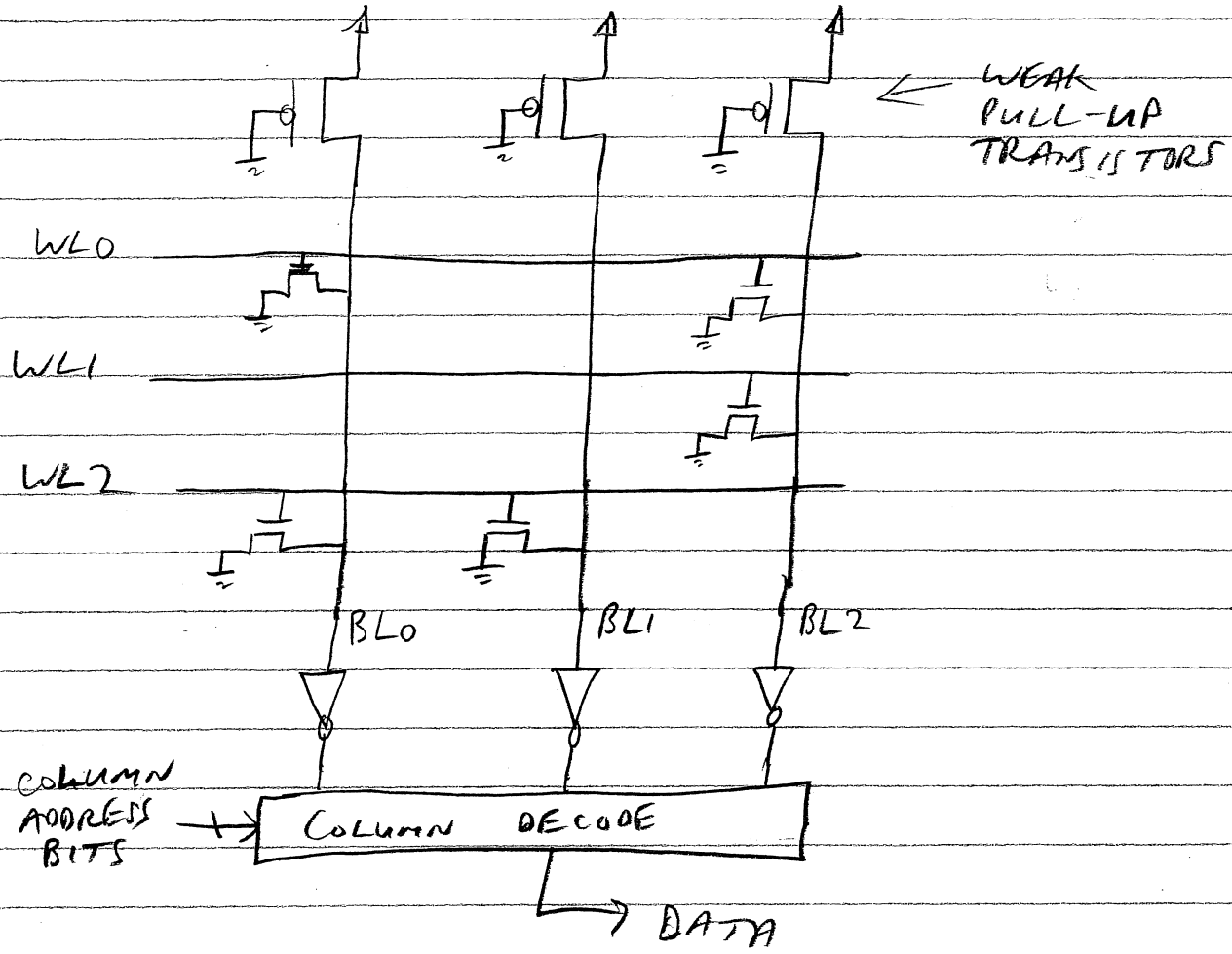
NOR ROM MEMORY



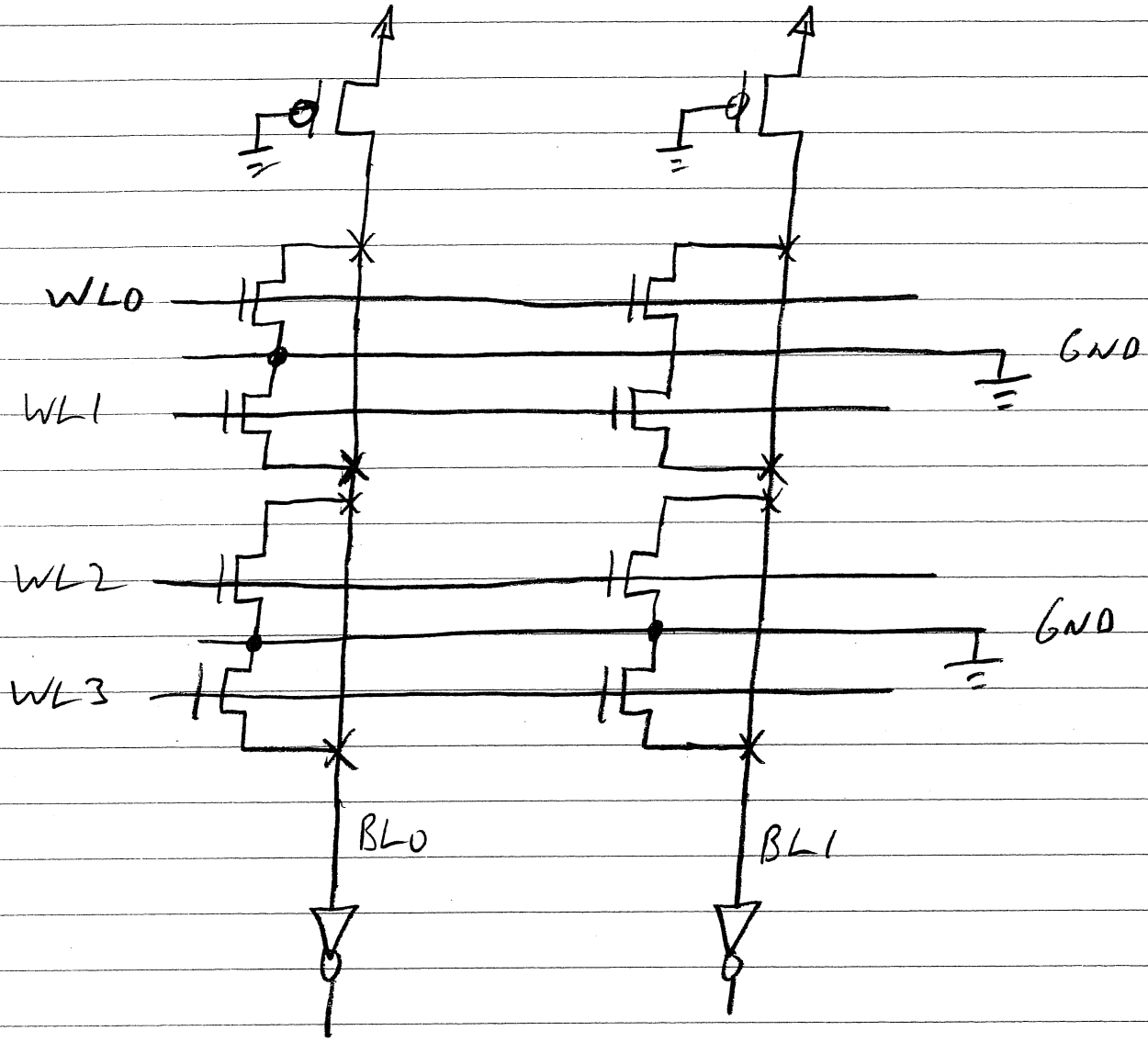
- ONE WL SELECTED (HIGH WHILE REST LOW)
- IN ABOVE EXAMPLE, MEMORY STORED IS

1	0	1
0	0	1
1	1	0

- TRANSISTOR PRESENT INDICATES A "1"

M33A

NOR ROM LAYOUT (4x2)



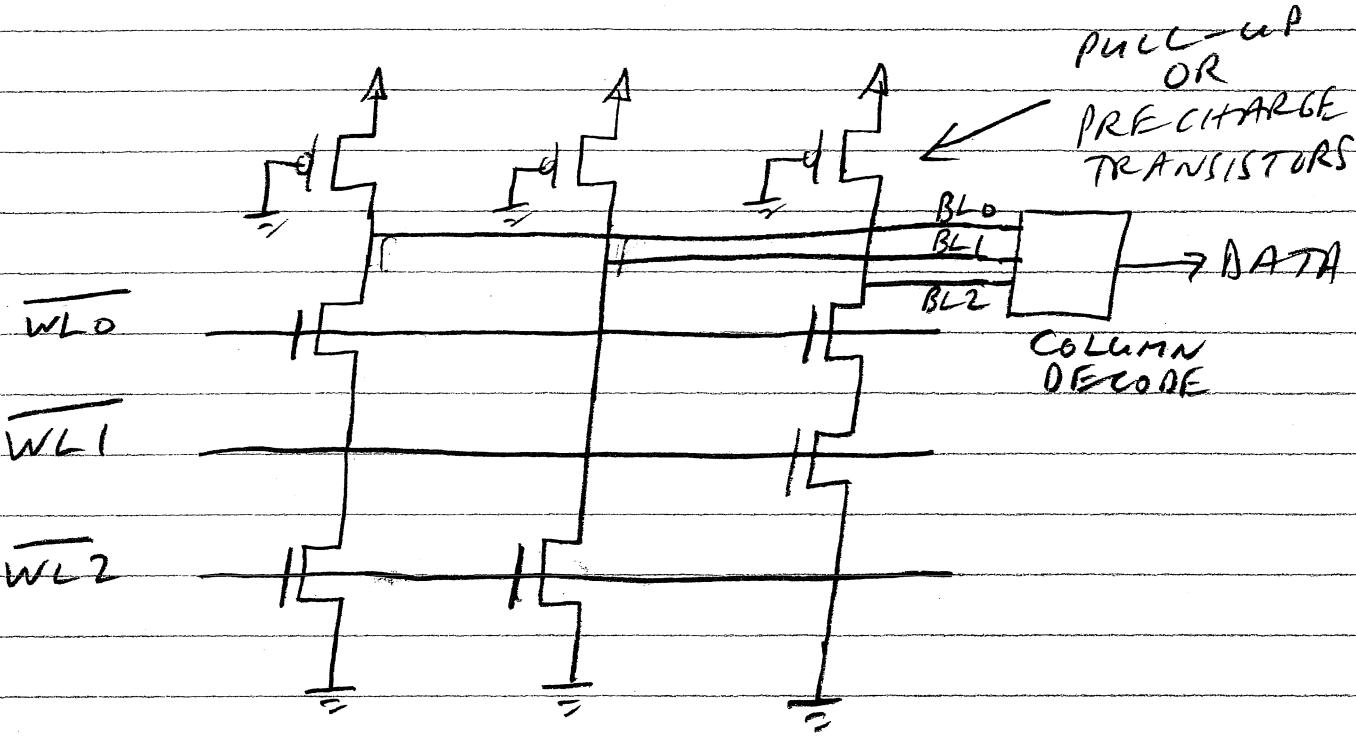
- ALL TRANSISTORS PRESENT
- PROGRAM THROUGH CONTACTS AT "X" EITHER PRESENT OR NOT
- SHARE GND LINES BETWEEN PAIRS OF ROWS

- BENEFIT OF WEAK-PULL UP PMOS TRANSISTORS IS THAT NO CLOCK IS REQUIRED

- CAN REDUCE POWER BY HAVING BIT LINES PRECHARGE HIGH (REQUIRES A CLOCK) INSTEAD.

- NOR ROM NOT AREA EFFICIENT - SINCE GROUND LINE & CONTACTS NEEDED IN ROM CELLS.

NAND ROM MEMORY

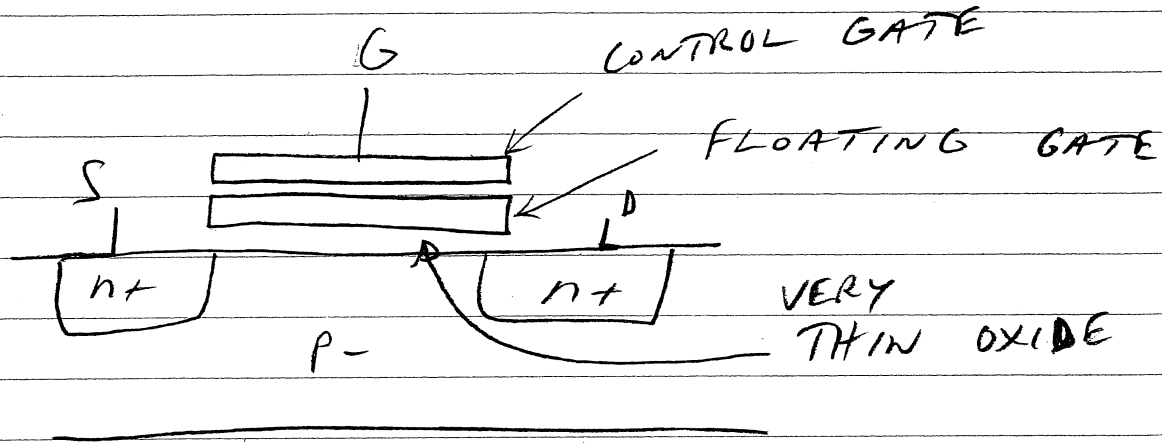


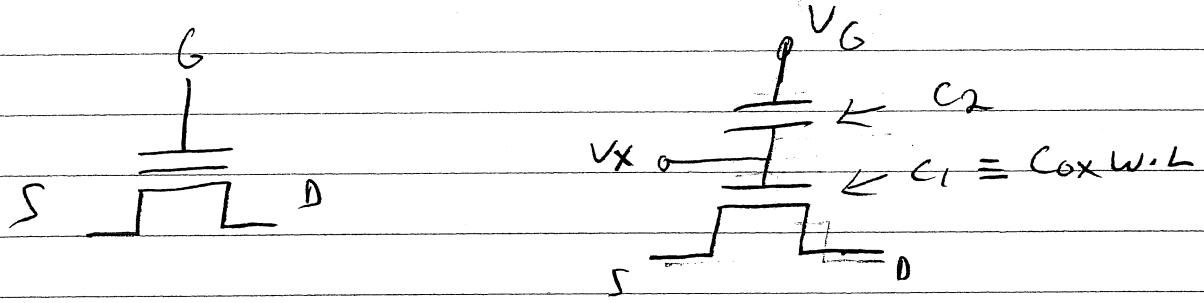
- SLOWER THAN NOR ROM
- DENSER THAN NOR ROM

ABOVE EXAMPLE, MEMORY STORED...

1	0	1
0	0	1
1	1	0

EEPROM & FLASH MEMORY





$$\Delta V_x = \frac{C_2}{C_1 + C_2} \Delta V_G$$

V_{X_0} ← INITIAL V_x

V_{G_0} ← INITIAL V_G

$$V_x - V_{x_0} = \left(\frac{C_2}{C_1 + C_2}\right)(V_G - V_{G_0})$$

ASSUMING $V_{G_0} = 0$

THEN

$$V_x = V_{x_0} + \left(\frac{C_2}{C_1 + C_2}\right) V_G$$

FOR TRANSISTOR TO TURN ON

$$V_x \geq V_{tN}$$

$$V_{x_0} + \left(\frac{C_2}{C_1+C_2}\right)V_G \geq V_{tN}$$

$$V_G \geq \left(\frac{C_1+C_2}{C_2}\right)\left(V_{tN} - V_{x_0}\right)$$

DEFINE

$$V_{tN}' = \left(\frac{C_1+C_2}{C_2}\right)\left(V_{tN} - V_{x_0}\right)$$

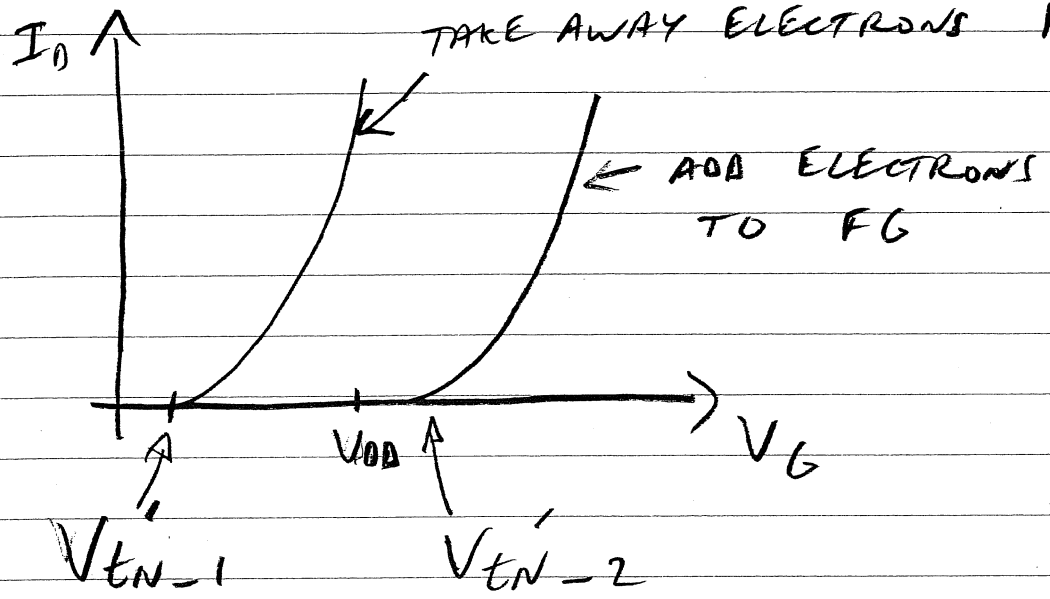
"EFFECTIVE" THRESHOLD OF TRANSISTOR

CAN CHANGE V_{tN}'

BY ADDING OR TAKING AWAY ELECTRONS ON FLOATING GATE (FG) $\Rightarrow$ CHANGES V_{x_0}

ADD ELECTRONS $\Rightarrow V_{x_0} < 0$

REMOVE ELECTRONS $\Rightarrow V_{x_0} > 0$



V_{tN_1} => NORMAL TRANSISTOR

V_{tN_2} => ALWAYS OFF TRANSISTOR FOR $V_G \leq V_{DD}$

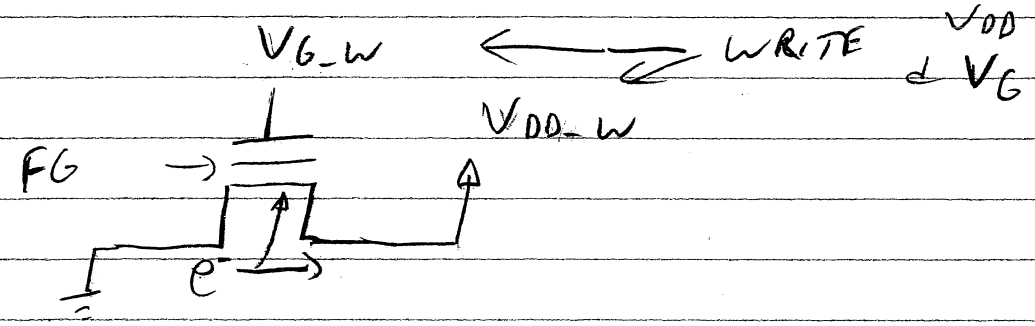
3 METHODS TO ADD/REMOVE ELECTRONS

1) HOT CARRIER INJECTION (OR AVALANCH INJECTION)
   => ADDS ELECTRONS TO FG

2) PHOTO ELECTRIC EFFECT
   => REMOVES ELECTRONS FROM FG

3) FOWLER-NORDHEIM TUNNELING
   => ADD/REMOVE ELECTRONS FROM FG

1) HOT CARRIER INJECTION (HCI)



- V_{DD_W} & V_{G_W} ARE LARGE V_{DD} VOLTAGES

= HIGH ELECTRIC FIELD IN CHANNEL ACCELERATES ELECTRONS TO HIGH VELOCITY
⇒ HOT CARRIERS

- FRACTION OF ELECTRONS COLLIDE & PASS THROUGH SiO_2 TO FLOATING GATE (FG)

- AS NEGATIVE CHARGE BUILDS UP ON FG, TRANSISTOR TURNS OFF & INJECTION STOPS
⇒ SELF-LIMITING PROCESS

2) PHOTOELECTRIC EFFECT

- SHINING LIGHT (UV LIGHT) MAKES SiO_2 SLIGHTLY CONDUCTIVE & ELECTRONS LEAK FROM FG BACK TO SUBSTRATE/SOURCE

- ERASES BIT

- REQUIRES A PACKAGE WITH TRANSPARENT WINDOW ↓ COVER

EPROM => ERASABLE PROM
USE UV LIGHT TO ERASE.

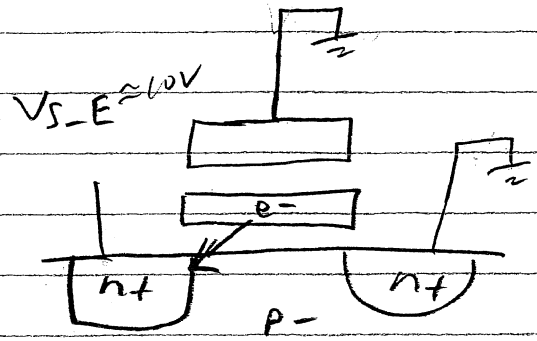
3) FOWLER-NORDHEIM TUNNELING

APPLY HIGH ELECTRIC FIELD ACROSS THIN SiO_2 + ELECTRONS "TUNNEL"

ACROSS SiO_2

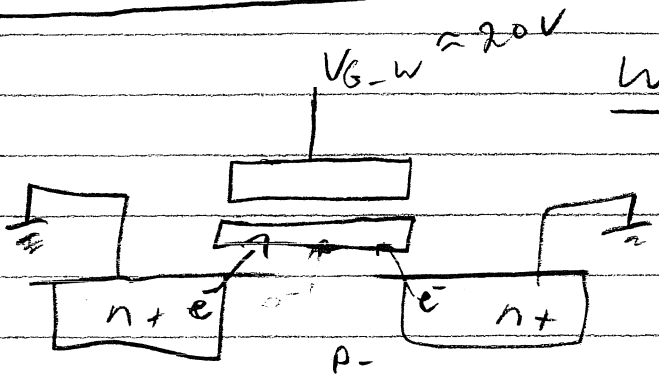
ELECTRIC FIELD $\hat{=} 10^7$ V/cm

- LESS DAMAGING TO SiO_2 THAN HCI
- LARGER # OF WRITE CYCLES



ERASE

- V_{S_E} IS HIGH VOLTAGE
- ERASES BIT
- NOT SELF-LIMITING => CAN MAKE $V_{tN}' < 0$
- TYPICALLY WRITE ALL BITS TO BE ERASED TO 1, THEN ERASE BITS WITH PULSED V_{S_E} FOR LENGTH OF TIME.

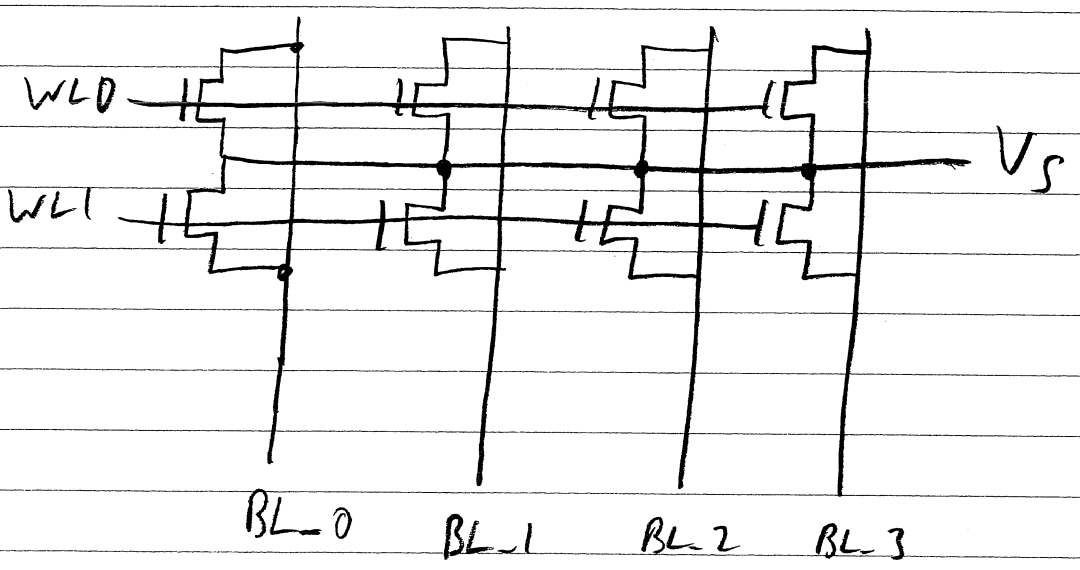


WRITE

- SLOWER THAN HCI
- VERY LITTLE CURRENT COMPARED TO HCI

NOR FLASH

ALL BITS INITIALLY "1"



- TO PROGRAM WL1, BL_1 TO "0"

$WL_1 = V_{G_W}$, $BL_1 = V_{DA_W}$

$V_S = 0$ (HCI)

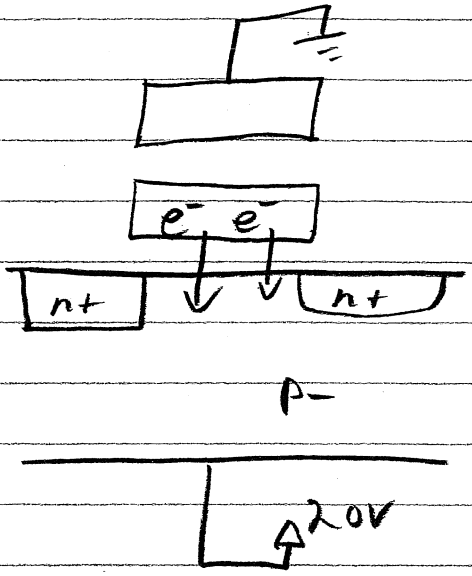
- TO ERASE ALL BITS BACK TO "1"

$WL0 = WL1 = 0$ ALL $BL = 0$

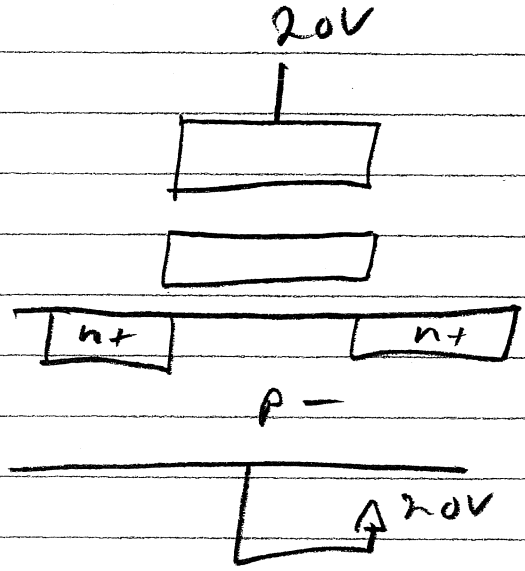
$V_S = V_{S_E}$ FOR A PULSE OF TIME

(FNT)

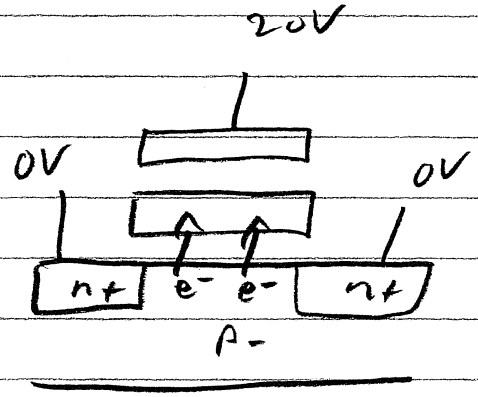
NAND FLASH



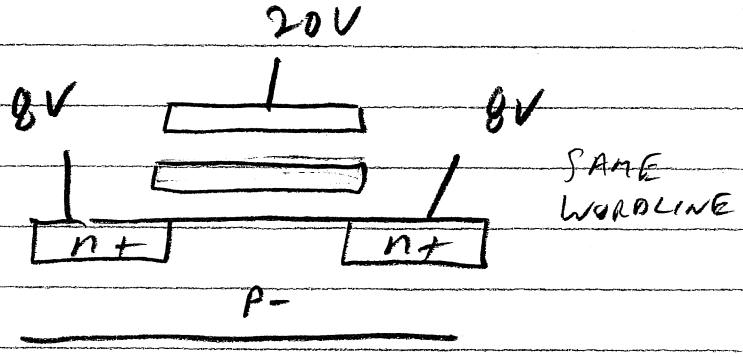
ERASE

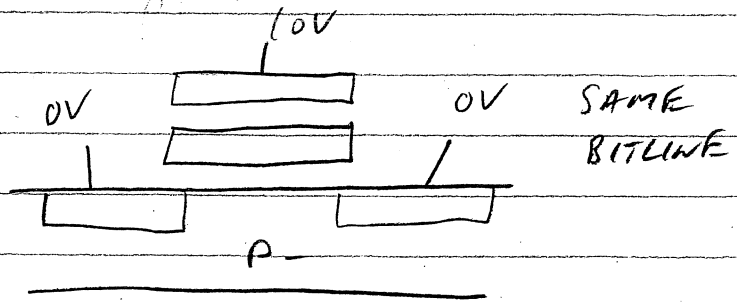


ERASE INHIBIT

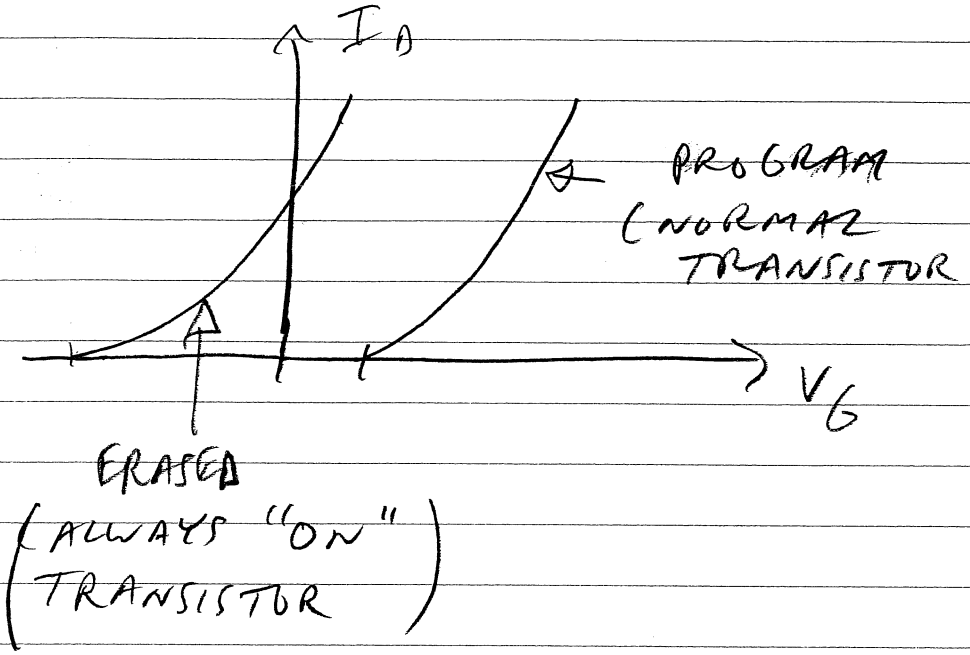


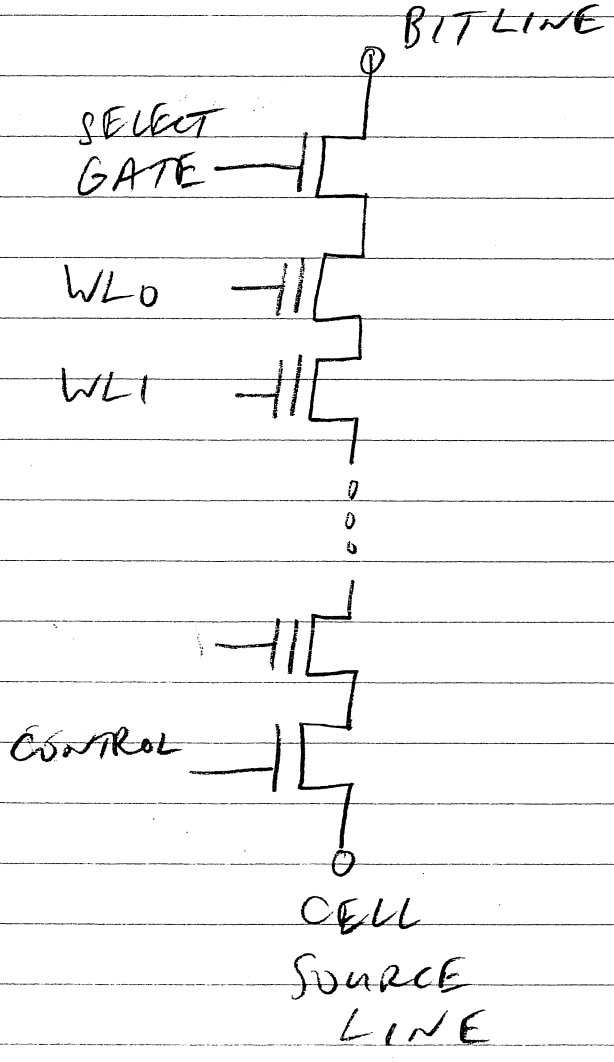
PROGRAM (WRITE)





PROGRAM INHIBIT


I_D
PROGRAM
(NORMAL
TRANSISTOR
V_G
ERASED
(ALWAYS "ON"
TRANSISTOR)


BIT LINE
SELECT
GATE
WL0
WL1
CONTROL
CELL
SOURCE
LINE

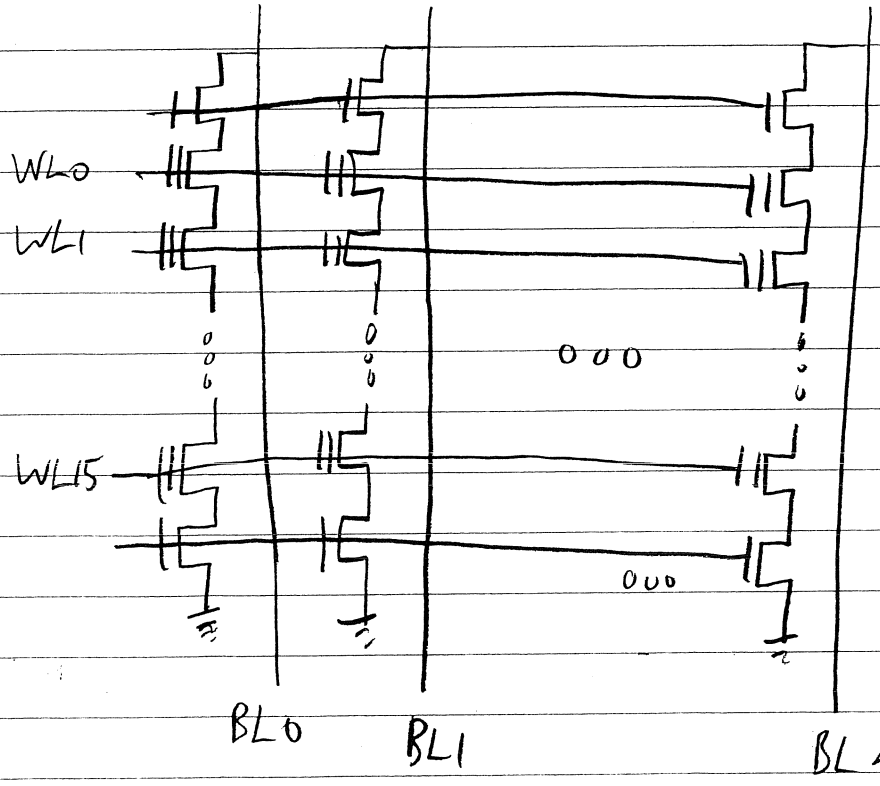
NAND FLASH MADE UP OF BLOCKS WHICH IN TURN ARE MADE UP OF PAGES

MEMORY IS WRITTEN 1 PAGE AT A TIME

MEMORY IS ERASED 1 BLOCK AT A TIME

TYPICAL BLOCK 8kB = 64kb

TYPICAL PAGE 512 B = 4kb



1 Block

= 16 x 4096

= 64 kb