NOR ROM MEMORY

- One WL selected (High while rest low)

- In above example, memory stored is

  1 0 1
  0 0 1
  1 1 0

- Transistor present indicates a "1"
- ALL TRANSISTORS PRESENT
- PROGRAM THROUGH CONTACTS AT "X" EITHER PRESENT OR NOT
- SHARE GND LINES BETWEEN PAIRS OF ROWS
- Benefit of weak-pull up PMOS transistors is that no clock is required.

- Can reduce power by having bit lines precharge high (requires a clock) instead.

- Nor ROM not area efficient since ground line & contacts needed in ROM cells.
NANO ROM MEMORY

- Slower than NOR ROM
- Denser than NOR ROM

Above example, memory stored...

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
EEPROM & FLASH MEMORY

**Diagram:**
- Control Gate (G)
- Floating Gate
- Very Thin Oxide

**Equations:**

\[ \Delta V_x = \frac{C_2}{C_1 + C_2} \Delta V_G \]

\[ V_{x-0} \leftarrow \text{INITIALIZE } V_x \]

\[ V_{G-0} \leftarrow \text{INITIALIZE } V_G \]

\[ V_x - V_{x-0} = \left( \frac{C_2}{C_1 + C_2} \right) (V_G - V_{G-0}) \]

Assuming \( V_{G-0} = 0 \)

Then

\[ V_x = V_{x-0} + \left( \frac{C_2}{C_1 + C_2} \right) V_G \]
For transistor to turn on

\[ V_x \geq V_{tn} \]

\[ V_{x-0} + \left( \frac{c_2}{c_1+c_2} \right) V_0 \geq V_{tn} \]

\[ V_0 \geq \left( \frac{c_1+c_2}{c_2} \right) (V_{tn} - V_{x-0}) \]

Define

\[ V'_{tn} = \left( \frac{c_1+c_2}{c_2} \right) (V_{tn} - V_{x-0}) \]

"Effective" threshold of transistor can change \( V'_{tn} \) by adding or taking away electrons on floating gate \( \Rightarrow \) changes \( (F_G) \)

\[ V_{x-0} \]

Add electrons \( \Rightarrow V_{x-0} < 0 \)

Remove electrons \( \Rightarrow V_{x-0} > 0 \)
3 METHODS TO ADD/REMOVE ELECTRONS

1) HOT CARRIER INJECTION
   (OR AVALANCHE INJECTION)
   => ADDS ELECTRONS TO FG

2) PHOTO ELECTRIC EFFECT
   => REMOVES ELECTRONS FROM FG

3) FOWLER-NORDHEIM TUNNELING
   => ADD/REMOVE ELECTRONS FROM FG

\( V_{TN-1} \Rightarrow \text{NORMAL TRANSISTOR} \)

\( V_{TN-2} \Rightarrow \text{ALWAYS OFF TRANSISTOR FOR } V_G \leq V_{dd} \)
1) HOT CARRIER INJECTION (HCI)

\[ V_{G,W} \leftarrow \text{WRITE} \downarrow V_{G} \]
\[ V_{DD,W} \]
\[ F_G \rightarrow \]
\[ e^+ \]

\[ V_{DD,W} + V_{G,W} \text{ ARE LARGE } V_{DD} \text{ VOLTAGES} \]

- HIGH ELECTRIC FIELD IN CHANNEL ACCELERATES ELECTRONS TO HIGH VELOCITY
  =) HOT CARRIERS

- FRACTION OF ELECTRONS COLIDE & PASS THROUGH SiO2 TO FLOATING GATE (F_G)

- AS NEGATIVE CHARGE BUILDS UP ON F_G, TRANSISTOR TURNS OFF & INJECTION STOPS
  =) SELF-LIMITING PROCESS
2) **PHOTOELECTRIC EFFECT**

- SHINING LIGHT (UV LIGHT) MAKES SiO₂ SLIGHTLY CONDUCTIVE 
  ELECTRONS LEAK FROM FG BACK TO SUBSTRATE/SOURCE

- ERASES BIT

- REQUIRES A PACKAGE WITH TRANSPARENT WINDOW + COVER

**EPROM =) ERASABLE PROM**

USE UV LIGHT TO ERASE.

3) **FOWLER-NORDHEIM TUNNELING**

APPLY HIGH ELECTRIC FIELD ACROSS THIN SiO₂ + ELECTRONS "TUNNEL"

ACROSS SiO₂

**ELECTRIC FIELD ~ 10⁷ V/cm**

- LESS DAMAGING TO SiO₂ THAN HCI
- LARGER # OF WRITE CYCLES
- $V_{SE} \leq 10\text{V}$
- "ERASE"
- $V_{SE}$ IS HIGH VOLTAGE
- ERASES BIT
- NOT SELF-LIMITING => CAN MAKE $V_{EN} < 0$

- TYPICALLY WRITE ALL BITS TO BE ERASED TO 1, THEN ERASE BITS WITH PULSED $V_{SE}$ FOR LENGTH OF TIME.

- $V_{SW} = 20\text{V}$
- "WRITE"

- SLOWER THAN HCI
- VERY LITTLE CURRENT COMPARED TO HCI
FLASH

- ALL BITS INITIALLY "1"

- TO PROGRAM WL1, BL-1 TO "0"

  \[\text{WL1} = V_G - W, \quad \text{BL-1} = V_{DD} - W\]

  \[\text{VS} = 0 \quad \text{(HCl)}\]

- TO ERASE ALL BITS BACK TO "1"

  \[\text{WL0 = WL1 = 0, ALL BL = 0}\]

  \[\text{VS} = \text{VS}_E \text{ FOR A PULSE OF TIME} \quad \text{(FNT)}\]
NAND FLASH

ERASE

PROGRAM (WRITE)

ERASE INHIBIT

SAME WORDLINE

SAME BITLINE

PROGRAM INHIBIT
Program (Normalized Transistor)

Erased (Always "On"

Transistor)

Bitline

Select Gate

WL0

WL1

Control

Cell

Source Line
NAND flash is made up of blocks which in turn are made up of pages.

Memory is written 1 page at a time.

Memory is erased 1 block at a time.

Typical block 8kB = 64kB

Typical page 512B = 4kB

```
WL0  WL1  WL15
BL0  BL1  BL4095
```

1 Block

\[ = 16 \times 4096 \]

\[ = 64 \text{ kB} \]