SYNCHRONIZERS & METASTABILITY.

CONSIDER AN ASYNCHRONOUS SIGNAL OR 2 DIFFERENT CLOCK DOMAINS.

POOR CLOCK DOMAIN CROSSING

CLOCK DOMAIN 1

CLOCK DOMAIN 2

ERROR

Q1 ≠ Q2
ERROR SINCE $Y_1$ AND $Y_2$ MAY HAVE DIFFERENT DELAYS

BETTER SOLUTION 1

ERROR $Y$ SHOULD HAVE REMAINED HIGH BUT PICKED UP A GLITCH
Better Solution 2

Glitch Free

Error due to metastability!!

Sampling X at V_m + unknown t_{PCQ}
BETTER (BEST) SOLUTION

1 LATCH
TO
ELIMINATE
GLITCHES

2 LATCHES
TO REDUCE
METASTABILITY
ERRORS

(MORE LATCHES
FURTHER REDUCES METASTABILITY
ERRORS BUT USUALLY
2 IS ENOUGH TO
REDUCE ERROR TO

Perhaps 1 ERROR IN 1000 YEARS.

REGULAR
CLOCK 2
SYSTEM.
SAMPLING A DATA TRANSITION INTO AN INVERTER WITH NO POSITIVE FEEDBACK

\[ T_D \]

\[ T_D \quad \text{INT} \quad \text{PLUS} \quad \text{VNC} \quad \text{VCL} \quad \text{CHANGES ONCE} \]

\[ T_{C} \quad \text{COULD BE ANY PHASE} \]

\[ \Phi \quad \text{OUTPUT } \]

\[ P_{ERROR} = \frac{T_{PD}}{T_{C}} \quad \text{ASSUMING } T_{C} > T_{PD} \]

EXAMPLE

\[ T_{PD} = 100 \text{ps} \]

\[ T_{C} = 10 \text{ns} = \Rightarrow f_{CLK} = 100 \text{MHz} \]

\[ P_{ERROR} = \frac{100 \text{ps}}{10 \text{ns}} = 0.01 \quad \text{OR} \quad 1\% \]
Sampling a single data transition into a latch with positive feedback

Assume $V_m$ is latch threshold.

$V_m$ grows exponentially with 1st order time constant due to positive feedback.
\[ V_x(t) = V_m + (V_x(0) - V_m) e^{\frac{t}{T_s}} \]

WHERE \( T_s \) IS LATCH TIME CONSTANT

\( T_s \) DEPENDS ON
- \( g_m \) OF TRANSISTORS
- INTERNAL CAPACITANCES

SO IF WE WAIT \( T \) SECONDS BEFORE USING SIGNAL

\[ P_{\text{error}} = \frac{\text{trd}}{T_c} \left( e^{-\frac{T}{T_s}} \right) \]

BECAUSE SAMPLED SIGNAL CAN BE \( T_s \) TIMES SMALLER

IF \( N \) DATA TRANSITIONS/SECOND (ON AVERAGE)

\[ P_{\text{errs}} = \frac{N \cdot \text{trd}}{T_c} e^{-\frac{T}{T_s}} \quad \text{[ERRORS/SECOND]} \]

(ON AVERAGE)
MEAN TIME BETWEEN FAILURES

\[
MTBF = \frac{1}{P_{err/s}} = T_c e^{\frac{T_c}{t_{rd}}} \leq \left( \frac{T_0}{t_{rd}} \right)_{in\ textbook}
\]

IF DATA HAS N TRANSITIONS/SECOND CAN DEFINE

AVERAGE TRANSITION FREQUENCY

\[ F_0 = \frac{N}{T_c} \]

+ CLOCK FREQ \( F_{CLK} = \frac{1}{T_c} \)

\[ F_{CLK} \]

+ DEFINE \( k_1 = \frac{1}{t_{rd}} \)

\[ MTBF = k_1 e^{\frac{T_c}{t_{rd}}} \]

\[ \frac{F_0}{F_{CLK}} \]

\[ T = T_c \text{ if 2 FLOP SYNCHRONIZER USED and } T_{setup} \text{ ignored} \]

EXAMPLE

\[ \text{GIVEN } t_{rd} = 15\text{ps}, T_c = 20\text{ps} \]

ASSUMING DATA AVERAGE TRANSITION FREQ \( F_0 \)

\[ F_0 = 50\text{MHz} \]
a) **Find max clock rate** if 2 flop synchronizer used and MTBF ≥ 1000 years

1000 years = 1000 × 60 × 60 × 24 × 365 = 3.15 × 10^10 seconds

\[
3.15 \times 10^{10} = \frac{T_c e^{(T_c/20 ps)}}{(5 \times 10^6)(15 \times 12)}
\]

**Trial & error gives** \( T_c = 760 \) ps

\( \text{Fclk} = 1.32 \) GHz

b) **Find MTBF** if Fd = 1 kHz and Fclk = 100 MHz

2 flop synchronizer used

\[
\text{MTBF} = \left( \frac{1}{15 \text{ps}} \right) \left( \frac{e^{(10^{10}/20 ps)}}{(1 \times 10^3)(10^8)} \right)
\]

= \( 2.97 \times 10^{29} \) years

C) **Find MTBF** if Fd = 1 kHz and Fclk = 100 MHz

No synchronizer used

\[
\text{MTBF} = \left( \frac{1}{15 \text{ps}} \right) \left( \frac{1}{(1 \times 10^3)(10^8)} \right) = 0.067 \text{ seconds}
\]
Communicating an N-Bit Data Word Across Clock Domains.

When N-Bit Data Stable (no synchronizer needed on data inputs)

4 Phase Handshake

Req High indicates data stable
Ack "" "" Data Read
Req Low "" Ack Received
Ack Low "" Req Low Received
2 PHASE

REQ CHANGES LOGIC LEVEL ==> DATA STABLE
ACK " " " " ==> DATA READ