2.4 Non-Ideal I-V Effects

1) Velocity Saturation
2) Channel Length Modulation
3) Body Effect
4) Subthreshold Conduction
5) Junction Leakage
6) Tunneling
7) Temperature Dependence
8) Geometry Dependence

1) Velocity Saturation

\[ I_D = \frac{\mu C_{ox} (V_{gs} - V_t)}{2} (V_{gs} - V_t)^2 \quad \text{(Active Region)} \]

\[ I_D \propto (V_{gs} - V_t)^2 \]

Velocity Saturation \[ I_D \propto (V_{gs} - V_t) \] not square law related

(As \( V_{os} \) increases)
2) CHANNEL-LENGTH MODULATION IN ACTIVE REGION

\[ I_{DS} = \frac{\mu n C_{ox}}{2} (V_{GS} - V_T)^2 (1 + \kappa V_{DS}) \]

Typically not important for digital design.
3) **Body Effect**  

$V_{TN}$ is a function of $V_{SB}$

$$V_{TN} = V_{TN0} + \gamma \left( \sqrt{V_{SB} + \phi_S} - \sqrt{\phi_S} \right)$$

$V_{TN0}$: Threshold voltage with $V_{SB} = 0$

$V_{SB}$: Source to substrate voltage

$\gamma$: Body effect coefficient $\gamma \approx 0.4$ $V^{1/2}$

Given for a device

$\phi_S$: Surface potential $\phi_S \approx 0.9$ $V$

Given for a device
Example

Given

\[ V_{t_0} = 0.4 \text{ V} \]
\[ \delta = 0.3 \sqrt{V} \]
\[ \phi_s = 0.9 \text{ V} \]

Find \( V_{tn} \) when \( V_{sb} = 1.5 \text{ V} \)

\[ V_{tn} = 0.4 + 0.3 \left( \sqrt{1.5 + 0.9} - \sqrt{0.9} \right) \]
\[ = 0.4 + 0.18 \]
\[ = 0.58 \text{ V} \]

\( V_{tn} \) increases as \( V_{sb} \) increases.
PASS TRANSISTOR LOGIC EXAMPLE

CASE I

CASE II
Given \( V_{DD} = 2 \text{ V} \), \( \phi_s = 0.9 \text{ V} \), \( \gamma = 0.3 \sqrt{\text{V}} \), \( V_{TN_0} = 0.4 \text{ V} \)

Find \( V_Y \) max for Case I + II

**Case I**

\[
C = V_{DD} = 2 \text{ V} \quad V_{SB} = 0
\]

\[
A = V_{DD} = 2 \text{ V} \quad V_{SB} = 0
\]

\[
V_{TN} = V_{TN_0} = 0.4 \text{ V}
\]

\[
V_Y(\text{max}) = V_{DD} - V_{TN} = 1.6 \text{ V}
\]

**Case II**

\[
C = V_{DD} = 2 \text{ V} \quad V_{SB} = V_Y - 0 = V_Y
\]

\[
A = V_{DD} = 2 \text{ V}
\]

\[
V_{TN} = V_{TN_0} + \gamma \left( \sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s} \right)
\]

\[
V_{TN} = 0.4 + 0.3 \left( \sqrt{V_Y + 0.9} - \sqrt{0.9} \right)
\]

\[
V_Y = V_{DD} - V_{TN}
\]

\[
V_Y = 2 - \left[ 0.4 + 0.3 \left( \sqrt{V_Y + 0.9} - \sqrt{0.9} \right) \right] \quad 0
\]

**Non-linear Equation**

Solve by Iteration
ESTIMATE $V_{y_1} = 1.6\, V$

FROM RHS of (1)

$V_{y_2} = 2 - [0.4 + 0.3(\sqrt{V_{y_1} + 0.9} - \sqrt{0.9})]$

$V_{y_2} = 1.41$

ESTIMATE $V_{y_2} = 1.41\, V$ & use RHS of (1) AGAIN

$\Rightarrow V_{y_3} = 1.43$

$\Rightarrow V_{y_4} = 1.43$ \underline{DONE}

$V_{y\, (max)} = 1.43\, V$

LOWER BY $0.17\, V$ THAN CASE I
4) **Subthreshold Conduction**

Ideally $I_D = 0$ for $V_{GS} < V_T$ (NMOS)

\[ I_D = I_{D0} e^{\frac{V_{GS} - V_T}{nV_T}} \left[ 1 - e^{-\frac{V_{GS} - V_T}{V_T}} \right] \]

$I_D = I_{D0}$ when $V_{GS} = V_T$

\[ V_T = \frac{kT}{q} \approx 25 \text{ mV at room temp} \]

$n \rightarrow$ process dependent
THE TERM \[ \left( 1 - e^{-\frac{V_{os}}{V_T}} \right) \]

ENSURES \( I_0 \to 0 \) AS \( V_{os} \to 0 \)

BUT IT IS APPROX. 1

WHEN \( V_{os} \gg V_T \) \( V_T \approx 25mV \) AT ROOM TEMP
Example

Given \( n = 1.5 \) and \( V_{CS} \) process

Find \( V_T \) (threshold) so that

\[
I_D \text{ at } V_{GS} = 0 = \frac{I_D \text{ at } V_{GS} = V_T}{1000} \quad \text{Worst Case}
\]

\[
I_D \text{ at } V_{GS} = 0 = I_{D0} e^{-\frac{V_{GS} - V_T}{\mu V_T}} \left(1 - e^{-\left(-\frac{1}{25\text{mV}}\right)}\right) = \frac{I_{D0}}{1000}
\]

\[
\approx 1
\]

\[
\frac{1}{1000} = e^{-\frac{V_T}{(1.5)(25\text{mV})}}
\]

\[
V_T = -(1.5)(25\text{mV})(\ln 10^{-3}) = 260\text{mV}
\]

\[
\frac{260}{3} \approx 90\text{mV/Decade of Current}
\]

\[\log\left(\frac{I_D}{I_{D0}}\right)\]
5) Junction Leakage

Reverse biased diodes leak some current.

Small \( I_s \approx 0.1 \Rightarrow 0.01 \text{ FA/} \mu \text{m}^2 \)

Increases exponentially with increasing temperature.

6) Tunneling

Gate oxides so thin, electrons can "jump" through thin oxide.

Used in EEPROM, flash memory.

Limits gate oxide thicknesses in modern technologies.
7) **TEMPERATURE**

- Increasing temp decreases mobility of electrons & holes.

- Increasing temp increases tunneling & junction leakage.

- Increasing temp decreases Vt & therefore increases subthreshold current.

- Increased temp reduces lifetime of devices.

- Increase temp \( \Rightarrow \) worse digital performance.

  Limit of \( T < 125^\circ C \) junction temp

  Need heat sinks or fans.
8) GEOMETRY DEPENDENCE

\[ L_{\text{drawn}} \]

\[ \text{S} \quad \text{G} \quad \text{D} \]

\[ W_{\text{drawn}} \]

\[ \text{L}_{\text{drawn}} \]

\[ \text{S} \quad \text{n}^+ \quad \text{n}^+ \]

\[ L_x \quad L_x \]

\[ L_{\text{eff}} \Rightarrow L \text{ "effective"} \]

\[ L_{\text{eff}} \text{ is actual transistor length} \]

\[ L_{\text{eff}} = L_{\text{drawn}} - 2L_x \]

\[ L_{\text{drawn}} \text{ is what is shown on schematics and layout} \]

\[ L_{\text{eff}} \text{ is what is actually in transistors} \]
SIMILAR FOR WEFF

\[ \text{WEFF} = W_{\text{DRAWN}} - 2W_x \]

FOR EXAMPLE, SAY \[ W_x = 0.1 \text{ mm} \]
2\(L_x\) = 0.05 \text{ mm}
AND WANT \[ I_2 = 2I_1 \]

FIRST TRY

\[ \begin{align*}
V_{G51} & = V_{G52} \\
\text{WEFF}_1 & = W_{\text{DRAWN}} - 2W_x \\
& = 0.8 \text{ mm} \\
\text{LEFF}_1 & = L_{\text{DRAWN}} - 2L_x \\
& = 0.2 \text{ mm} \\
\end{align*} \]

\[ \frac{\text{WEFF}_1}{\text{LEFF}_1} = \frac{0.8}{0.2} = 4 \]
\[ W_{\text{EFF}2} = W_{\text{DRAWN}2} - 2W_L = 1.8 \ \mu m \]
\[ L_{\text{EFF}2} = L_{\text{DRAWN}2} - 2L_X = 0.2 \ \mu m \]

\[ \frac{W_{\text{EFF}2}}{L_{\text{EFF}2}} = \frac{1.8}{0.2} = 9 \]

\[ \frac{W_{\text{EFF}2}}{L_{\text{EFF}2}} = 2 \left( \frac{W_{\text{EFF}1}}{L_{\text{EFF}1}} \right) \text{ so } I_2 = 2I_1 \]

**Better Approach**

\[ I_{2A} = I_{2B} = I_1 \text{ since all same } \frac{W_{\text{EFF}}}{L_{\text{EFF}}} \]

\[ I_2 = I_{2A} + I_{2B} \]

So \[ I_2 = 2I_1 \]
There still exists random variations to make

\[ I_2 = 2I_1 \]

But second approach is much better

In addition, some designs are optically "shrunk" where all lengths and/or widths are shrunk by fixed amounts

This is another reason to use second approach.