IC Packaging

- Connects signals and power between chip and printed circuit board (PCB) with little delay and distortion
- Removes heat from chip
- Protects chip from mechanical damage and thermal expansion stress
- Is low cost

Two main types

- Through-hole pins
  - Pass through PCB and soldered from below

- Surface mount technology (SMT)
  - Soldered to surface of PCB

- Through-hole less dense as holes require more spacing and block inner board traces, also more inductance
### Through-Hole Types

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP - Dual Inline Package</td>
<td>8-64</td>
</tr>
<tr>
<td>PGA - Pin Grid Array</td>
<td>64-400</td>
</tr>
</tbody>
</table>

### SMT Types

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOIC - Small Outline IC</td>
<td>8-28</td>
</tr>
<tr>
<td>TSOP - Thin Small Outline Package</td>
<td>8-100</td>
</tr>
<tr>
<td>PLCC - Plastic Ledless Chip Carrier</td>
<td>20-84</td>
</tr>
<tr>
<td>QFP - Quad Flat Pack</td>
<td>44-240</td>
</tr>
<tr>
<td>BGA - Ball Grid Array</td>
<td>50-2000</td>
</tr>
</tbody>
</table>

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**Diagram:**

- **Bond Pad**
- **Bond Wire**
- **Lead Frame**
  - (Pin when visible)
Bond pad adds capacitance.
Bond wire adds inductance.
Lead frame adds inductance.
Also mutual inductance and capacitance between bond wires and lead frames.

\[ \text{Simple model} \]

\[ \text{CHIP} \quad \text{LBW} \quad \text{PCB} \]

\[ \quad \text{CBP} \quad \text{Cp} \]

Bond bond pin/board.
Pad wire capacitance.

Bond pad capacitance \( \approx 0.1 \text{pF} \).
Bond wire \( \approx 1 \text{mH/mm} \) length 1-5 mm.

\[ \text{Cp} \approx 0.5 \text{pF} \]
**FLIP CHIP**

- Eliminates bond wire
- Solder balls on top of chip
- Attach directly to package or PCB
HEAT DISSIPATION

60W LIGHT BULB HAS SURFACE AREA OF 120 cm²

130W CPU HAS SURFACE AREA OF 4 cm² (CHIP)

60 x POWER DENSITY!!

(NOT FAIR SINCE FILAMENT IN LIGHT BULB HAS HIGH POWER DENSITY)

DEFINE Tj TO BE JUNCTION TEMPERATURE ON CHIP.

USUALLY A MAXIMUM Tj MAX IS SPECIFIED

3) TO MEET TIMING Tj MAX = 125°C

T_a DEFINED TO BE AMBIENT TEMPERATURE.
\( \Theta_{ja} \) defined to be

thermal resistance between junction and ambient [\( \degree C/W \)]

\( \Theta_{ja} \) is sum of thermal resistances

\( \Theta_{ja} = \Theta_{jp} + \Theta_{ph} + \Theta_{ha} \)

\( \Theta_{jp} \Rightarrow \text{junction} \Rightarrow \text{package} \)

\( \Theta_{ph} \Rightarrow \text{package} \Rightarrow \text{heat sink} \)

\( \Theta_{ha} \Rightarrow \text{heat sink} \Rightarrow \text{ambient} \)

\( T_j - T_a = \Theta_{ja} P \)

\( P \Rightarrow \text{chip power} \)
Ex

\[ \Theta_{jp} = 0.9 \, ^\circ C/w \]

\[ \Theta_{HA} = 4.0 \, ^\circ C/w \]

\[ \Theta_{PH} = 0.1 \, ^\circ C/w \text{ HEAT SINK ADHESIVE} \]

**Find Max Power Dissipated If**

\[ T_{j,\text{max}} = 100^\circ C \quad TA = 55^\circ C \]

\[ \Theta_{ja} = 0.9 + 4 + 0.1 = 5.0 \, ^\circ C/w \]

\[ P = \frac{T_j - TA}{\Theta_{ja}} = \frac{45}{5} = 9 \, W \]

*What if heat sink made perfect (i.e. \( \Theta_{HA} = 0 \))

\[ \Rightarrow \Theta_{ja} = 1.0 \, ^\circ C/w \Rightarrow P = 45 \, W \]