POWER DISTRIBUTION

IR DROP

V_DD

V_SS

V_DD

V_SS Logic CELLS

IR DROP

V_DD

Logic

V_DD and V_SS SAME SIDE

BETTER THAN HAVING
EX

64 REPEATERS \( V_{DD} = 1.8 \) V

Each Power Bus is 320 \( \mu \)m Long
1 \( \mu \)m Wide

Resistance is 0.05 \( \Omega/\mu \)m

Repeaters Each Drive 0.4 \( pf \) + Desired 200 ps Transition

Estimate Power Supply Drop.

SOLN

For Each Repeater

\[ I = C \frac{\Delta V}{\Delta t} = (0.4 \text{pf}) \frac{1.8 \text{V}}{200 \text{ps}} = 3.6 \text{mA} \]

Each Power Bus Has 320 \( \Omega \) \( \Rightarrow \) 16 \( \Omega \)

R Total
\[ V_{64} = 1.8 - \left[ \left( \frac{R_{\text{Total}}}{64} \right) (64)(3.6) + \left( \frac{R_{\text{Total}}}{64} \right) (63)(3.6) + \ldots + \left( \frac{R_{\text{Total}}}{64} \right) (1)(3.6) \right] \]

\[ = 1.8 - \left( \frac{R_{\text{Total}}}{64} \right) (3.6) \sum_{i=1}^{64} i \]

\[ = 1.8 - \frac{R_{\text{Total}}}{64} (3.6) \frac{64(65)}{2} \]

\[ = 1.8 - 64 \left( \frac{R_{\text{Total}}}{64} \right) \frac{(1)}{2} \]

\[ = 1.8 - 1.85v \quad \text{LESS THAN 0.151} \]

**Actually, power supply will drop, slow down gates, and "I" will drop (AT)**

**Power supply might drop 30\(^\circ\)C and delay gates and miss timing!!**
Also need to be conserved with \( \frac{d}{dt} \) of power bus inductance mostly due to bond wires.

If a 16Hz chip can transition from idle (2A) to full power (6A) in one clock cycle, estimate power supply drop if no bypass capacitance.
CAPACITOR \[ I = C \frac{dV}{dt} \]

INDUCTOR \[ V = L \frac{di}{dt} \]

\[ V = (100 \, \text{pH}) \frac{(6-2)}{(1 \, \text{mH})} = 0.4 \, V \] (ACROSS BOTH 50 pF INDUCTORS)

SIGNIFICANT.

**BY PASS CAPACITANCE**

![Circuit Diagram]

SECOND ORDER SYSTEM, NEED TO ENSURE NOT TOO MUCH RINGING

REQUIRED C FOR BYPASS CAN BE QUITE LARGE. FORTUNATELY ALOT COMES FROM LOGIC GATES THEMSELVES
SYMBIOTIC BYPASS CAPACITANCE

\[ C = C_{gs4} \text{ or } C_{gs3} \text{ depending whether } M_1 \text{ or } M_2 \text{ on} \]

Also as \( C_{gs3} \) charges up

\( C_{gs4} \) is discharged

\[ \frac{C_{gs2}}{2} \text{ is used as bypass capacitance} \]

Ex. A 0.18\,\text{µm} \text{ has } 2\,\text{fF/µm of gate capacitance. If transistor gates occupy } 90\% \text{ of chip area, calculate symbiotic bypass cap per (mm)}^2 \]
The number of transistors $N$ is given by:

$$N = \frac{2 \text{um}}{0.18 \text{ um}} = 5.55$$

So, if $100\%$ gate utilization,

$$2 \times 5.55 = 11 \text{ fF/\mu m}^2$$

At $90\%$ gate utilization,

$$11 \text{ fF/\mu m}^2 \times 90\% = 1 \text{ fF/\mu m}^2$$

Therefore, $\frac{C_{sym}}{C_{sym}} = 0.5 \text{ fF/\mu m}^2 \Rightarrow \text{HFAF IS } C_{sym}$

$$= 0.5 \text{ mF/\mu m}^2$$
IC IN BOTH VDD AND VSS WHEN CHARGING

- DC FOR BOTH WHEN DISCHARGING
0.5C in both cases

IN $V_{in}$ & $V_{SS}$