

Processing



Silicon Wafer

- Create 8-12 inch diameter cylinder (1m long) of single-crystalline silicon with light doping (usually p-)
- Ingot cut into wafers about 1mm thick

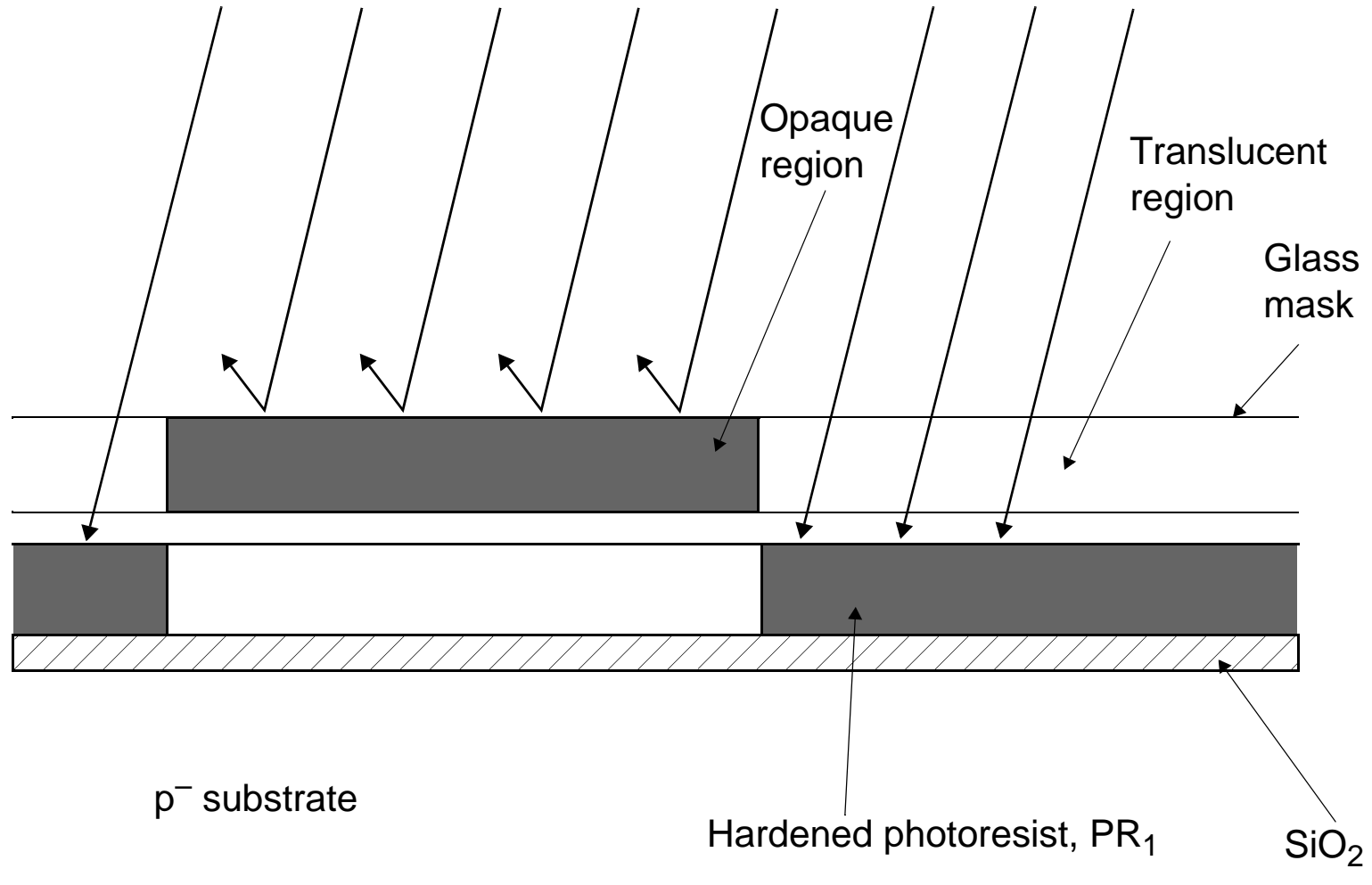
Photolithography

- Portions of silicon wafer are **masked out** so processing can be applied to remaining areas
- First create glass mask with dark areas using e-beam (cost of mask set \$25k-\$1M)
- Thermally grow SiO_2 on wafer, apply negative photoresist, align glass mask and expose to UV light
- Photoresist hardens (after baking) where exposed to light, remaining region removed (including SiO_2)
- Negative since SiO_2 remains where mask is light

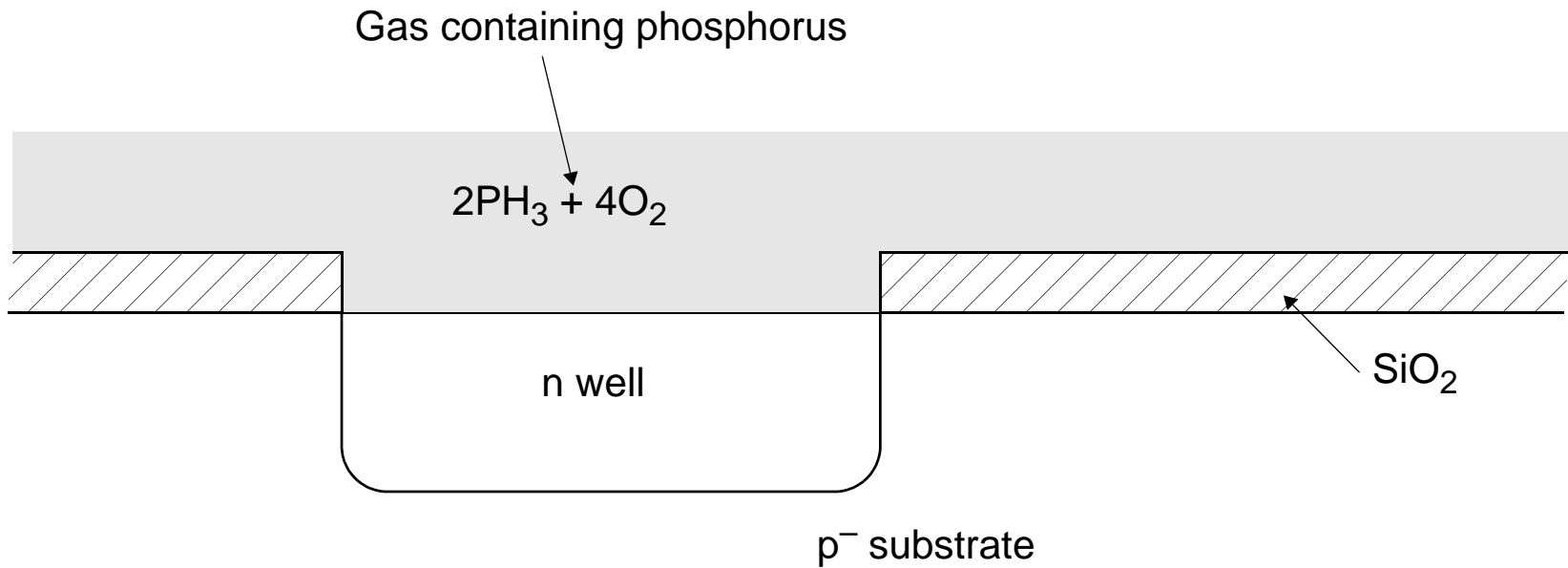


Photolithography

Ultraviolet light



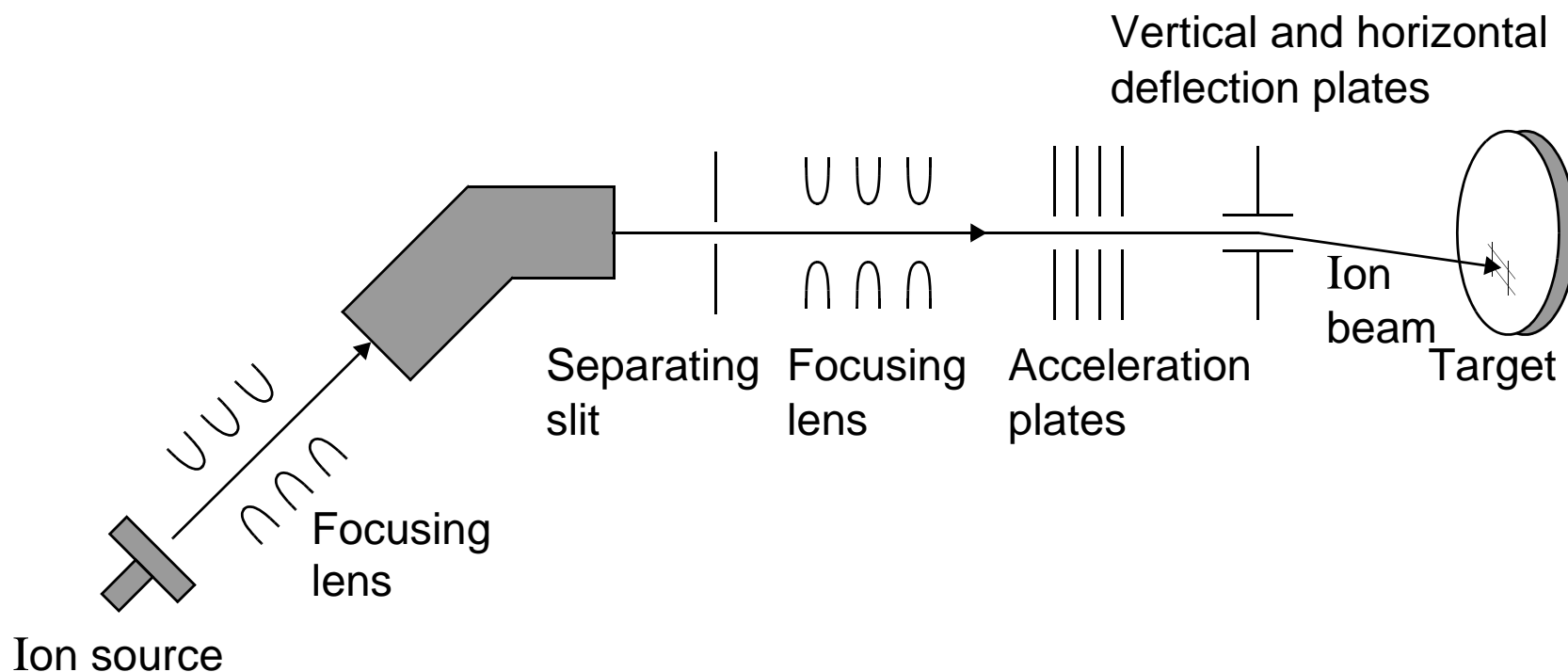
Diffusion



- Introduce dopants where well will be located
- Phosphorus gas used in furnace (1000 °C)



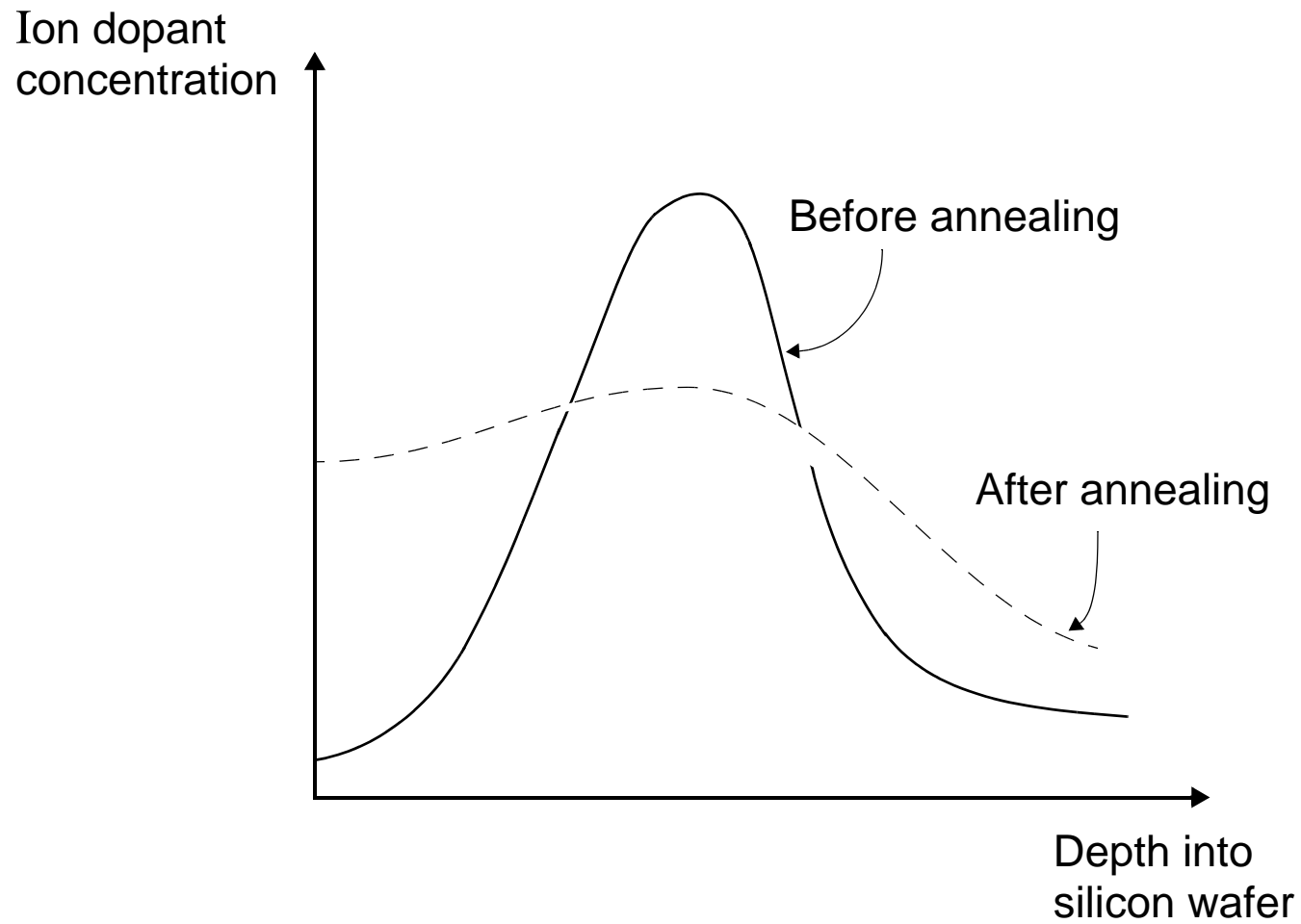
Ion Implantation



- More control as can set concentration and thickness
- Acceleration sets depth, current and time set dosage
- However, lattice damage and narrow doping profile — requires annealing



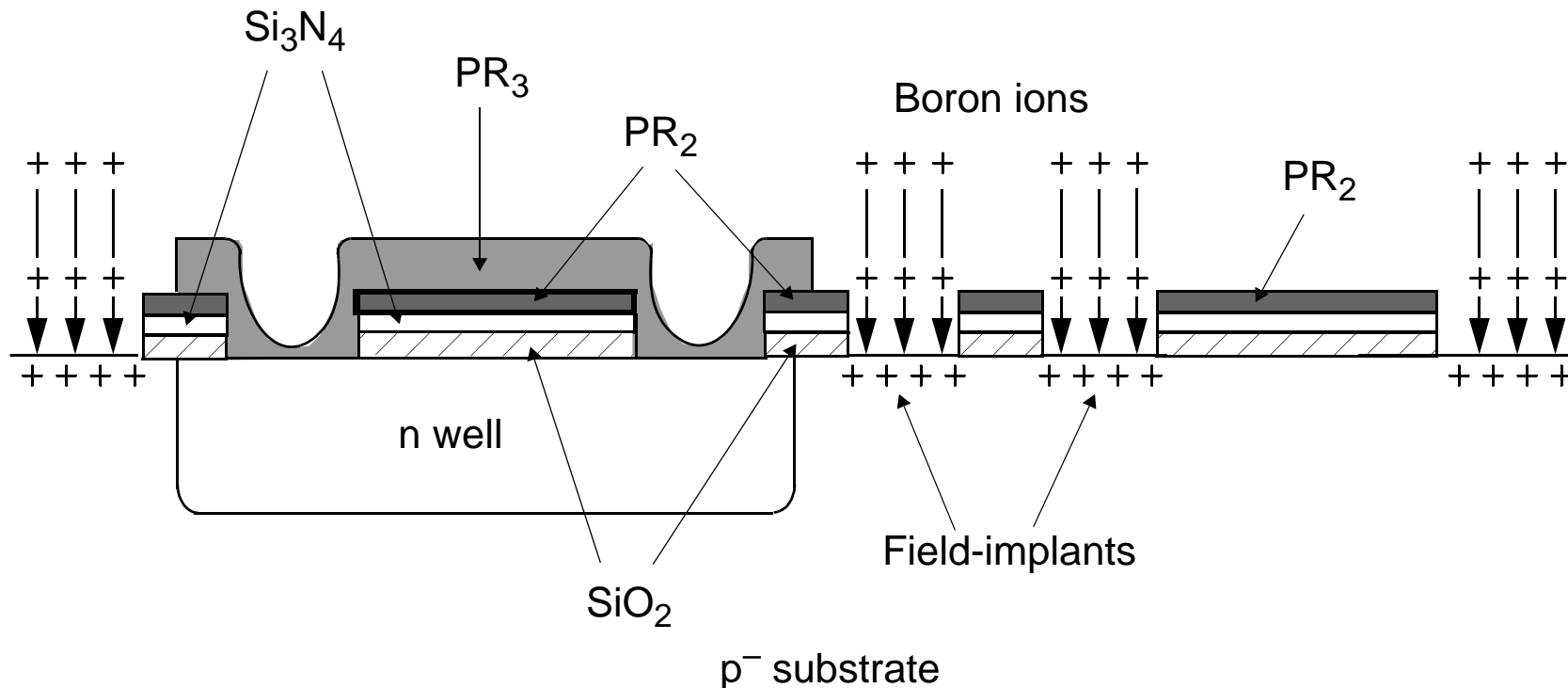
Annealing



- Heat to 1000 °C then cool slowly



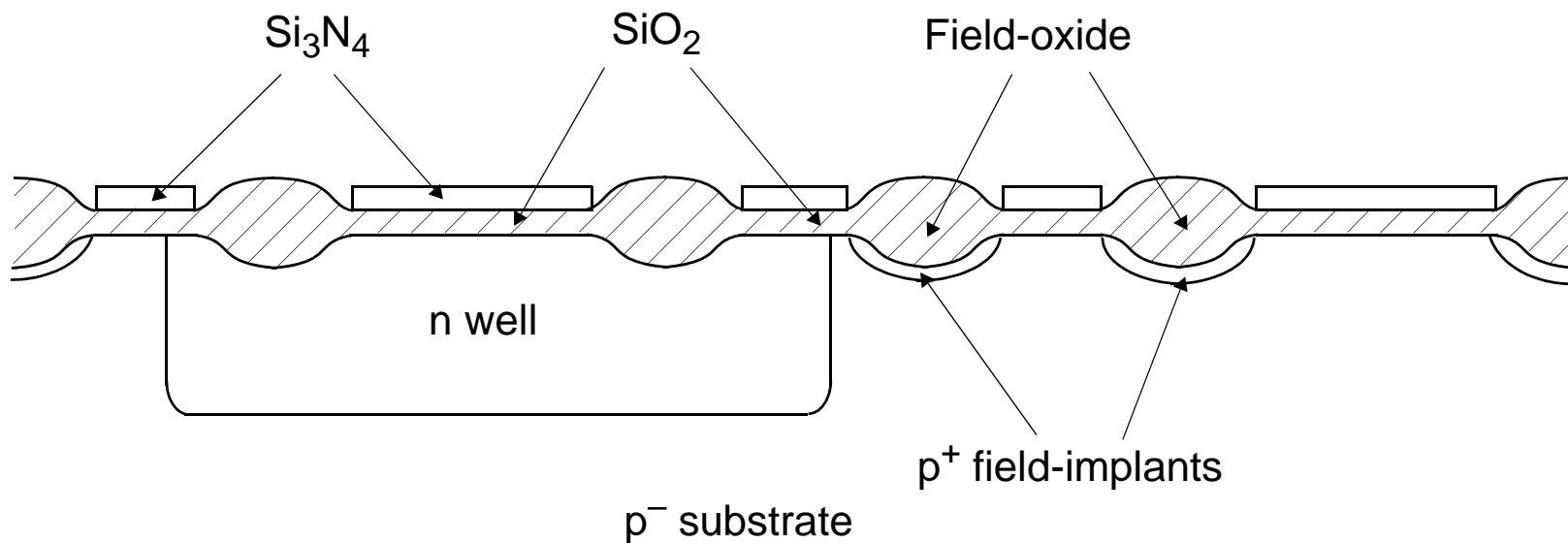
Field-implants



- Ensures silicon under field-oxide will not invert (will remain p^-) although conductors above



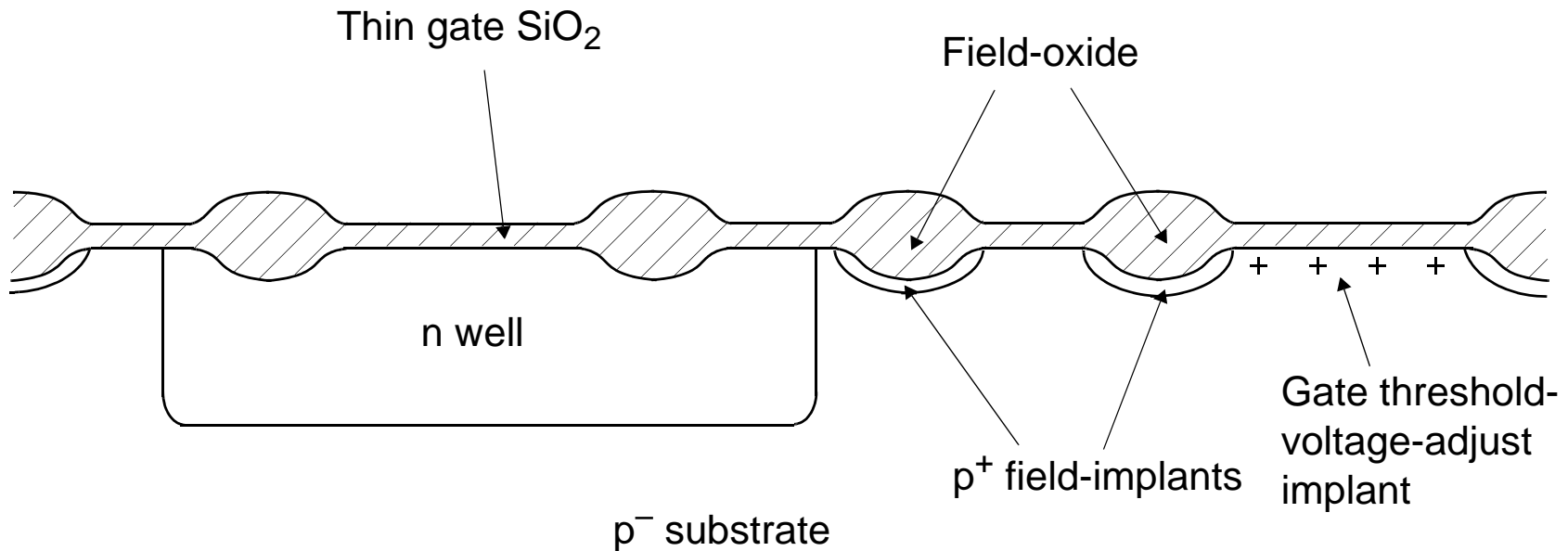
Field-oxide



- Thick SiO_2 where no transistors
- Wet process (H_2O) — fast but more defects
- Dry process (O_2) — slower but denser and higher quality (high temp so called ***thermal oxide***)



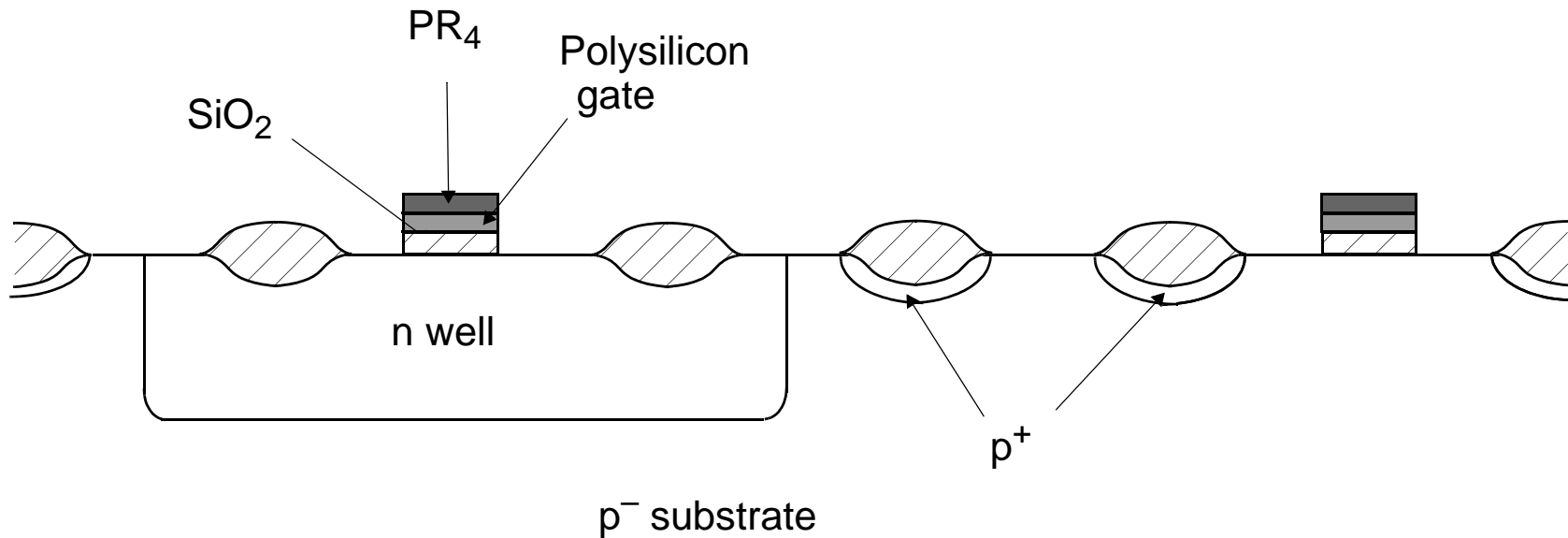
Thin gate-oxide and threshold-adjust



- Thin oxide grown using dry process ($0.01 \mu\text{m}$)
- If n -well more heavily doped then single boron implant will adjust V_{tn} from -0.1V to 0.8V and V_{tp} from -1.6V to -0.8V



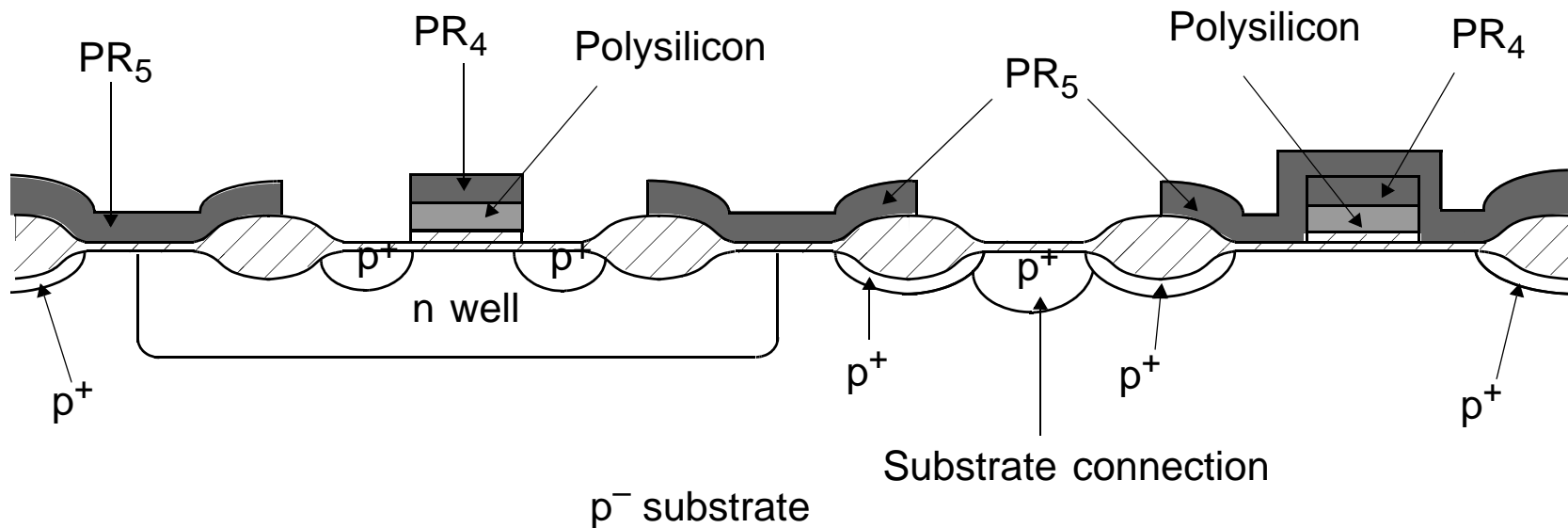
Polysilicon Gates



- Apply gate but only heat to $650\text{ }^\circ\text{C}$ — polysilicon (rather than single crystal)
- 10 to $30\ \Omega/\square$ and thickness of $0.25\ \mu\text{m}$



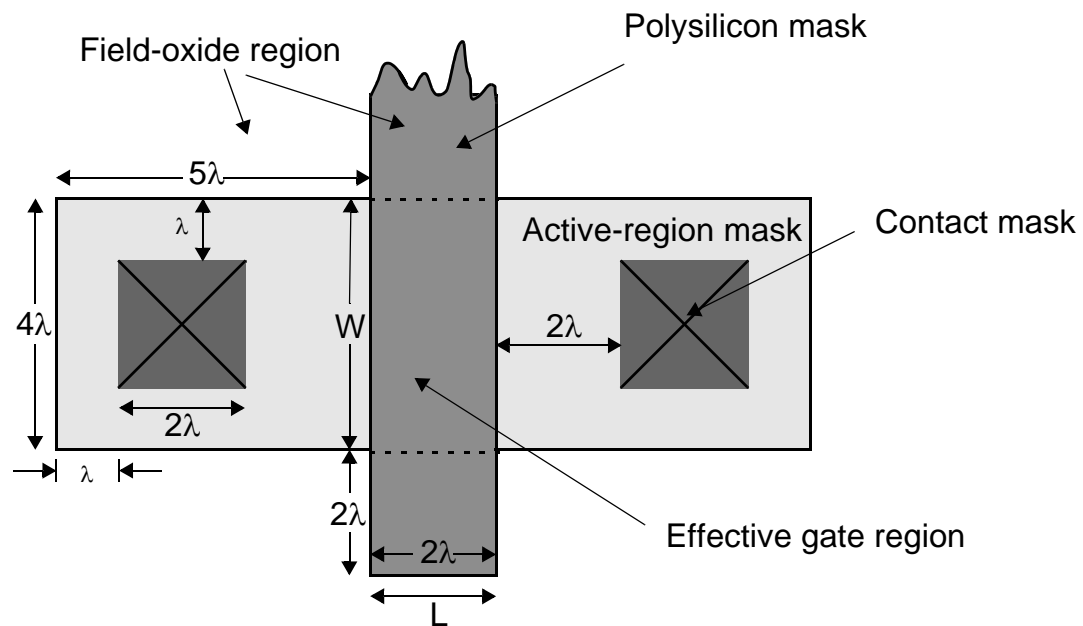
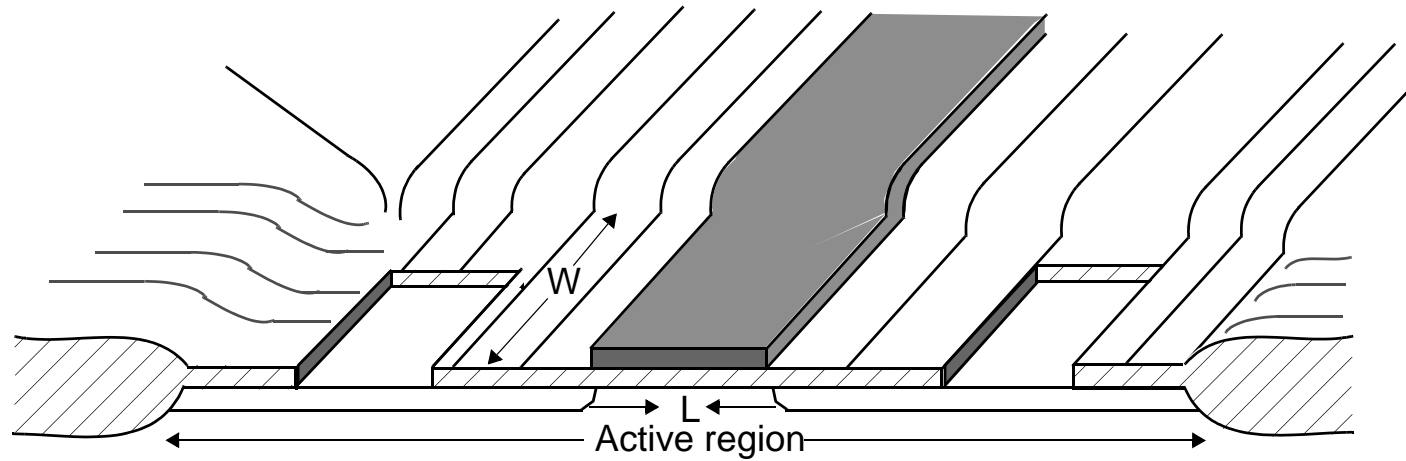
P+ Junctions



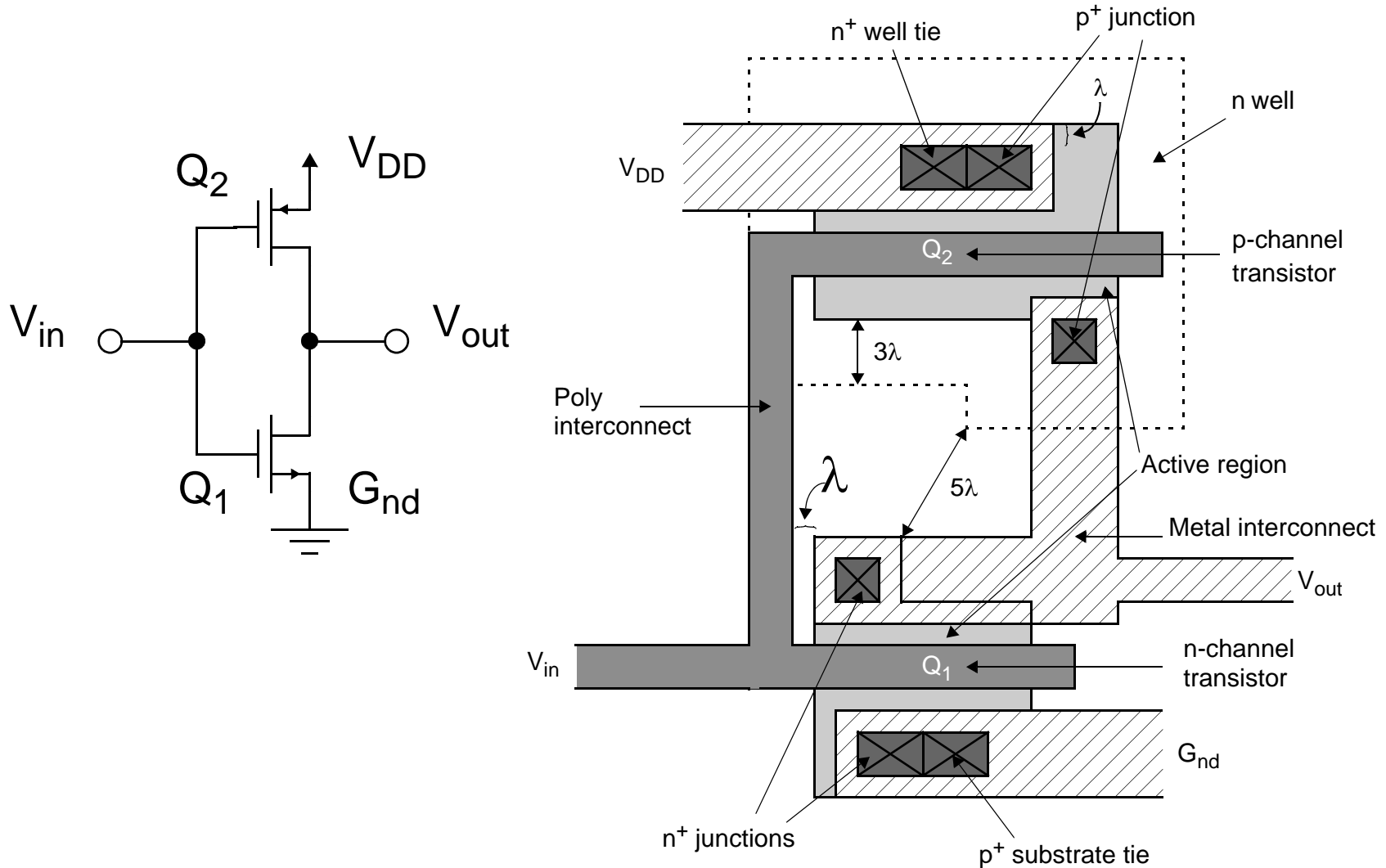
- Gates and drains formed for p-channel
- Use ion implantation
- Self-aligned as gate determines edges
- Substrate connection also shown



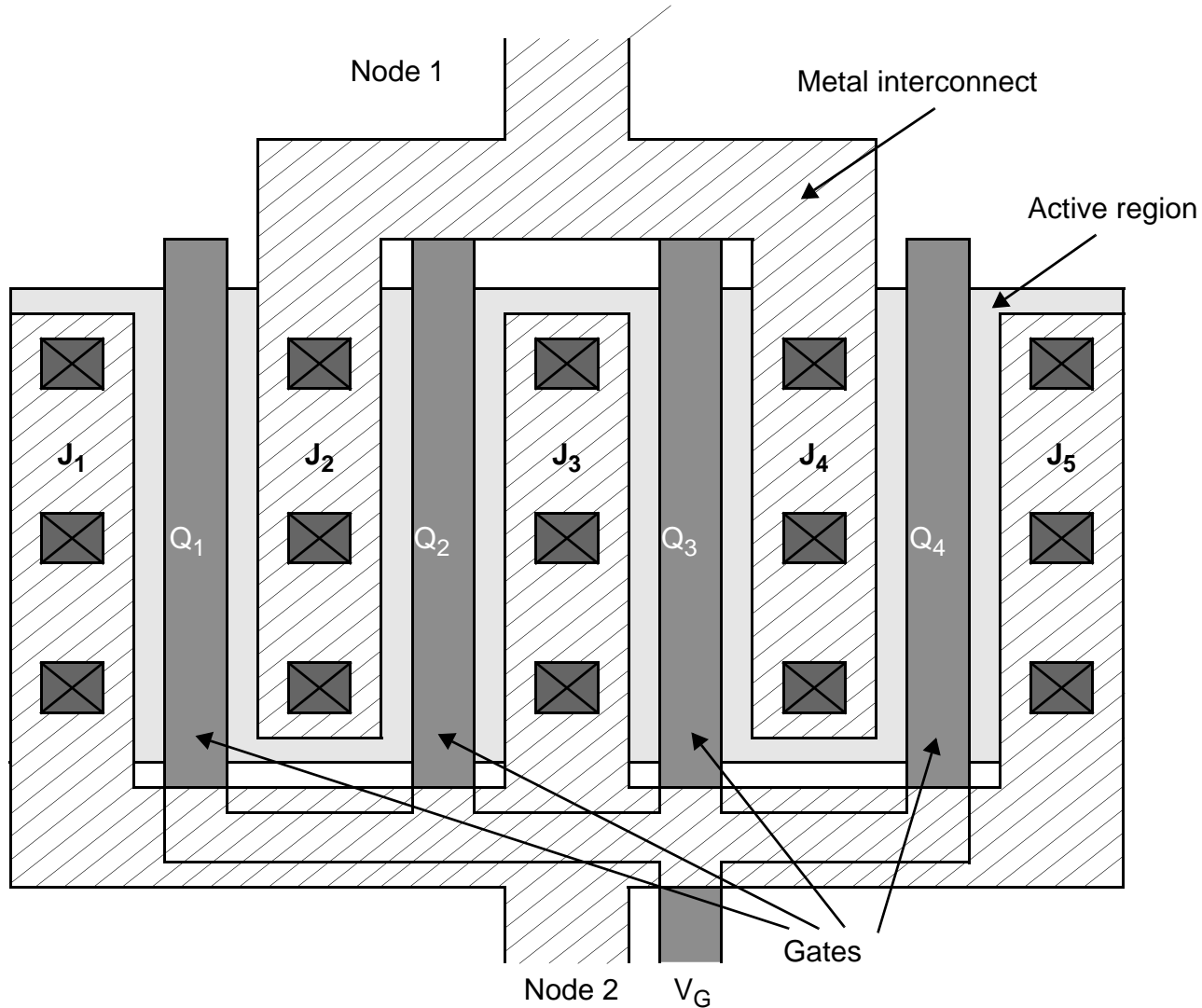
Transistor Layout



CMOS Inverter



Single Large Transistor (4 in parallel)



Schematic of Large Transistor

