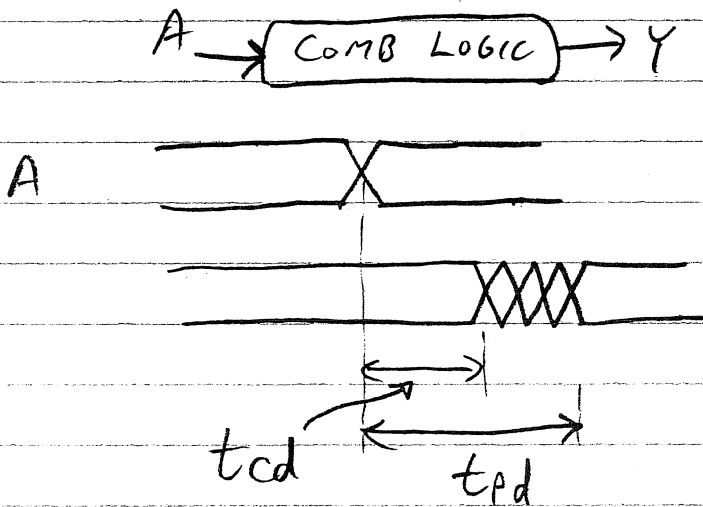


SIMILAR FOR COMBINATIONAL LOGIC



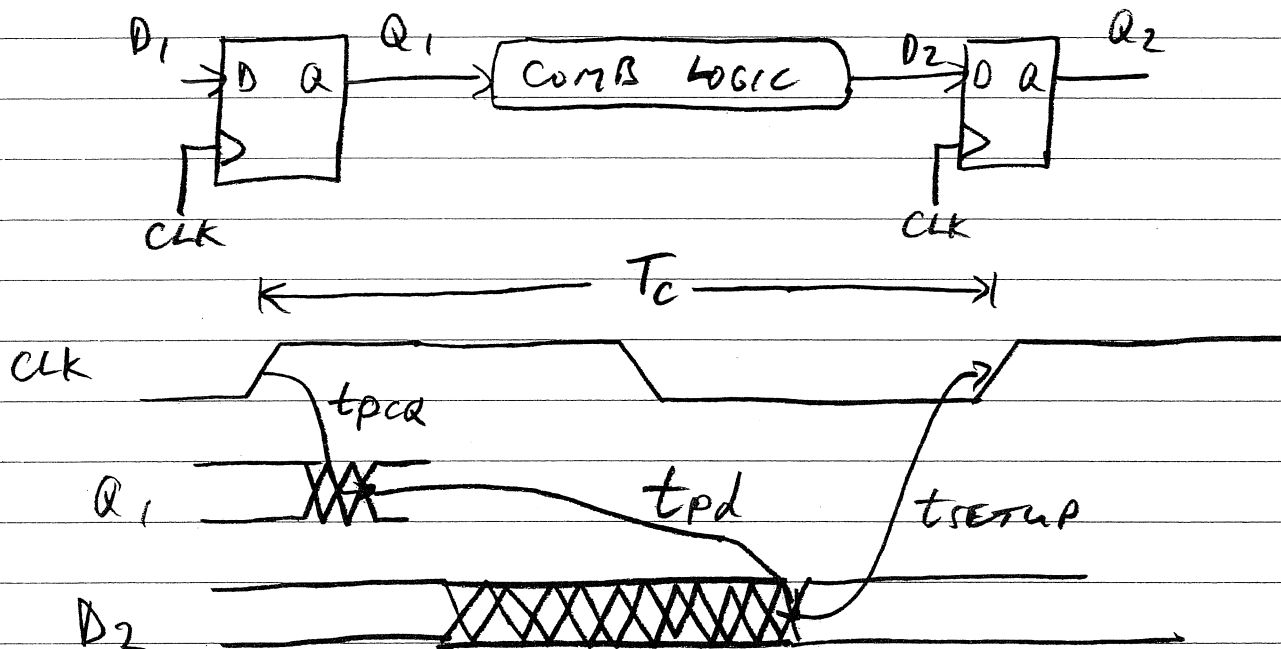
t_{cd} COMB LOGIC CONTAMINATION DELAY

t_{pd} COMB LOGIC PROPAGATION DELAY

MAX DELAY CONSTRAINT

(S-3)

MAX CLOCK FREQ OF SYNCHRONOUS SYSTEM DETERMINED BY t_{setup} , t_{pcq} , t_{pd}



$$T_c \geq t_{\text{pcq}} + t_{\text{pd}} + t_{\text{setup}}$$


OR

$$t_{\text{pd}} \leq T_c - \overbrace{(t_{\text{setup}} + t_{\text{pcq}})}^{\text{REGISTER OVERHEAD}}$$

IF NOT SATISFIED, KNOWN AS "SETUP TIME FAILURE" OR "MAX-DELAY FAILURE"

MIN-DELAY CONSTRAINT

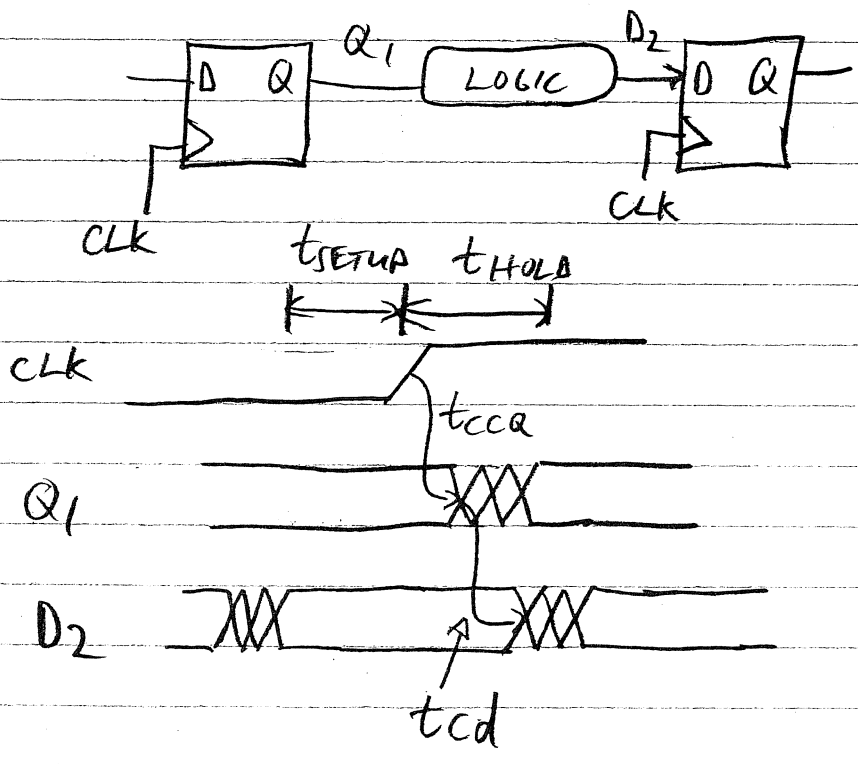
IF "D" NOT HELD LONG ENOUGH

AFTER  THEN DATA MAY PROPAGATE

THROUGH 2 REGISTERS ON ONE CLOCK

EDGE.

KNOWN AS RACE CONDITION
HOLD-TIME FAILURE
MIN-DELAY FAILURE



$$t_{HOLD} \leq t_{CCQ} + t_{CD}$$

EXAMPLE

S-6

GIVEN REGISTERS WITH

$$t_{\text{setup}} = 150 \text{ ps}$$

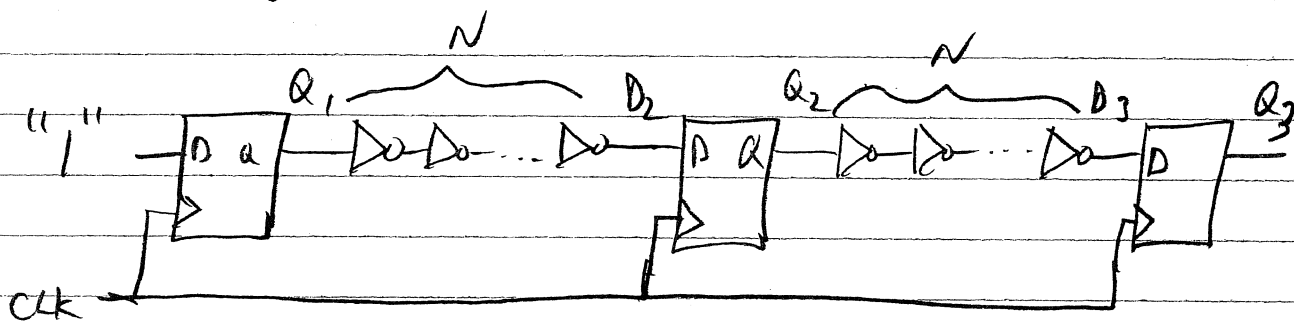
$$t_{\text{hold}} = 120 \text{ ps}$$

$$t_{\text{ccq}} = 60 \text{ ps}$$

$$t_{\text{pcq}} = 180 \text{ ps}$$

AND INVERTERS WITH $t_{\text{di}} = 30 \text{ ps}$

AND FOLLOWING CIRCUIT WITH INITIAL STATES ALL "0"



a) IF $N=15$, WHAT IS MAX CLOCK RATE?

b) FOR A 26GHz CLOCK, WHAT IS MAX N ?

c) SHOW Q_1, Q_2, Q_3 IF $N=15$

WHEN $f_{\text{clk}} = 500 \text{ MHz}$ AND WHEN $f_{\text{clk}} = 26 \text{ GHz}$

d) SHOW Q_1, Q_2, Q_3 IF $N=0$ AND
 $f_{\text{clk}} = 100 \text{ MHz}$

5-7

e) FIND MIN N SO NO RACE CONDITION OCCURS.

SOLN

$$\begin{aligned} a) \quad T_C &\geq t_{pcq} + N t_{dI} + t_{setup} \\ &\geq 180 + (15)(30) + 150 \\ &\geq 780 \text{ ps} \end{aligned}$$

$$f_{clk} = \frac{1}{T_C} \leq \frac{1}{780 \text{ ps}} = \underline{\underline{1.28 \text{ GHz}}}$$

$$b) \quad T_C = \frac{1}{26 \text{ GHz}} = 500 \text{ ps} \geq t_{pcq} + N t_{dI} + t_{setup}$$

$$500 \geq 180 + N(30) + 150$$

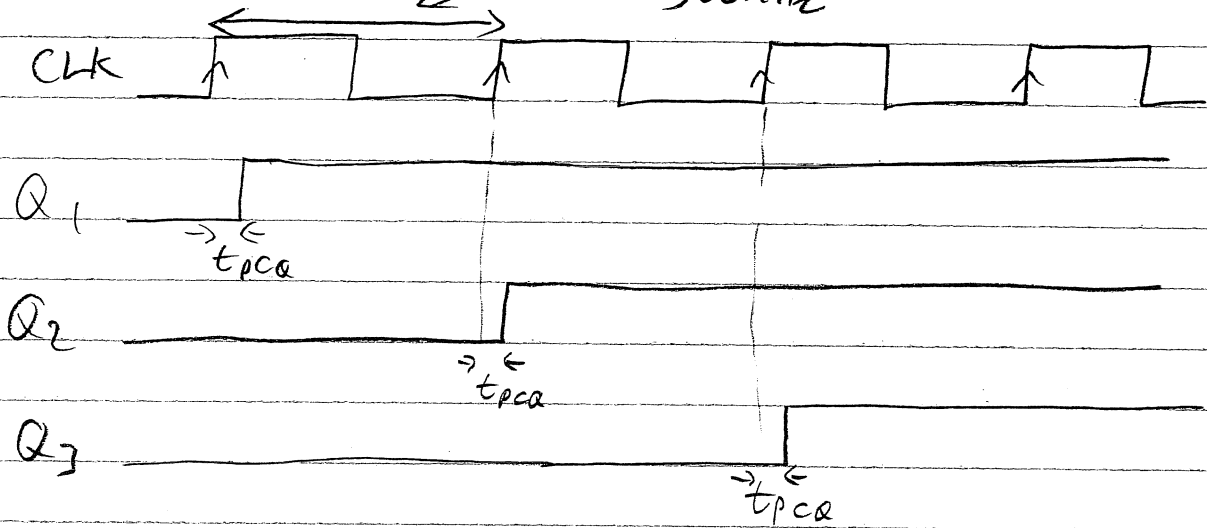
$$N(30) \leq 170 \text{ ps}$$

$$N \leq 5.6 \quad \text{MAX } N = \underline{\underline{5}}$$

5-8

c) $f_{CLK} = 500 \text{ MHz}$ (OPERATES CORRECTLY)

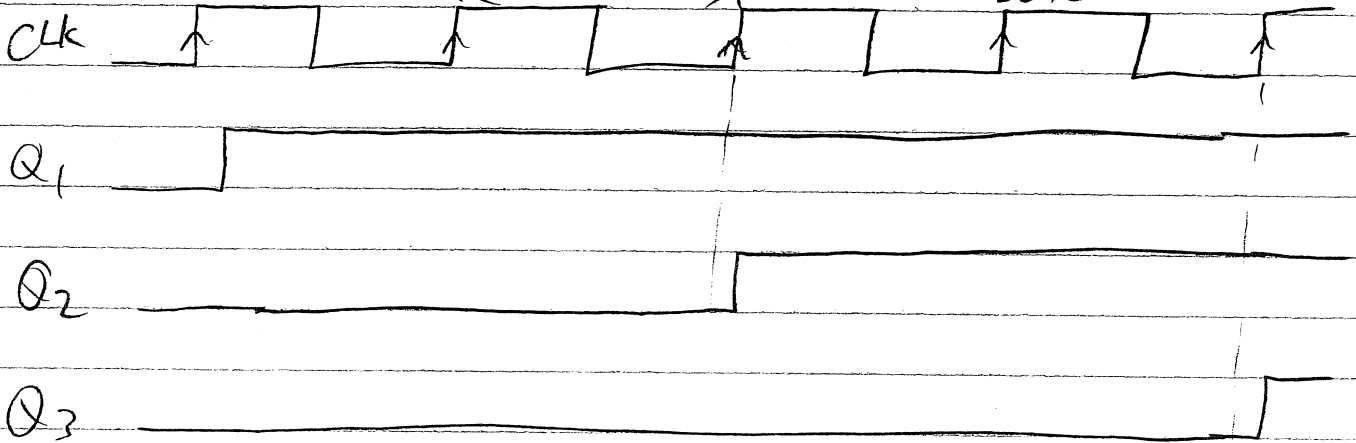
$N = 15$ $T_C = \frac{1}{500 \text{ MHz}}$



$f_{CLK} = 26 \text{ GHz}$ (SETUP TIME VIOLATION)

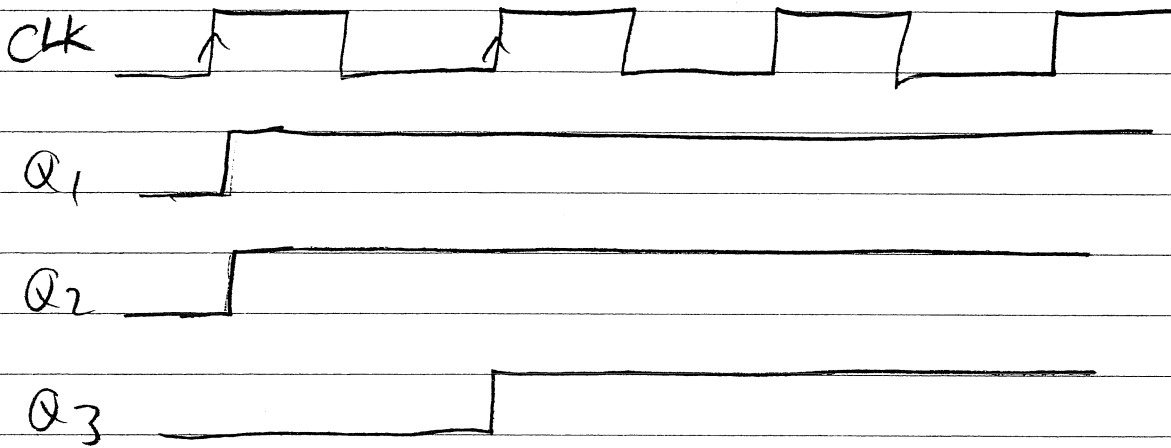
$N = 15$

$T_C = \frac{1}{26 \text{ GHz}}$



ERROR

d) IF $N=0$ (HOLD TIME VIOLATION)



RACE CONDITION ERROR

e) TO NOT VIOLATE HOLD TIME

$$t_{\text{HOLD}} \leq t_{\text{CCQ}} + N t_{\text{DE}}$$

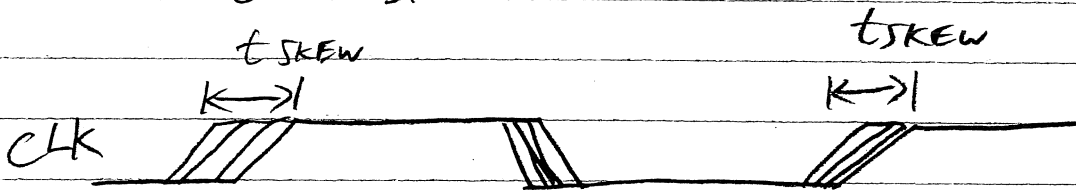
$$120 \leq 60 + N(30)$$

$$N \geq 2 \quad \text{MIN } N = 2$$

DOES NOT DEPEND ON CLOCK RATE
 HOWEVER t_{HOLD} OFTEN A FUNCTION OF
 CLOCK RISE/FALL TIMES \Rightarrow KEEP FAST
 CLOCK EDGES!

CLOCK SKEW

S-10



FOR MAX DELAY WORST IS IF
LAUNCHING REGISTER RECEIVES LATE CLOCK
WHILE RECEIVING REGISTER IS CLOCKED EARLY

$$t_{pd} \leq T_C - (t_{pcq} + t_{setup} + t_{skew})$$

FOR MIN DELAY WORST CASE IS
IF LAUNCHING REGISTER RECEIVES EARLY
CLOCK AND RECEIVING REGISTER IS
CLOCKED LATE

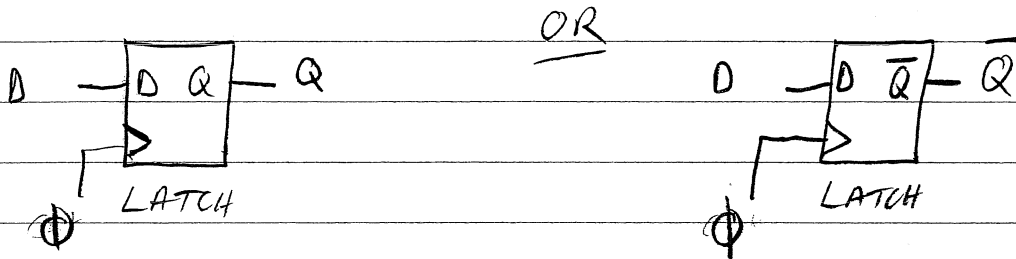
$$t_{cd} \geq t_{hold} - t_{ccq} + t_{skew}$$

LATCH / REGISTER CIRCUITS

S-11

LATCHES

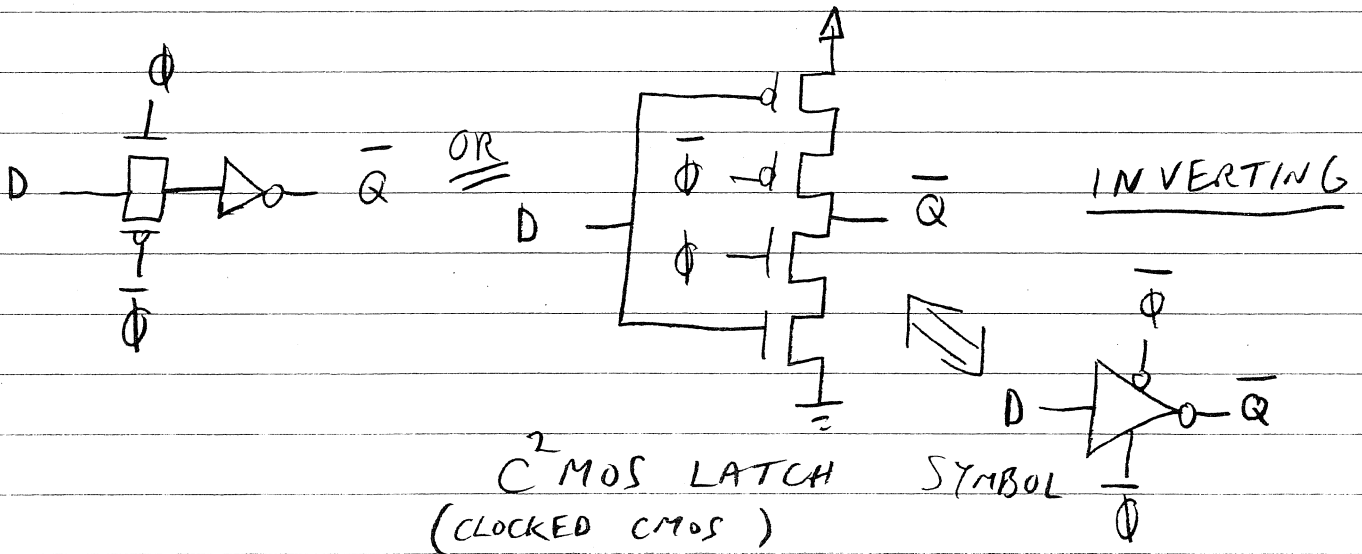
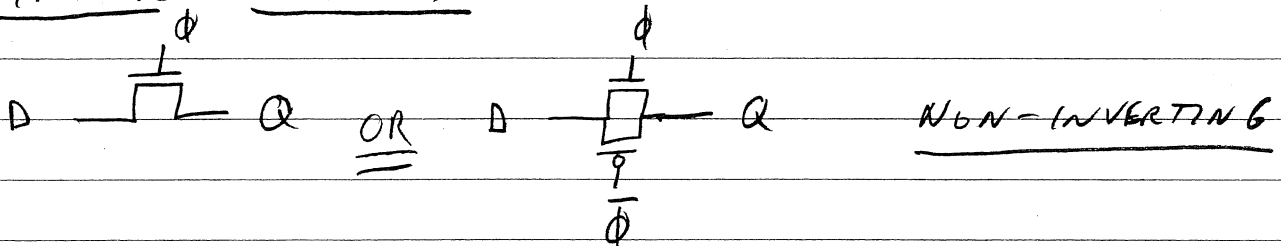
RECALL



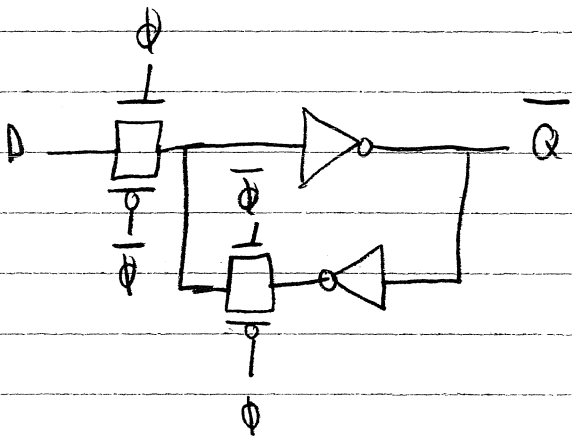
$\phi = 1 \quad Q = D$
 $\phi = 0 \quad Q \text{ HELD}$

$\phi = 1 \quad \bar{Q} = \bar{D}$
 $\phi = 0 \quad \bar{Q} \text{ HELD}$

DYNAMIC LATCHES

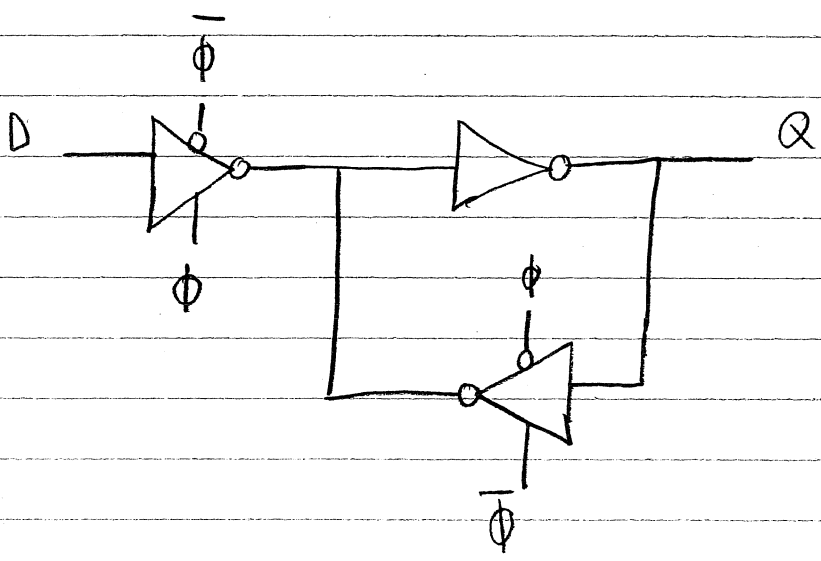


STATIC LATCHES



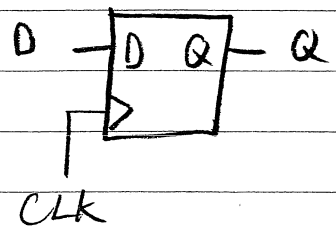
T-GATE LATCH

OR

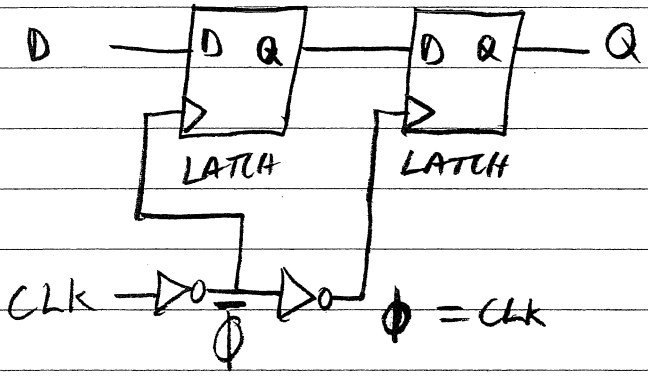


2CMOS STATIC LATCH

REGISTERS

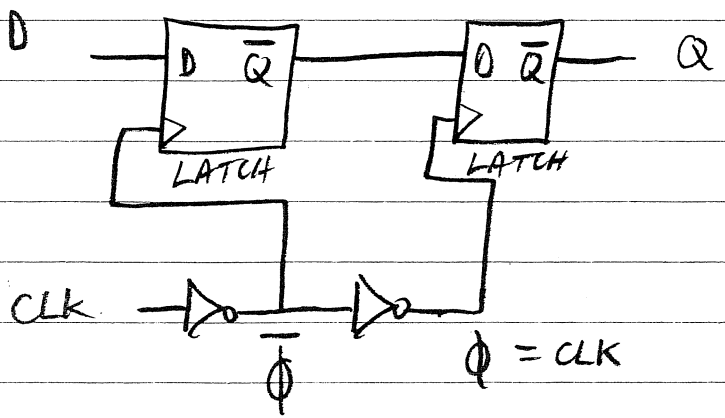


CLK \uparrow $Q = D$
CLK = 0 Q HELD
CLK = 1 Q HELD
CLK $\Rightarrow \downarrow$ Q HELD



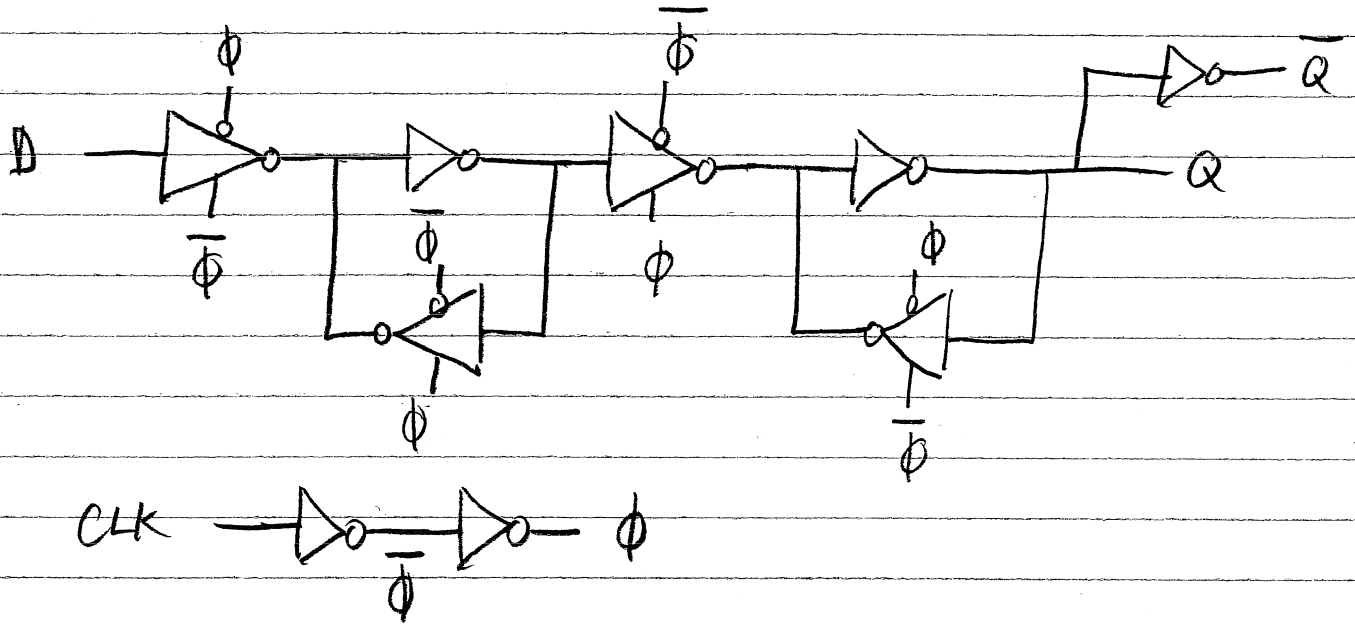
NON-INVERTING LATCHES

OR



INVERTING LATCHES

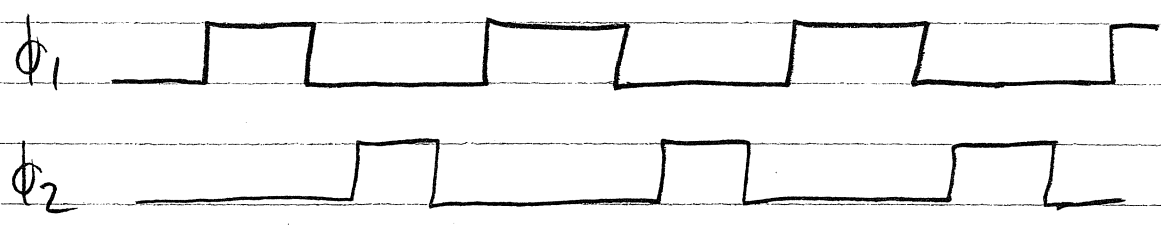
EX REGISTER USING C²MOS STATIC LATCHES



IF CONCERNS ABOUT RACE CONDITIONS

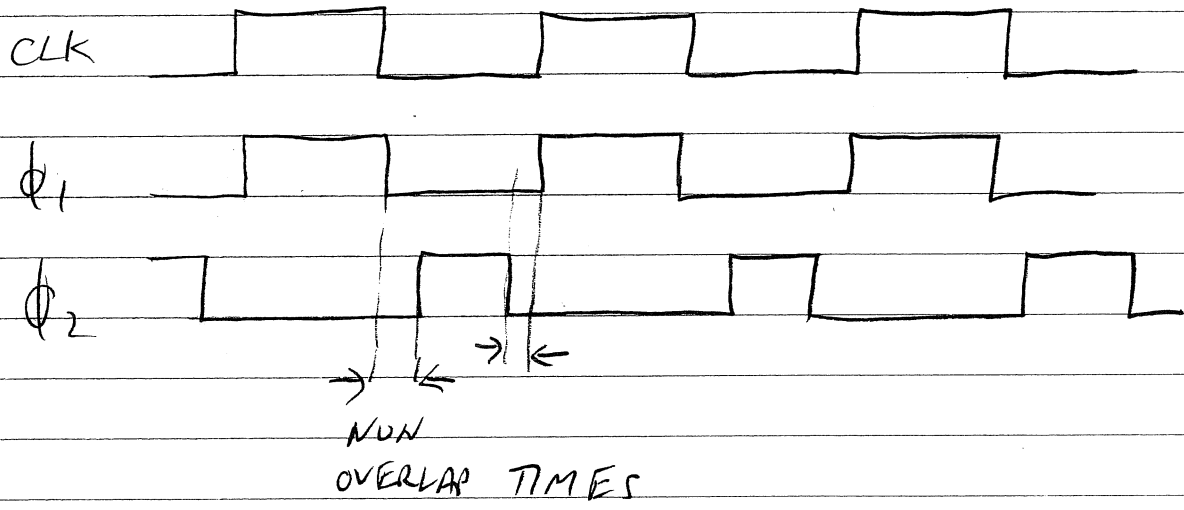
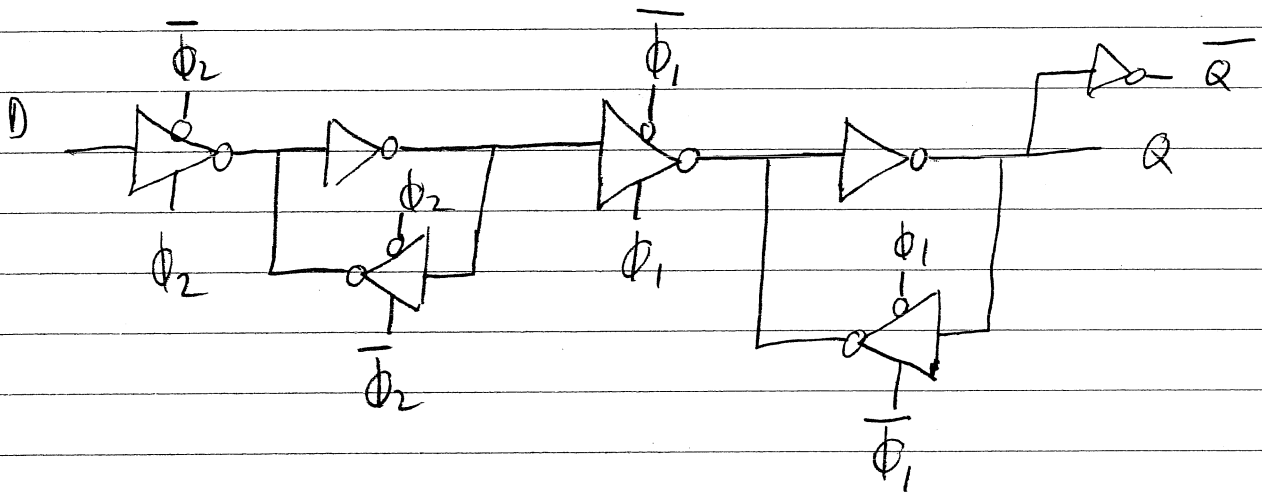
CAN USE NON-OVERLAPPING CLOCKS

ϕ_1, ϕ_2 (AND $\bar{\phi}_1, \bar{\phi}_2$)

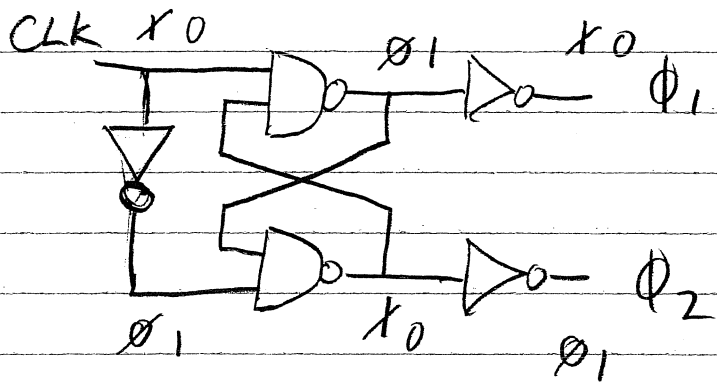


REGISTER WITH NON-OVERLAPPING CLOCKS

S-15



NON-OVERLAPPING CLOCK GENERATOR



RESETTABLE REGISTERS

- NORMALLY USE CLOCKED "RESETS"
OR "SETS" SO NO ASYNCHRONOUS
PROBLEMS TO DEAL WITH

