**LATCH/REGISTER CIRCUITS**

**LATCHES**

RECALL

\[ D \rightarrow Q \rightarrow \overline{Q} \]  \[ D \rightarrow \overline{Q} \rightarrow Q \]

\[ \phi = 1 \quad Q = D \quad \phi = 1 \quad \overline{Q} = D \]
\[ \phi = 0 \quad Q = \text{HOLD} \quad \phi = 0 \quad \overline{Q} = \text{HOLD} \]

**DYNAMIC LATCHES**

\[ D \rightarrow \overline{Q} \rightarrow Q \quad \text{NON-INVERTING} \]

\[ D \rightarrow \overline{Q} \rightarrow Q \quad \text{INVERTING} \]

**CMOS LATCH SYMBOL**

(CLOCKED CMOS)
STATIC LATCHES

T-GATE LATCH

CMOS STATIC LATCH
REGISTERS

\[ D \rightarrow \overline{D} \rightarrow Q \frac{\text{CLK}}{\uparrow} \rightarrow \overline{Q} = 0 \]

\[ \text{CLK} = 0 \quad Q \text{ held} \]

\[ \text{CLK} = 1 \quad Q \text{ held} \]

\[ \text{CLK} \Rightarrow \overline{Q} \quad Q \text{ held} \]

\[ \text{Non-Inverting Latches} \]

\[ \text{Inverting Latches} \]
REGISTER USING CMOS STATIC LATCHES

CLK

IF CONCERNS ABOUT RACE CONDITIONS
CAN USE NON-OVERLAPPING CLOCKS

\[ \phi_1, \phi_2 \quad \text{(AND } \overline{\phi_1}, \overline{\phi_2}) \]
REGISTER
WITH NON-OVERLAPPING CLOCKS

D

\[ \Phi_2 \]

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ \Phi_1 \]

CLK

\[ \Phi_1 \]

\[ \Phi_2 \]

NON-OVERLAP TIMES
NON-OVERLAPPING CLOCK GENERATOR

RESETTABLE REGISTERS

- Normally use clocked "resets"
- Or "sets" so no asynchronous problems to deal with