University of Toronto

Final Exam

Date - Apr 28, 2009

Duration: 2.5 hrs

ECE334 — Digital Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Assume the parameters on the parameter sheet (last page) unless otherwise stated (mosfets are from a 0.25um CMOS technology)
2. Single handwritten aid sheet allowed.
3. Only tests written in pen will be considered for a re-mark.
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
6	
7	
Total	

(max grade = 41)

Last Name: ______________________

First Name: ______________________

Student #: ______________________

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

T F Trench capacitors in DRAM memory arrays are implemented differentially to reduce noise effects.

T F In clock distribution using both grid and H-trees, a grid is used for global clocking while H-trees are used for local clock distribution.

T F Bond wires used in IC packaging connect the bond pad to the lead frame of the package.

T F Although through-hole pin packages result in less PCB density than SMT packages, through-hole pin packages are good for high speed due to less inductance.

T F Phase-locked-loops are commonly used to build clock multipliers through the use of a clock divider in the feedback portion of the PLL.

T F NOR flash memory is generally more dense than NAND flash memory.

T F DRAM memory is normally built in standard CMOS technology.

T F SRAM memory is normally built in standard CMOS technology.

T F When the clock is routed in the same direction as data signals in sequential logic, race conditions are more likely than when the clock is routed in the opposite direction.

T F The purpose of using $V_{DD}/2$ for the trench capacitors back bias is to reduce voltage stress on the trench capacitors.

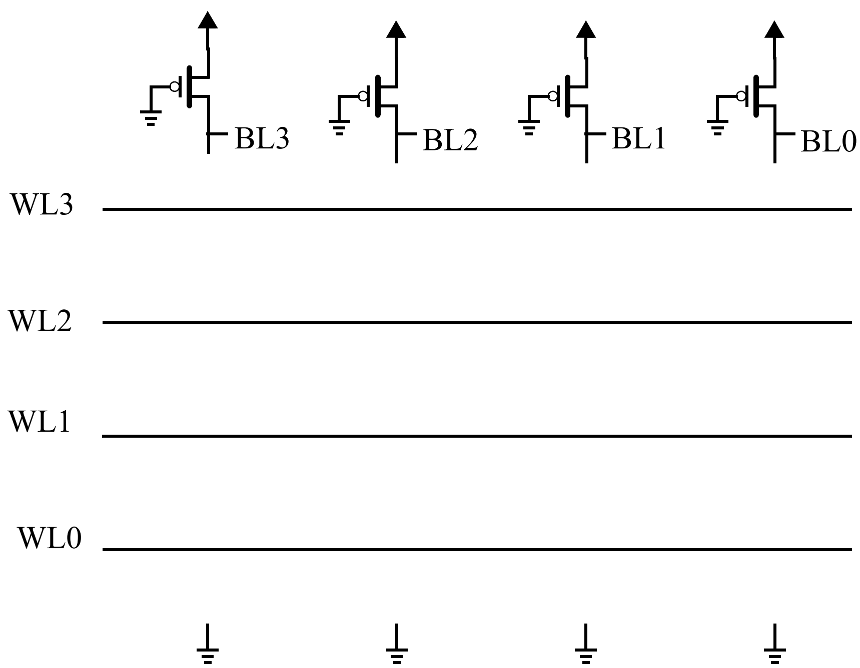
[6] Question 2: Implement the equation $X = (\bar{A} \bullet \bar{B}) + \bar{C}$ using CMOS logic assuming that A, B, C are all available as inputs. Assume that the transistors have been sized to give an output resistance of 10k for the worst-case input pattern (in both the high output and low output cases). Find the input pattern, ABC, that gives the lowest output resistance when the output is LOW. Also find the value of that resistance, R_{out} when the output is LOW.

ABC =

R_{out} =

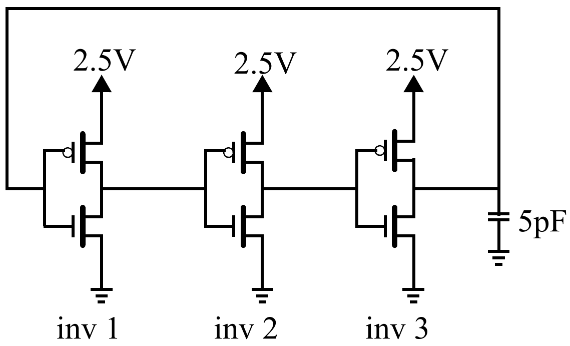
[6] Question 3: a) Add the NMOS transistors in the shown 4x4 MOS NAND ROM to store the following data:

BL3	BL2	BL1	BL0
0	1	0	0
1	0	1	0
0	0	0	0
1	1	1	0



b) What is the main advantage of a MOS NAND ROM over a MOS NOR ROM and why does it occur?

[6] Question 4: Find the propogation delay of each inverter (t_{p1}, t_{p2}, t_{p3}) in the ring oscillator below (only account for gate capacitance (WLC_{ox}) and the shown 5pF capacitance. Also find the oscillation frequency, f_{osc}. Assume n-channel transistors are sized 0.5um/0.25um while p-channel transistors are sized 1.5um/0.25um. (use transistor values on last page)



t_{p1} =

t_{p2} =

t_{p3} =

f_{osc} =

[6] Question 5:

a) Explain the mechanism of Fowler-Nordheim tunneling.

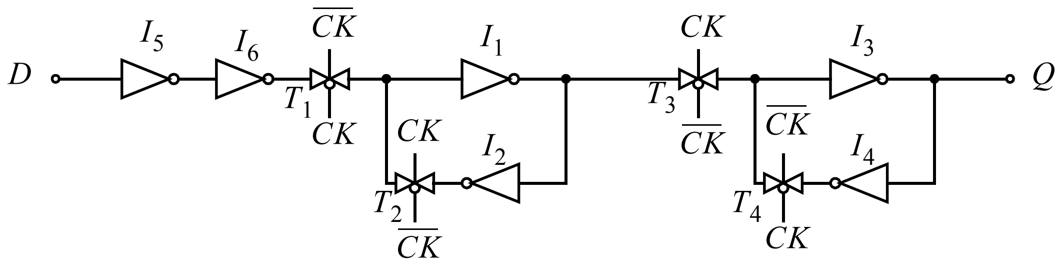
b) Explain the mechanism of hot carrier injection.

c) Which mechanism causes more damage to the oxide and therefore limits the number of programs/erase cycles of non-volatile memories?

d) What mechanism is used to erase EPROM memory? (not EEPROM or Flash but only EPROM).

Last Name: ________________

[6] Question 6: Consider the "d" register shown below.



Assuming that CK and $\overline{CK}$ occur at the same time, and defining the following delays:

T_{I_i} is the delay through the i 'th inverter

T_{G_i} is the delay through the i 'thT-gate from its clock input to its output

T_{T_i} is the delay through the i 'thT-gate from its "data" input to its output

a) Find T_{setup} in terms of T_{I_i}, T_{G_i} and T_{T_i} (be specific in terms of i).

T_{setup} =

b) Find T_{pcq} in terms of T_{I_i}, T_{G_i} and T_{T_i} (be specific in terms of i).

T_{pcq} =

[6] Question 7: It is required to transfer a 16 bit bus across 2 asynchronous clock domains. Show how this is achieved using a 2 phase handshake. (Draw block diagrams, clock timing diagrams and words to make it clear).

(blank sheet for scratch calculations)

ECE334F Digital Electronics Parameter Sheet

Physical Constants;

$\phi_T = kT/q = 26$mV (at 300K); $k = 1.38 \times 10^{-23}$ J/K; $T = 300$ K (at $27°C$); $q = 1.6 \times 10^{-19}$ C;

$\varepsilon_o = 8.854 \times 10^{-12} F/\text{m}$; $k_{ox} = 3.9$; $\phi_s = 2|\phi_F| = 0.6V$

MOS Transistor; CMOS basic parameters. Channel length = $0.25\mu m$, $m_j = 0.5$, $\phi_o = 0.9$V

	V_{T0} (V)	γ $(V^{0.5})$	μC_{ox} $(\mu A/V^2)$	λ (V^{-1})	C_{ox} $(fF/\mu m^2)$	C_o $(fF/\mu m)$	C_j $(fF/\mu m^2)$	C_{jsw} $(fF/\mu m)$
NMOS	0.4	0.4	120	0.06	6	0.3	2	(see below)
PMOS	-0.4	0.4	30	0.1	6	0.3	2	(see below)

V_{T0} is the threshold voltage with zero bulk-source voltage.

γ is used to account for non-zero bulk-source voltage.

μC_{ox} is the transistor current gain parameter.

λ is to account for the transistor finite output impedance (channel length modulation).

C_{ox} is the gate capacitance per unit area.

C_o is the gate overlap capacitance per unit length.

C_j is the drain/source junction capacitance per unit area.

C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters **except under the gate**.

$C_{jsw} = 0.3\ fF/\mu m$ for both NMOS and PMOS

C_{jswg} is the drain/sourc junction capacitance per unit length under the gate.

$C_{jswg} = 0.15\ fF/\mu m$ for both NMOS and PMOS