

- 1.4 Sketch a transistor-level schematic for a single-stage CMOS logic gate for each of the following functions:
- a) $Y = \overline{ABC + D}$
 - b) $Y = \overline{(AB + C) \cdot D}$
 - c) $Y = \overline{AB + C \cdot (A + B)}$
- 1.6 Sketch a transistor-level schematic of a CMOS 3-input XOR gate. You may assume you have both true and complementary versions of the inputs available.
- 1.7 Sketch transistor-level schematics for the following logic functions. You may assume you have both true and complementary versions of the inputs available.
- a) A 2:4 decoder defined by
$$Y0 = \overline{A0} \cdot \overline{A1}$$
$$Y1 = \overline{A0} \cdot A1$$
$$Y2 = A0 \cdot \overline{A1}$$
$$Y3 = A0 \cdot A1$$
 - b) A 3:2 priority encoder defined by
$$Y0 = \overline{A0} \cdot (A1 + \overline{A2})$$
$$Y1 = \overline{A0} \cdot A1$$
- 1.8 Sketch a stick diagram for a CMOS 4-input NOR gate from Exercise 1.3.
- 1.11 Figure 1.72 shows a stick diagram of a 2-input NAND gate. Sketch a side view (cross-section) of the gate from X to X'.
- 1.13 Draw a transistor-level schematic for the latch of Figure 1.73. How does the schematic differ from Figure 1.30(b)?
- 1.14 Consider the design of a CMOS compound OR-AND-INVERT (OAI21) gate computing $F = \overline{(A + B) \cdot C}$.
- a) sketch a transistor-level schematic
 - b) sketch a stick diagram
- 1.16 A 3-input majority gate returns a true output if at least two of the inputs are true. A minority gate is its complement. Design a 3-input CMOS minority gate using a single stage of logic.
- a) sketch a transistor-level schematic
- 1.17 Design a 3-input minority gate using CMOS NANDs, NORs, and inverters. How many transistors are required? How does this compare to a design from Exercise 1.16(a)?