

2.21 Give an expression for the output voltage for the pass transistor networks shown in Figure 2.40. Neglect the body effect.

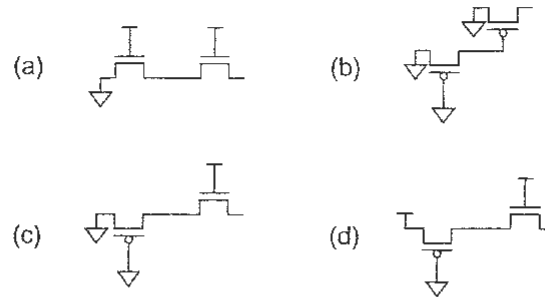


FIG 2.40 Pass transistor networks

2.22 Suppose $V_{DD} = 1.2\text{ V}$ and $V_t = 0.4\text{ V}$. Determine V_{out} in Figure 2.41 for: (a) $V_{in} = 0\text{ V}$; (b) $V_{in} = 0.6\text{ V}$; (c) $V_{in} = 0.9\text{ V}$; and (d) $V_{in} = 1.2\text{ V}$. Neglect the body effect.

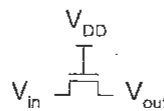
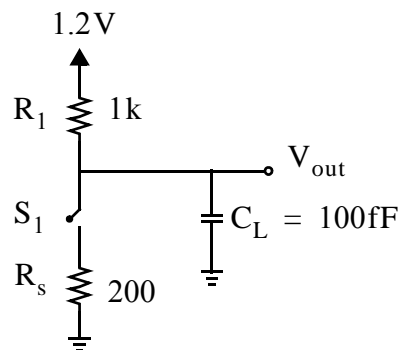


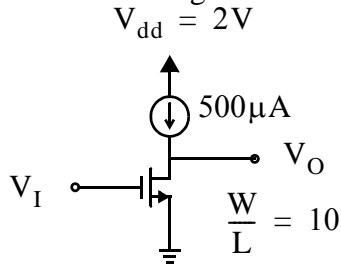
FIG 2.41 Single pass transistor

1) Consider the following resistor transistor logic (RTL) inverter where switch S_1 represents the transistor and R_s represents the switch on resistance (it's off resistance is infinite).



- a) Sketch the output waveform for the switch toggling from open to closed. What is the time-constant in this case?
- b) Sketch the output waveform for the switch toggling from closed to open. What is the time-constant in this case?

- 2) Consider the following inverter circuit.



$$\mu_n = 3\mu_p = 0.06 \text{ m}^2/\text{Vs}$$

$$C_{\text{ox}} = 8\text{fF}/\mu\text{m}^2$$

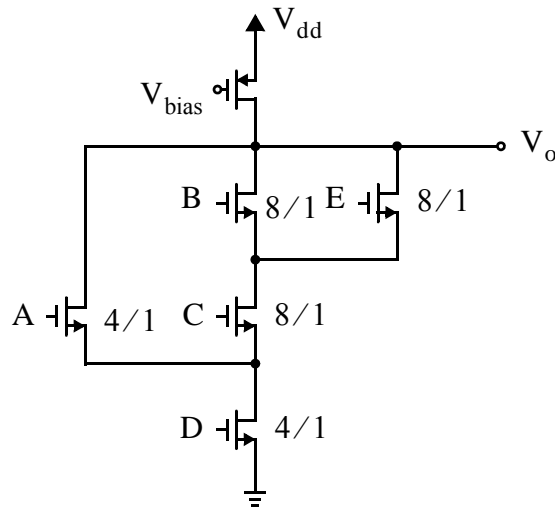
$$V_{\text{tn}} = 0.3\text{V}$$

- Sketch the input/output transfer curve.
- Find the threshold, V_{th} , of this inverter.
- Find the output logic high and output logic low levels (assume the current source cannot drive the output above V_{dd}).

For questions 3-6 below, assume $\mu_n = 3\mu_p = 0.06 \text{ m}^2/\text{Vs}$, $V_{\text{tn}} = -V_{\text{tp}} = 0.3\text{V}$, $C_{\text{ox}} = 8\text{fF}/\mu\text{m}^2$, and $V_{\text{dd}} = 2\text{V}$.

- Given a CMOS inverter with $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 10$, where the input is at V_{dd} , find the maximum current that the output can sink before the output rises above 0.2V .
- Given a CMOS inverter with $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 10$, where the input is at 0 , find the maximum current that the output can source before the output falls below 1.8V .
- Given a CMOS inverter with $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 10$, estimate its input capacitance if the minimum length of $0.3\mu\text{m}$ is used for both devices.
- Given a CMOS inverter with $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 10$, estimate its input capacitance if the length of $0.6\mu\text{m}$ is used for both devices.
- A 2.5V CMOS inverter is designed with the width of the PMOS equal to twice the width of the NMOS and $W_n = 1\mu\text{m}$. Considering only gate capacitance, estimate using an RC delay estimation of the average gate delay time, $t_{\text{av}} = (t_{+70} + t_{-70})/2$ if this inverter is driving 4 similar sized inverters. All lengths equal $0.25\mu\text{m}$. CMOS parameters: $\mu_n C_{\text{ox}} = 120\mu\text{A}/\text{V}^2$, $\mu_p C_{\text{ox}} = 30\mu\text{A}/\text{V}^2$, $V_{\text{tn}} = 0.45\text{V}$, $V_{\text{tp}} = -0.4\text{V}$, $C_{\text{ox}} = 6\text{fF}/\mu\text{m}^2$
- Using the concept of equivalent transistors, simplify the n-channel driver network shown below to a single pull-down transistor with a width of W_n and a length of $1\mu\text{m}$. Find this

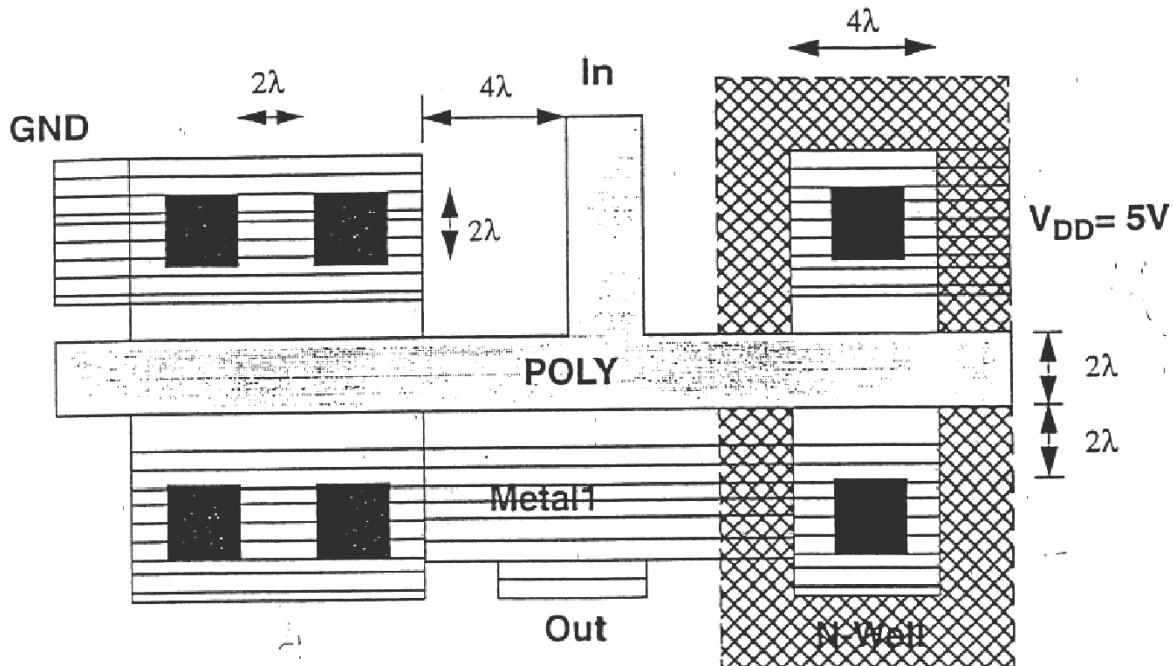
equivalent transistor for 2 cases: $W_{n(\text{fast})}$ representing the input pattern with the fastest pull-down and $W_{n(\text{slow})}$ for the slowest pull-down input case.



$$W_{n(\text{fast})} =$$

$$W_{n(\text{slow})} =$$

- 9) A single CMOS inverter is sized with minimum transistor lengths of $0.25\mu\text{m}$, NMOS width of $1\mu\text{m}$ and PMOS width of $2\mu\text{m}$. Given that the drain and source extensions are each $0.5\mu\text{m}$ past the gate, find the total load capacitance, C_L , (include appropriate drain and/or source to bulk capacitance as well as gate capacitance that the inverter drives) when the inverter drives 4 similar sized inverters all in parallel. (See last page for CMOS parameters).
- 10) A CMOS inverter layout is shown below. The scaling parameter is $\lambda = 0.125\mu\text{m}$.



a) Fill in the following lines of SPICE source code:

M1 out in vdd vdd pmos l= w= ad= pd= as= ps=

M2 out in gnd gnd nmos l= w= ad= pd= as= ps=

b) Using the parameters on the last page, estimate the total input capacitance of this inverter, C_{in} . Also, estimate the total parasitic capacitance at the output of the inverter, C_{out} .

c) The layout is missing two important connections. In fact, the inverter will not function properly without these connections. What are the missing connections?

Physical Constants:

$$\phi_T = kT/q = 26\text{mV (at 300K)}; k = 1.38 \times 10^{-23} \text{ J/K}; T = 300 \text{ K (at 27°C)}; q = 1.6 \times 10^{-19} \text{ C};$$

$$\epsilon_{\text{si}} = 1.05 \times 10^{-12} \text{ F/cm}; \phi_s = 2|\phi_F| = 0.6\text{V}$$

MOS Transistor: CMOS basic parameters. $V_{\text{dd}} = 2.5\text{V}$. Channel length = $0.25\mu\text{m}$

	V_{T0} (V)	γ ($\text{V}^{0.5}$)	μC_{ox} ($\mu\text{A}/\text{V}^2$)	λ (V^{-1})	C_{ox} ($\text{fF}/\mu\text{m}^2$)	C_o ($\text{fF}/\mu\text{m}$)	C_j ($\text{fF}/\mu\text{m}^2$)	C_{jsw} ($\text{fF}/\mu\text{m}$)
NMOS	0.4	0.4	120	0.06	6	0.3	2	0.3
PMOS	-0.4	0.4	30	0.1	6	0.3	2	0.3

V_{T0} is the threshold voltage with zero bulk-source voltage.

γ is used to account for non-zero bulk-source voltage.

μC_{ox} is the transistor current gain parameter.

λ is to account for the transistor finite output impedance (channel length modulation).

C_{ox} is the gate capacitance per unit area.

C_o is the gate overlap capacitance per unit length.

C_j is the drain/source junction capacitance per unit area.

C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. **Assume this value is the same for all 4 sides of the perimeter.**