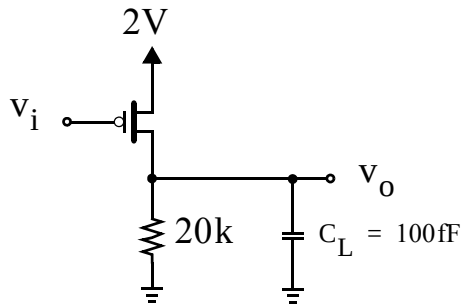
1) Given that a minimum size inverter has a gate capacitance of 3fF and it's inherent delay equals 15ps, find the number of inverters for an inverter chain that minimizes the propogation delay to drive a 20pF load when using a fan-out factor of 4 for inverter sizing. Also, what is the propogation delay?

4.27 A 180 nm standard cell process can have an average switching capacitance of 150 pF/mm$^2$. You are synthesizing a chip composed of random logic with an average activity factor of 0.1. Estimate the power consumption of your chip if it has an area of 70 mm$^2$ and runs at 450 MHz at $V_{DD}$ = 0.9 V.

4.28 You are considering lowering $V_{DD}$ to try to save power in a static CMOS gate. You will also scale $V_t$ proportionally. Will dynamic power consumption go up or down? Will static power consumption go up or down?

2) For the inverter shown below, estimate the static and dynamic power dissipation (due to capacitor charging/discharging) assuming the input is a 2V data signal that can change on every 10ns positive clock edge and the probability of a "1" at the input is 0.7. Also assume the logic high level of the output is 1.8V.

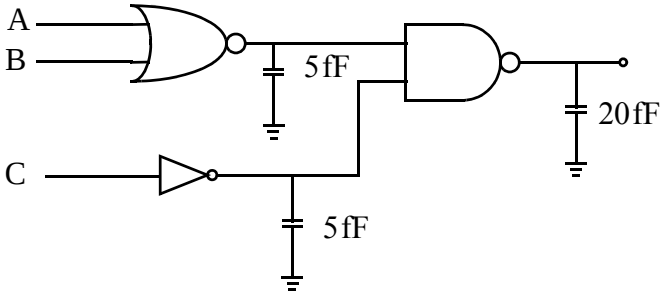



$P_{static}$ =

$P_{dynamic}$ =

3) Find the dynamic power dissipation, $P_{dyn}$, for the following CMOS circuit assuming the clock is 1GHz, $V_{DD}$ = 2V and the inputs have the following probability values that change on the positive edge of the clock.

P(A=1) = 0.4, P(B=1) = 0.2, P(C=1) = 0.5




$P_{dyn}$ =