Q1) Consider a bank of CMOS registers where $T_{\text{setup}} = 300 \text{ ps}$, $T_{\text{hold}} = 200 \text{ ps}$, $T_{\text{ccq}} = 100 \text{ ps}$ and $T_{\text{pcq}} = 250 \text{ ps}$. Also assume an average gate delay equals $T_{\text{gate}} = 50 \text{ ps}$.

a) If it is desired to run a system clock at 1GHz, how many gate delays can be in the logic between registers?

b) If there are 15 gate delays in the logic between registers, what is the maximum clock frequency?

c) To ensure no race conditions occur, what is the minimum number of gate delays that should exist between any two registers? How does the clock frequency affect this result?