In the Weste/Harris textbook: Chapter 7 questions shown below

7.23 A synchronizer uses a flip-flop with $\tau = 54$ ps and $T_0 = 21$ ps. Assuming the input toggles at 10 MHz and the setup time is negligible, what is the minimum clock period for which the mean time between failures exceeds 100 years?

7.25 Inferior Circuits, Inc., wants to sell you a perfect synchronizer that they claim never produces a metastable output. The synchronizer consists of a regular flip-flop followed by a high-gain comparator that produces a high output for inputs above $0.25 \cdot V_{DD}$ and a low output for inputs below that point. The VP of marketing argues that even if the flip-flop enters metastability, its output will hover near $V_{DD}/2$ so the synchronizer will produce a good high output after the comparator. Why wouldn’t you buy this synchronizer?

Q1) A regular synchronizer uses 2 registers (or flip-flops) in the synchronized clock domain and will be referred to here as a 2 flop synchronizer. A designer wants to compare a 2 flop synchronizer with a 3 flop synchronizer running at different speeds. For the same technology and assuming setup time is negligible, is a 3 flop synchronizer running at 40MHz
- more reliable (greater MTBF)
- equally reliable (same MTBF), or
- less reliable (less MTBF)
than a 2 flop synchronizer running at 20MHz?

Q2) A designer decides to implement a 2 flop synchronizer using the dynamic latches shown below (a single register is shown). Through simulations, the designer finds that $T_0$ (or equivalently, $t_{rd}$) equals 21ps.

Assuming the input toggles at 10 kHz and the setup time is negligible, what is the mean time between failures if the synchronizer is run at 500 MHz? Assume each inverter has a gain of $-20 \, \text{V/V}$ around it’s threshold voltage. (Recall, you want to ensure the input to the second register does NOT get sampled during the $t_{rd}$ time).