Q1) A dynamic memory (DRAM) cell has a capacitance of 0.1pF and is charged to \( V_{dd} = 3\) V when refreshed. The worst case leakage current of the cell is 2nA to ground and is independent of the DRAM cell voltage.

a) How often must the DRAM cell be refreshed if we do not allow the node voltage for a stored “one” to drop lower than \( V_{dd}/2 \). 

b) Assuming the leakage and charging currents of the cell capacitance are the cause of the dominant power dissipation, what is the worst case power dissipation for a DRAM array of 256 million \( (2^{28}) \) such nodes when all the memory cells contain a logic one and the refresh rate is that found in part a)
Q2) Consider an SRAM cell shown below where BL and BL are both precharged to $V_{DD} = 2.5V$ during a read operation.

![SRAM Cell Diagram](image)

a) Estimate the peak voltage at $V_A$ during a read operation when the cell stores a “one” at $V_B$.

b) Assuming this SRAM cell is one of 256 x 256 array, estimate the word line capacitance for a single row. Ignore any wiring capacitance.

c) Starting with the word line capacitance and working backwards to the smallest inverter, design a chain of inverters to drive the word line such that each inverter drives an equivalent fanout of 4 until the smallest inverter sized is reached (minimum width is 0.5um). Show transistor sizes for the inverter chain.

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all lengths = 0.25um

- $W_1 = 1.0\mu m$
- $W_3 = 0.5\mu m$
- $W_5 = 0.5\mu m$
- $\mu_nC_{ox} = 120 \mu A/V^2$
- $\mu_pC_{ox} = 30 \mu A/V^2$
- $V_{tn} = -V_{tp} = 0.4V$
Q3) Consider an SRAM cell shown below.

\[ \begin{align*}
\mu_n C_{ox} &= 120 \mu A/V \\
\mu_p C_{ox} &= 30 \mu A/V \\
V_{tn} &= |V_{tp}| = 0.4 V
\end{align*} \]

a) Find the NMOS transistor sizes so that during a read operation, the “0” internal node of the SRAM cell stays below \( V_{tn} \) even though the bit lines are precharged to \( V_{DD} \). In addition, let the smaller of the NMOS transistors have \( W/L = 1 \) with all transistor lengths equal to 0.25um.

b) Assume that the above SRAM is initially storing \( V_A = 2.5V \), \( V_B = 0V \) and \( BL = 0 \) and \( \overline{BL} = 2.5V \) and WL is initially low and a write sequence is activated by taking WL high. Sketch the waveforms of the signals, \( V_A \) and \( V_B \) making the simplifying assumptions that if a transistor is in active or triode, then the transistor is modelled as a 1k resistor if M1/M2, a 10k resistor if M3/M4 and a 100k resistor if M5/M6. Determine time constants within 20% accuracy (so a 1k in parallel with a 10k or 100k can be approximated as a 1k). Ignore all capacitances except for the shown 10fF capacitors.