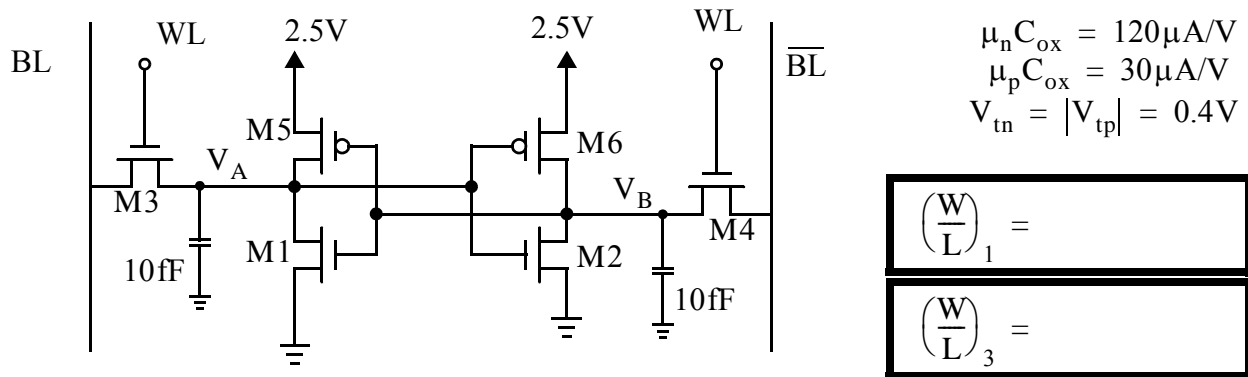


In the Weste/Harris textbook: Chapter 11 questions shown below

- 11.1 An embedded SRAM contains 2048 8-bit words. If it is physically arranged in a square fashion, how many inputs does each column multiplexer require?
(assume cell aspect ratio is square)
 - 11.2 Estimate the dimensions of the SRAM array in Exercise 11.1 using the SRAM cell from Figure 11.6b, assuming periphery circuitry adds 10% to each dimension of the core.
 - 11.3 Sketch designs for a 6:64 decoder with and without predecoding. Comment on the pros and cons of predecoding.
(a 6:64 decoder has a 6 bit input and 64 outputs)
 - 11.8 Explain the tradeoffs between open, closed, and twisted bitlines in a dynamic RAM array.
 - 11.9 Sketch a dot diagram for a 2-input XOR using a ROM.
 - 11.12 Explain the advantages and disadvantages of NAND ROMs as compared to NOR ROMs.
- Q1) A dynamic memory (DRAM) cell has a capacitance of 0.1pF and is charged to $V_{dd} = 3V$ when refreshed. The worst case leakage current of the cell is 2nA to ground and is independent of the DRAM cell voltage.
- a) How often must the DRAM cell be refreshed if we do not allow the node voltage for a stored “one” to drop lower than $V_{dd}/2$.
 - b) Assuming the leakage and charging currents of the cell capacitance are the cause of the dominant power dissipation, what is the worst case power dissipation for a DRAM array of 256 million ($= 2^{28}$) such nodes when all the memory cells contain a logic one and the refresh rate is that found in part a)

Q3) Consider an SRAM cell shown below.



a) Find the NMOS transistor sizes so that during a read operation, the “0” internal node of the SRAM cell stays below V_{tn} even though the bit lines are precharged to V_{DD} . In addition, let the smaller of the NMOS transistors have $W/L = 1$ with all transistor lengths equal to 0.25um.

b) Assume that the above SRAM is initially storing $V_A = 2.5\text{V}$, $V_B = 0\text{V}$ and $BL = 0$ and $\overline{BL} = 2.5\text{V}$ and WL is initially low and a write sequence is activated by taking WL high. Sketch the waveforms of the signals, V_A and V_B making the simplifying assumptions that if a transistor is in active or triode, then the transistor is modelled as a 1k resistor if M1/M2, a 10k resistor if M3/M4 and a 100k resistor if M5/M6. Determine time constants within 20% accuracy (so a 1k in parallel with a 10k or 100k can be approximated as a 1k). Ignore all capacitances except for the shown 10fF capacitors.

