2.5 The minimum size diffusion contact is \(4 \times 5 \lambda\), or \(1.2 \times 1.5 \mu m\). The area is \(1.8 \mu m^2\) and perimeter is \(5.4 \mu m\). Hence the total capacitance is

\[C_{db}(0V) = (1.8)(0.42) + (5.4)(0.33) = 2.54 \mu F\]

At a drain voltage of \(V_{DD}\), the capacitance reduces to

\[C_{db}(5V) = (1.8)(0.42)\left(1 + \frac{5}{0.98}\right)^{-0.44} + (5.4)(0.33)\left(1 + \frac{5}{0.98}\right)^{-0.12} = 1.78 \mu F\]

2.6 The new threshold voltage is found as

\[\phi_s = 2(0.026)\ln \frac{2 \cdot 10^{17}}{1.45 \cdot 10^{16}} = 0.85V\]

\[\gamma = \frac{100 \cdot 10^{-8}}{3.9 \cdot 8.85 \cdot 10^{-14}} \sqrt{2 \left(1.6 \cdot 10^{-19}\right)\left(11.7 \cdot 8.85 \cdot 10^{-14}\right)\left(2 \cdot 10^{17}\right)} = 0.75V^{1/2}\]

\[V_t = 0.7 + \gamma \left(\sqrt{\phi_s} + 4 - \sqrt{\phi_s}\right) = 1.66V\]

The threshold increases by \(0.96V\).

2.7 No. Any number of transistors may be placed in series, although the delay increases with the square of the number of series transistors.

2.8 The threshold is increased by applying a negative body voltage so \(V_{db} > 0\).

2.9 (a) \((1.2 - 0.3) / (1.2 - 0.4) = 1.26 \ (26\%)\)

\(\frac{e^{-0.3}}{1.4 \cdot 0.026} = 15.6\)

(b) \(\frac{e^{-0.4}}{1.4 \cdot 0.026} = 8.2\)

(c) \(v_T = kT/q = 34 \text{ mV}; \ \frac{e^{-0.3}}{1.4 \cdot 0.034} = 8.2\)

will normally be higher for both threshold voltages at high temperature.

2.10 The current through an ON transistor tends to decrease because the mobility goes down. The current through an OFF transistor increases because \(V_t\) decreases. A chip will operate faster at low temperature.
1) a) \[ V_{CL} = (R_1 / (R_1 + R_S)) C_L = 16.7 \text{ ps} \]

\[ V_{OL} = (1.2 \text{ V}) \left( \frac{R_S}{R_S + R_1} \right) = 0.2 \text{ V} \]

b) \[ C_L = R_1 C_L = 100 \text{ ps} \]

2) b) \[ V_{TH} \text{ occurs for } V_0 = V_T \text{ therefore } \]

NMOS in saturation region \( (V_{GS} = V_{DS}) \)

\[ \mu_n C_{OX} = (0.06 \text{ m}^2/\text{V} \cdot \text{s}) \cdot (8 \times 10^{-3} \text{ F/m}^2) = 480 \text{ mA/V}^2 \]

\[ I_{DN} = \frac{\mu_n C_{OX} (W/L)}{2} \left[ V_{TH} - V_{TN} \right]^2 \]

\[ 500 \text{ mA} = \frac{(480 \times 10^{-6}) (10)}{2} \left[ V_{TH} - 0.3 \right]^2 \]

\[ V_{TH} = 0.756 \text{ V} \]
2c) For $V_I = 0 \Rightarrow V_{OH} = V_{DD}$

For $V_I = V_{DD} \Rightarrow$ NMOS in TRIODE

$$I_{ON} = \frac{mnC_{ox}W}{L}[(V_{GS} - V_{TN})V_{OS} - \frac{V_{OS}}{2}]$$

Here $I_{ON} = 500 \text{ mA}$, $V_{GS} = V_{DD}$, $V_{OS} = V_{OL}$

$$500 \times 10^{-6} = (480 \times 6)(10)[(2 - 0.3)V_{OL} - \frac{V_{OL}^2}{2}]$$

$$V_{OL} = 0.062 \text{ V or } 3.34 \text{ V}$$

$\underline{\text{NOT POSSIBLE}}$

Since out of TRIODE

3) $I_{source} = ? \text{ when } V_o = 0.2 \text{ V}$

$$I_{source} = (480 \times 6)(10)[(2 - 0.3)0.2 - \frac{0.2^2}{2}]$$

$$= 1.536 \text{ mA}$$
4) Similar to 3)

\[ I_{sink} = (160 \times 10^{-6})(10) \left[ (-2 + 0.3)(-0.2) + \frac{(0.2)^2}{2} \right] \]

\[ = 512 \, \text{mA} \]

5) \( C_{in} = C_{gap} + C_{gap} \)

\[ = C_{ox} \times W_{MN} + C_{ox} \times W_{PLP} \]

\[ = (8)(3)(0.3) + (8)(3)(0.3) \]

\[ = 14.4 \, \text{fF} \]

6) Since length & width are 2 times sizes of 5), then \( C_{in} \) is 4 times

\[ C_{in} = 4 \times 14.4 \, \text{fF} = 57.6 \, \text{fF} \]