

SOLUTIONS

The output voltage in region B is found by solving

$$\frac{\beta_n}{2}(V_{in} - V_{tn})^2 = \beta_p \left((V_{in} - V_{DD}) - \frac{(V_{out} - V_{DD})}{2} - V_{tp} \right) (V_{out} - V_{DD})$$

$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - \frac{\beta_n}{\beta_p} (V_{in} - V_{tn})^2 + V_{DD} (V_{DD} - 2V_{in} + 2V_{tp})}$$

and the output voltage in region D is

$$\frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2 = \beta_n \left(V_{in} - V_{tn} - \frac{V_{out}}{2} \right) (V_{out})$$

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{\beta_p}{\beta_n} (V_{DD} - V_{in} + V_{tp})^2}$$

2.19 Take derivatives or solve numerically for the unity gain points: $V_{IL} = 0.43$ V, $V_{IH} = 0.50$ V, $V_{OL} = 0.04$ V, $V_{OH} = 0.97$ V, NM_H = 0.39, NM_L = 0.47 V.

2.20 The nMOS is in the linear region and the pMOS is saturated. By KCL

$$\beta_n \left(V_{DD} - V_{tn} - \frac{V_{out}}{2} \right) V_{out} = \frac{\beta_p}{2} (V_{DD} + V_{tp})^2$$

$$V_{out} = (V_{DD} - V_{tn}) - \sqrt{(V_{DD} - V_{tn})^2 - \frac{\beta_p}{\beta_n} (V_{DD} + V_{tp})^2}$$

***see Uyemura p. 343 EQ 9.5 for solution to check

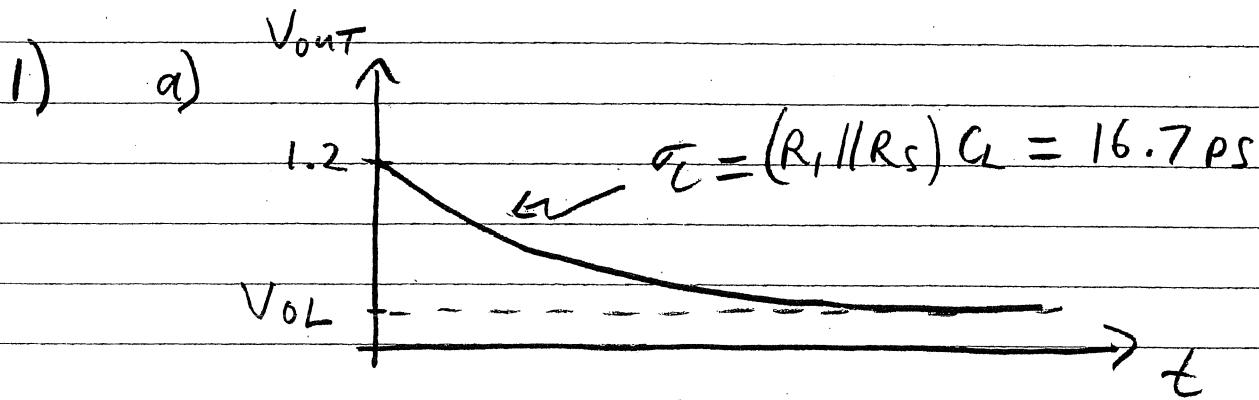
2.21 (a) 0; (b) $2|V_{tp}|$; (c) $|V_{tp}|$; (d) $V_{DD} - V_{tn}$

2.22 (a) 0; (b) 0.6; (c) 0.8; (d) 0.8

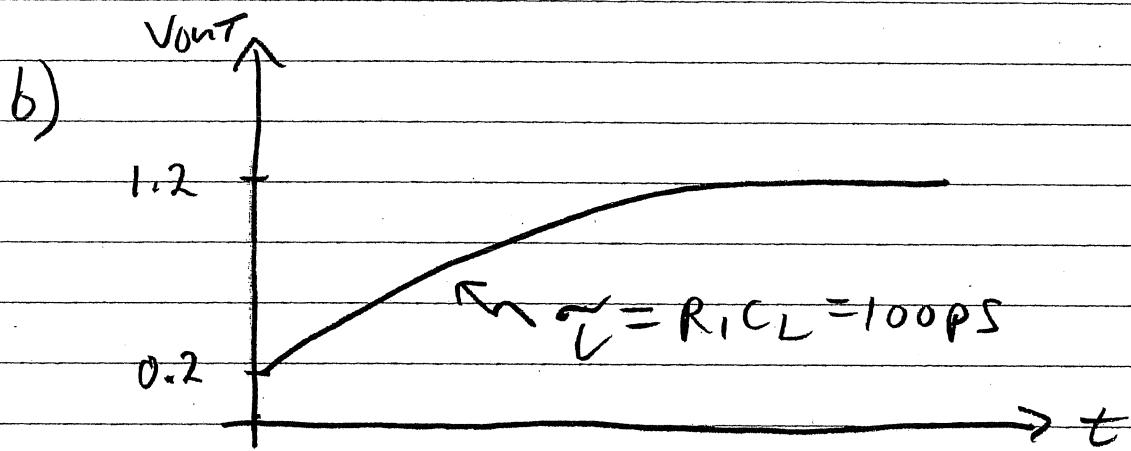
CHAPTER 3

3.1 First, the cost per wafer for each step and scan. 248nm – number of wafers for four years = $4*365*24*80 = 2,803,200$. 157nm = $4*365*24*20 = 700,800$. The cost per wafer is the (equipment cost)/(number of wafers) which is for 248nm \$10M/2,803,200 = \$3.56 and for 147nm is \$40M/700,800 = \$57.08. For a run through the equipment 10 times per completed wafer is \$35.60 and \$570.77 respectively.

Now for gross die per wafer. For a 300mm diameter wafer the area is roughly 70,650 mm² ($\pi*(r^2/A - r/(sqrt(2*A)))$). For a 50mm² die in 90nm, there are 1366 gross die per wafer. Now for the tricky part (which was unspecified in the question and could



$$V_{oL} = (1.2V) \left(\frac{R_S}{R_S + R_1} \right) = 0.2V$$



2) b) V_{TH} occurs for $V_o = V_I$ THEREFORE

SINCE
NMOS IN SATURATION REGION ($V_{GS} = V_{DS}$)
 $\mu_N C_{ox} = (0.06 \text{ m}^2/\text{Vs})(8 \times 10^{-3} \text{ F/m}^2) = 480 \text{ }\mu\text{A/V}^2$

$$I_{DN} = \frac{\mu_N C_{ox}}{2} \left(\frac{W}{L} \right) [V_{TH} - V_{TN}]^2$$

$$500 \text{ mA} = \frac{(480 \text{ e-6})}{2} (10) [V_{TH} - 0.3]^2$$

$$\underline{\underline{V_{TH} = 0.756 \text{ V}}}$$

2(c) FOR $V_I = 0 \Rightarrow V_{OH} = V_{DD}$

FOR $V_I = V_{DD} \Rightarrow NMOS \text{ in TR(ODE)}$

$$I_{DN} = \mu n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

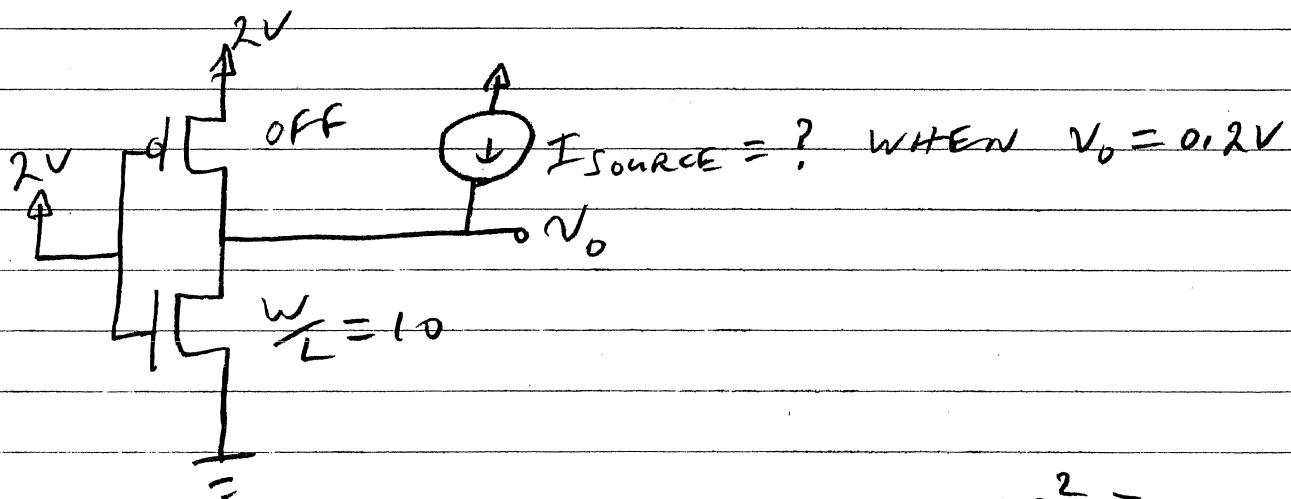
HERE $I_{DN} = 500 \mu A$, $V_{GS} = V_{DD}$, $V_{DS} = V_{OL}$

$$500 \times 10^{-6} = (480 \times 10^{-6})(10) \left[(2 - 0.3) V_{OL} - \frac{V_{OL}^2}{2} \right]$$

$V_{OL} = 0.062 \text{ V}$ OR ~~3.3 V~~

NOT POSSIBLE
SINCE OUT OF
TR(ODE)

3)



$$I_{SOURCE} = (480 \times 10^{-6})(10) \left[(2 - 0.3) 0.2 - \frac{0.2^2}{2} \right]$$

$= 1.536 \text{ mA}$

4) SIMILAR TO 3)

$$I_{SINK} = (160 \text{ e-6})(10) \left[(-2 + 0.3)(-0.2) + \frac{(-0.2)^2}{2} \right]$$
$$= \underline{\underline{512 \mu\text{A}}}$$

5) $C_{IN} = C_{gDN} + C_{gDP}$

$$= C_{ox} W_N L_N + C_{ox} W_P L_P$$

$$= (8)(3)(0.3) + (8)(3)(0.3)$$

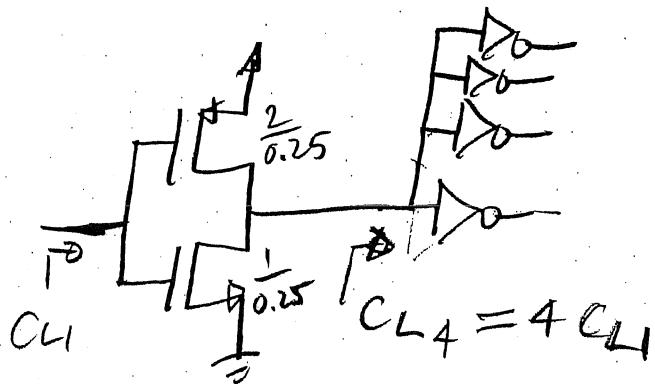
$$= 14.4 \text{ fF}$$

6) SINCE LENGTH + WIDTH ARE 2 TIMES SIZES OF 5), THEN C_{IN} IS 4 TIMES

$$C_{IN} = 4 \times 14.4 \text{ fF} = 57.6 \text{ fF}$$

7)

- Question 5:** A 2.5V CMOS inverter is designed with the width of the PMOS equal to twice the width of the NMOS and $W_n = 1\text{ um}$. Considering only gate capacitance, estimate the average gate delay time, $t_{av} = (t_{+70} + t_{-70})/2$ if this inverter is driving 4 similar sized inverters. All lengths equal 0.25um. See last page for CMOS parameters.



$$t_{av} = 81 \text{ ps}$$

$$C_{L1} = C_0 \times (1 \times 0.25 + 2 \times 0.25) = (6 \text{ fF}/(\mu\text{m})^2)(0.75) \\ = 4.5 \text{ fF}$$

$$C_{L4} = 4C_{L1} = 18 \text{ fF}$$

$$R_{EQN} = \frac{2.5}{m_n C_0 x \left(\frac{W}{L} \right)_N (V_{DD} - V_{TN})} = \frac{2.5}{(12 \times 10^{-6})(4)(2.5 - 0.45)} \\ = 2.541 \text{ k}\Omega$$

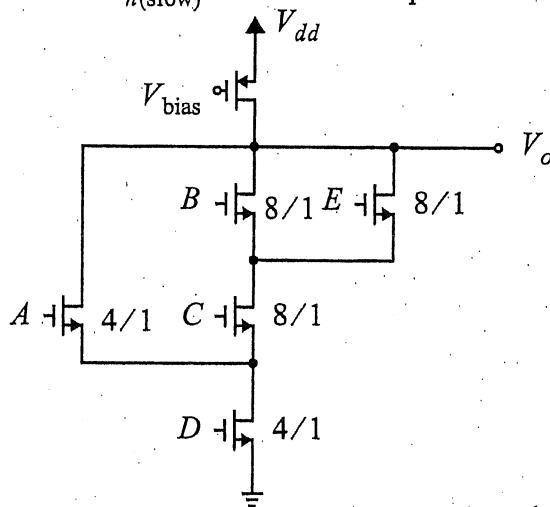
$$R_{EQP} = \frac{2.5}{m_p C_0 x \left(\frac{W}{L} \right)_P (V_{DD} + V_{TP})} = \frac{2.5}{(30 \times 10^{-6})(8)(2.5 + 0.4)} \\ = 4.96 \text{ k}\Omega$$

$$t_{av} = 1.2 \left(\frac{R_{EQN} + R_{EQP}}{2} \right) C_{L4}$$

$$= 81 \text{ ps}$$

8)

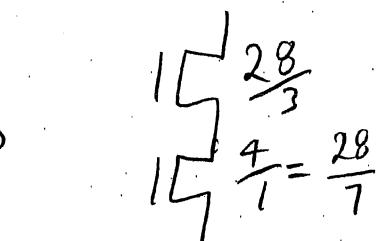
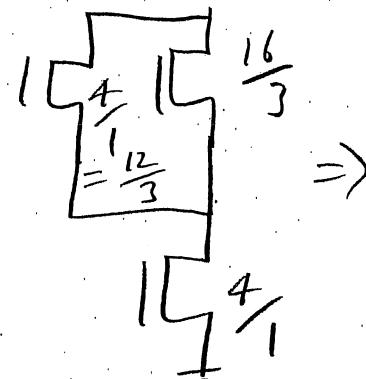
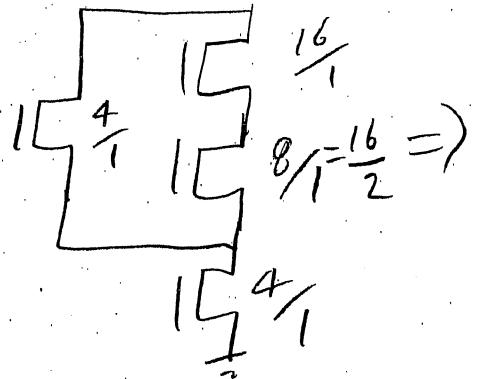
15.1 Question: Using the concept of equivalent transistors, simplify the n-channel driver network shown below to a single pull-down transistor with a width of W_n and a length of 1um. Find this equivalent transistor for 2 cases: $W_{n(\text{fast})}$ representing the input pattern with the fastest pull-down and $W_{n(\text{slow})}$ for the slowest pull-down input case.



$$W_{n(\text{fast})} = 2.8 \mu\text{m}$$

$$W_{n(\text{slow})} = 2.0 \mu\text{m}$$

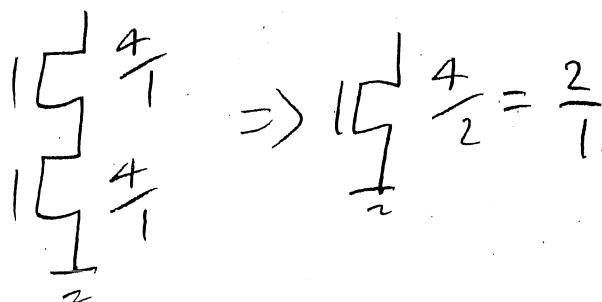
$W_N(\text{FAST})$ ALL inputs = "1"



$$\Rightarrow \boxed{\frac{28}{10} = \frac{2.8}{1.0}}$$

$W_N(\text{slow})$

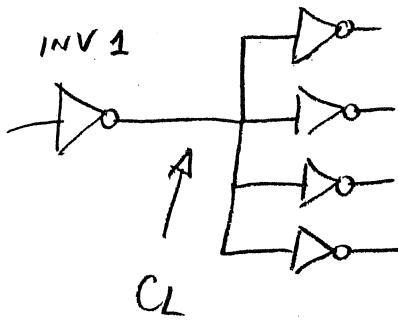
$$\text{EITHER } \begin{cases} A=1 & D=1 \\ B=C=E=0 \end{cases} \quad \begin{cases} A=0 & D=1 \\ C=1 & B \text{ or } E=1 \end{cases}$$



9)

- [5] **Question 1:** A single CMOS inverter is sized with minimum transistor lengths of 0.25um, NMOS width of 1um and PMOS width of 2um. Given that the drain and source extensions are each 0.5um past the gate, find the total load capacitance, C_L , (include appropriate drain and/or source to bulk capacitance as well as gate capacitance that the inverter drives) when the inverter drives 4 similar sized inverters all in parallel. (See last page for CMOS parameters).

$$C_L = 25 \text{ fF}$$



$$C_L = 4 C_{INV} + C_{dBP} + C_{dB_N}$$

$$C_{INV} = C_{ox} W_p L_p + C_{ox} W_n L_n = (6)(2)(0.25) + (6)(1)(0.25) \\ = 4.5 \text{ fF}$$

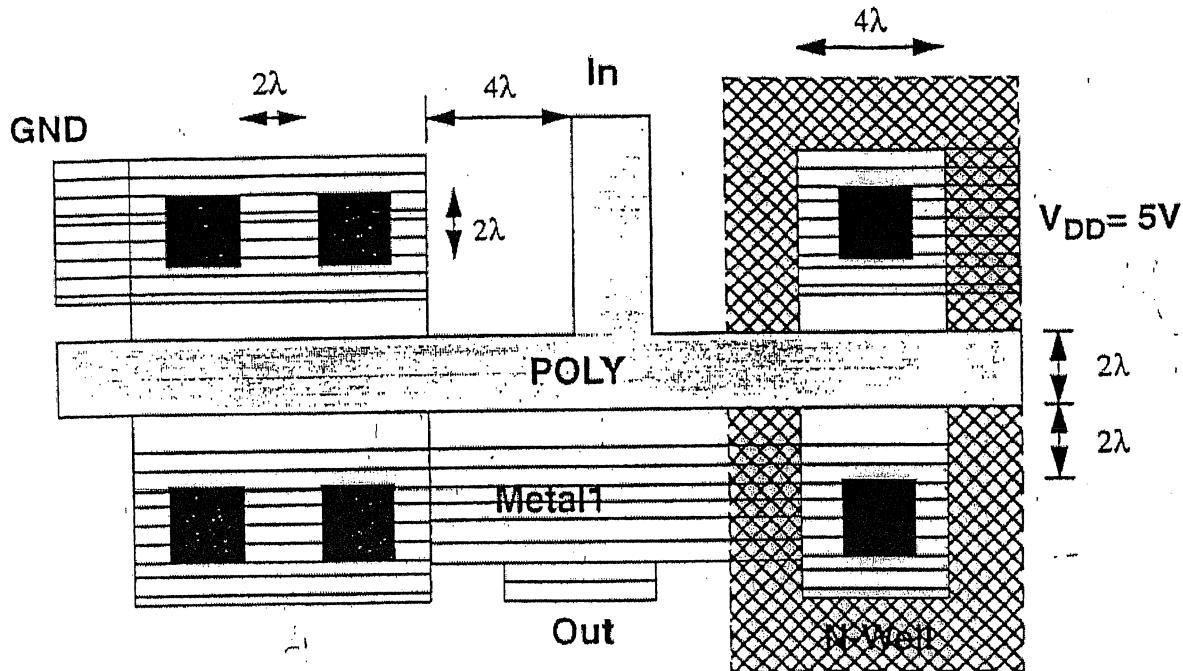
$$C_{dBP} = (C_J)(W_p)(0.5) + (C_{Jsw})(2[W_p + 0.5]) \\ = (2)(2)(0.5) + (0.3)[2[2 + 0.5]] \\ = 3.5 \text{ fF}$$

$$C_{dB_N} = (C_J)(W_N)(0.5) + C_{Jsw}(2[W_p + 0.5]) = C_{dBP} \\ = 3.5 \text{ fF}$$

$$C_L = 4(4.5) + 3.5 + 3.5 = \underline{\underline{25 \text{ fF}}}$$

(10)

[6] Question 1: A CMOS inverter layout is shown below. The scaling parameter is $\lambda = 0.125\mu\text{m}$.



a) Fill in the following lines of SPICE source code:

$3.13e-13$ $3.13e-13$
 M1 out in vdd vdd pmos l= 0.25μ w= 1μ ad= 4λ pd= 2.25μ as= 2.25μ ps= 2.25μ

M2 out in gnd gnd nmos l= 0.25μ w= 1μ ad= 4λ pd= 3.25μ as= 3.25μ ps= 3.25μ

$$L_p = L_N = 2\lambda = 0.25\mu \quad 6.25e-13 \quad 6.25e-13$$

$$W_p = 4\lambda = 0.5\mu$$

$$W_N = 8\lambda = 1\mu$$

$$\cancel{PMOS} \quad A_D = A_S = 4\lambda \times 5\lambda = 20\lambda^2 = 3.13e+13$$

$$P_D = P_S = 2(4\lambda + 5\lambda) = 18\lambda = 2.25\mu$$

NMOS

$$A_D = A_S = 8\lambda \times 5\lambda = 40\lambda^2 = 6.25e-13$$

$$P_D = P_S = 2(8\lambda + 5\lambda) = 26\lambda = 3.25\mu$$

b) Using the parameters on the last page, estimate the total input capacitance of this inverter, C_{in} . Also, estimate the total parasitic capacitance at the output of the inverter, C_{out} .

$$C_{in} = C_{ox}(W_N L_N) + C_{ox}(W_P L_P)$$

$$= (6)((1)(0.25)) + (6)((0.5)(0.25))$$

$$= 2.25 \text{ fF} \quad \left(\begin{array}{l} \text{IF } C_0 \text{ increased} \\ C_{in} = 2.25 \text{ fF} + C_0 (3 \mu\text{m}) \\ = 3.15 \text{ fF} \end{array} \right)$$

$$C_{out} = C_j(A_{DN} + A_{DP}) + C_{jSW}(P_{DN} + P_{DP})$$

$$= 2(0.625 + 0.313) + 0.3(3.25 + 2.25)$$

$$= 1.88 \text{ fF} + 1.65$$

$$= \underline{\underline{3.5 \text{ fF}}}$$

c) The layout is missing two important connections. In fact, the inverter will not function properly without these connections. What are the missing connections?

- SUBSTRATE CONNECTION TO P-SUBSTRATE

AND N-WELL CONNECTION ARE MISSING

- P-SUBSTRATE SHOULD CONNECT TO GND

- N-WELL CONNECTION SHOULD CONNECT TO VDD