6.41 *** simulation

6.42 When the clock is low, the two outputs equalize at \( V_{DD}/2 \). When the clock rises, one side pulls down, fully turning ON the pMOS transistor to pull the other side up. This gate saves precharge power relative to dynamic logic because the precharge equalizes the two outputs rather than drawing power from the rail. The partial swing may lead to faster transitions. However, it consumes extra power early in evaluation because of contention between the partially ON pMOS transistor and the ON pulldown stack.

\[ \phi \]
\[ \gamma / \bar{\gamma} \]

6.43 n/a

Chapter 7

7.1 (a) \( t_{pd} = 500 - (50 + 65) = 385 \) ps; (b) \( t_{pd} = 500 - 2(40) = 420 \) ps; (c) \( t_{pd} = 500 - 40 = 460 \) ps.

7.2 (a) \( t_{pd} = 500 - (50 + 65 + 50) = 335 \) ps; (b) \( t_{pd} = 500 - 2(40) = 420 \) ps; (c) \( t_{pd} = 500 - (50 + 25 - 80 + 50) = 455 \) ps.

7.3 (a) \( t_{cd} = 30 - 35 = 0 \); (b) \( t_{cd} = 30 - 35 = 0 \); (c) \( t_{cd} = 30 - 35 - 60 = 0 \); (d) \( t_{cd} = 30 - 35 + 80 = 75 \) ps.

7.4 (a) \( t_{cd} = 30 - 35 + 50 = 45 \) ps; (b) \( t_{cd} = 30 - 35 + 50 = 45 \) ps; (c) \( t_{cd} = 30 - 35 + 50 - 60 = 0 \); (d) \( t_{cd} = 30 - 35 + 80 + 50 = 125 \) ps.

7.5 (a) \( t_{borrow} = 0 \); (b) \( t_{borrow} = 250 - 25 = 225 \) ps; (c) \( t_{borrow} = 250 - 25 - 60 = 165 \) ps; (d) \( t_{borrow} = 80 - 25 = 55 \) ps.

7.6 (a) \( t_{borrow} = 0 \); (b) \( t_{borrow} = 250 - 25 - 50 = 175 \) ps; (c) \( t_{borrow} = 250 - 25 - 60 - 50 = 115 \) ps; (d) \( t_{borrow} = 80 - 25 - 50 = 5 \) ps.

7.7 If the pulse is wide and the data arrives while the pulsed latch is transparent, the latch contributes its D-to-Q delay just like a regular transparent latch. If the pulse is narrow, the data will have to setup before the earliest skewed falling edge. This is at time \( t_{setup} - t_{pw} + t_{skew} \) before the latest rising edge of the pulse. After the rising edge, the latch contributes a clk-to-Q delay. Hence, the total sequencing overhead is \( t_{pcq} = t_{setup} - t_{pw} + t_{skew} \).

7.8 \( t_{setup} = t_{setup} + t_{nonoverlap} \), \( t_{hold} = t_{hold} - t_{nonoverlap} \), \( t_{pcq} = t_{pcq} \).

7.9 (a) 1200 ps: no latches borrow time, no setup violations. 1000 ps: 50 ps borrowed
Q1)

\[ D = k(50 \text{ps}) \text{ where } k \text{ is \# of gate delays} \]

\[ T_{\text{CLK}} = \frac{1}{16 \text{Hz}} = 1 \text{ms} \]

\[ a) \quad T_{\text{CLK}} \geq t_{\text{pcq}} + D + t_{\text{setup}} \]

\[ 1 \text{ms} \geq 250 \text{ps} + k(50 \text{ps}) + 300 \text{ps} \]

\[ k \leq \frac{1000 - 300 - 250}{50} = 9 \]

Maximum of 9 gate delays

\[ b) \quad T_{\text{CLK}} \geq 250 \text{ps} + 15(50 \text{ps}) + 300 \]

\[ \geq 1300 \text{ps} \]

\[ F_{\text{CLK}} = \frac{1}{T_{\text{CLK}}} = 769 \text{MHz} \text{ (MAX clock freq)} \]

\[ c) \quad \text{To ensure no race conditions} \]

\[ t_{\text{ccq}} + k(50 \text{ps}) \geq t_{\text{hold}} \]

\[ 100 + k(50 \text{ps}) \geq 200 \text{ps} \Rightarrow k \geq 2 \text{ gate delays} \]

Not affected by clock freq.