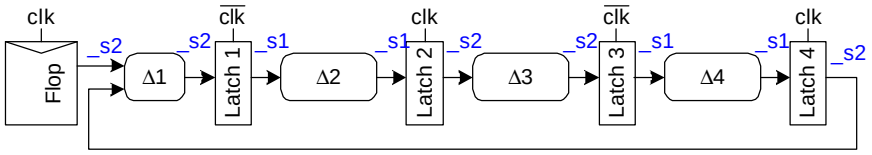
through L1, 130 ps through L2, 80 ps through L3. 800 ps: 150 ps borrowed through L1, 330 ps borrowed through L2, L3 misses setup time.

(b) 1200 ps: no latches borrow time, no setup violations. 1000 ps: 100 ps borrowed through L2, 50 ps through L4. 800 ps: 200 ps borrowed through L2, 200 ps borrowed through L3, 350 ps borrowed through L4, 250 ps borrowed through L1, L2 then misses setup time.

7.10 (a) 700 ps; (b) 825 ps; (c) 1200 ps.

7.11 (a) 700 ps; (b) 825 ps; (c) 1200 ps. The transparent latches are skew-tolerant and moderate amounts of skew do not slow the cycle time.

7.12



7.13 *** simulation

7.14 *** simulation

7.15 t_{pd} = 500 - 2(40) = 420 ps.

7.16 t_{pd} = 500 - 2(40 + 50) = 320 ps.

7.17 t_{pd} = 500 ps. Skew-tolerant domino with no latches has no sequencing overhead.

7.18 t_{pd} = 500 ps. The path can tolerate moderate amounts of skew without degradation.

7.19 t_{borrow} = 125 ps - 50 ps - t_{hold} = 75 ps - t_{hold}.

7.20 t_{borrow} = (0.65-0.25)*500 - 50 ps - t_{hold}= 150 ps - t_{hold}.

7.21 *** simulation

7.22 *** simulation

7.23 Solve for T_c:

$$100 \text{ years} = \frac{T_c e^{\frac{T_c}{54 \text{ ps}}}}{(10^7)(21 \text{ ps})} \Rightarrow T_c = 1811 \text{ ps}$$

7.24 *** simulation

7.25 If the output goes metastable near $V_{DD}/2$, the flip-flop will indeed produce a good high output. However, when it resolves from metastability, the output might suddenly fall low. Because the resolution time can be unbounded, the clock-to-Q delay of the synchronizer is also unbounded. The problem with synchronizers is not that their output takes on an illegal logic level for a finite period of time (all logic gates

do that while switching), but rather that the delay for the output to settle to a correct value cannot be bounded. With high probability it will eventually resolve, but without knowing more about the internal characteristics of the flip-flop, it is dangerous to make assumptions about the probability.

Chapter 8

8.1 Selection of a gate array cell comes down to selecting the number of transistors to place in series in a cell, remembering that if a cell uses less transistors, then the extra transistors are not utilized. We can categorize individual gates by the number of series transistors they require (i.e. an n-strip below a p-strip, as in Figure 8.28). The following table summarizes the usage in particular chip in the exercise:

Cell Type	Series transistors	Circuit	Percentage
D-latch	5	Figure 7.17f with clock inverter	
D-flipflop	10	Two D-latches	
Scannable D-flipflop	15-16	Allowing for input multiplexer	30
4 input gate	4		10
3 input gate	3		10
2 input gate	2		40
buffers	various		10

Clearly if we were to center on a D-flop, and use a five series transistor cell, at least 60% of the gates would waste transistors (2,3,4 input gates). As an aside, a scannable D-register would need three blocks if they were 5 transistor series blocks.

While we can guess, a little bit of analysis might help. The pitch of a contacted transistor is 8λ (Exercise 3.7). (However see Exercise 8.5 where this gets blown out to 14λ if interior poly-contacts are required. For this exercise we'll stick with 8λ.) A break in the active area adds 3λ (Table 3.2 Rule 2.2). So the pitch of various gate arrays is as follows:

Series Transistors	Pitch	
2	2*8+3	19

Q1)

$$MTBF = \frac{T_C \, e^{\frac{T}{\tau_S}}}{t_{rD} \, F_D}$$

FOR 2 FLOP SYNCHRONIZER $T_C = \frac{1}{20MHz} = 50ns$

$$T = T_C = 50ns$$

$$MTBF_2 = \frac{(50e\text{-}9) \, e^{\frac{(50e\text{-}9)}{\tau_S}}}{\tau_{rD} \, F_D}$$

FOR 3 FLOP SYNCHRONIZER $T_C = \frac{1}{40MHz} = 25ns$

& $T = 2T_C = 50ns$

$$MTBF_3 = \frac{(25e\text{-}9) \, e^{\left(\frac{50e\text{-}9}{\tau_S}\right)}}{\tau_{rD} \, F_D}$$

SO $$MTBF_3 = \frac{MTBF_2}{2}$$

⇒ LESS RELIABLE BY FACTOR OF 2
(WHICH IS NOT A LOT IN FAILURE ANALYSIS)

Q2 NO REGENERATION USED

BUT GAIN OF $20 \times 20 = 400$ V/V

FROM INPUT TO OUTPUT OF

SINGLE REGISTER.

$$t_{rD}' = \frac{t_{rD}}{400} \qquad T_C = \frac{1}{500\text{MHz}} = 2\text{ns}$$

$$\text{MTBF} = \frac{T_C}{t_{rD}' F_D} = \frac{2\text{ns}(400)}{(21e\text{-}12)(1e4)}$$

$$= 3.8\text{ s}$$

FAILS EVERY 4 s