

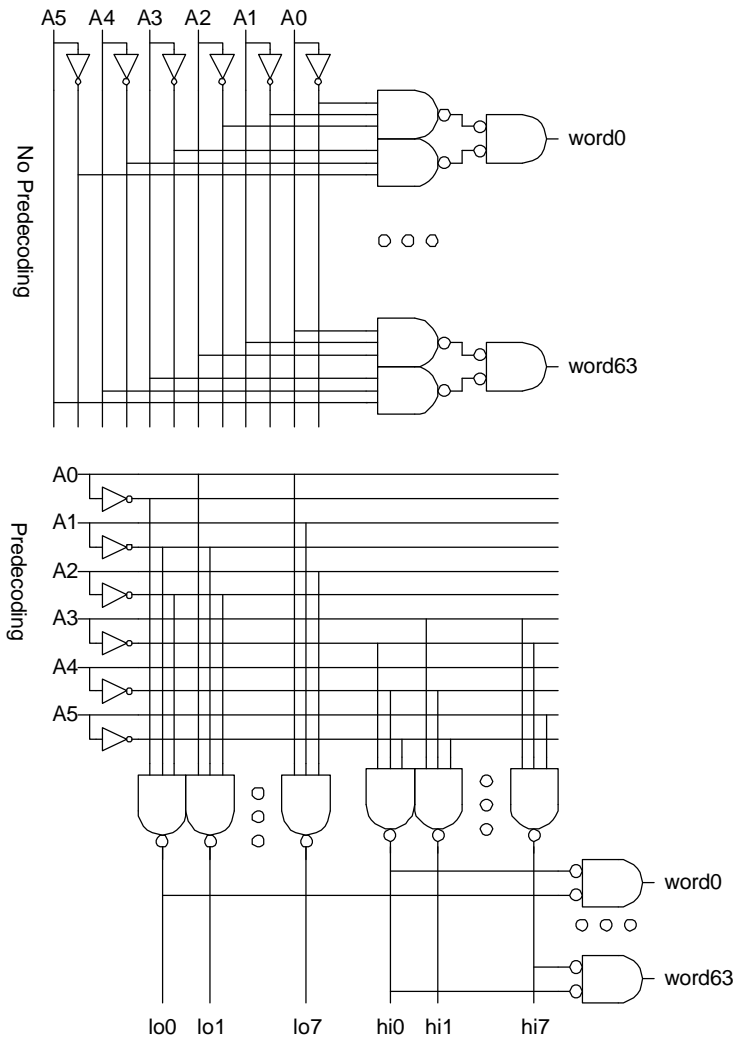
- 10.21 Assume the branching effort on each A input is approximate 2 because it drives two gates (the initial inverter and the final AND). A path from input to output passes through an inverter and five AND gates, each made from a NAND and an inverter. There are four two-way branches within the network. Hence, $B = 32$. $G = 1^{6*}(4/3)^5 = 4.2$. $H = 1$. $P = 1*6 + 2*5 = 16$. $F = GBH = 135$. $N = 11$. $f = F^{1/N} = 1.56$. $D = Nf + P = 33.2 \tau$. Note that the stage effort is lower than that desirable for a fast circuit. The circuit might be redesigned with NANDs and NORs in place of ANDs to reduce the number of stages and the delay.
- 10.22 The following equations are a slight modification of EQ.10.50. Use the base case $X_{1:1} = 1$, $W_{1:1} = 0$.

$$\begin{aligned}
 X_{i:i} &= \overline{A_i A_{i-1}} && \text{bitwise precomputation} \\
 W_{i:i} &= A_i \overline{A_{i-1}} \\
 X_{i:j} &= X_{i:k} \cdot X_{k-1:j} && \text{group logic} \\
 W_{i:j} &= W_{i:k} \cdot X_{k-1:j} + X_{i:k} \cdot W_{k-1:j} \\
 Y_i &= W_{i:i} \cdot W_{i-1:1} && \text{output logic}
 \end{aligned}$$

Chapter 11

- 11.1 If the array is organized as 128 rows by 128 columns, each column multiplexer must choose among $(128/8) = 16$ inputs.
- 11.2 The dimensions are $(128 \text{ columns} * 1.3 \mu\text{m/col} * 1.1) \times (128 \text{ rows} * 1.44 \mu\text{m/row} * 1.1) = 183 \mu\text{m} \times 203 \mu\text{m}$.
- 11.3 The design with predecoding uses 16 3-input NANDs while the design without uses 128. Both designs have the same path effort. Hence, the layout of the prede-

coded design tends to be more convenient.



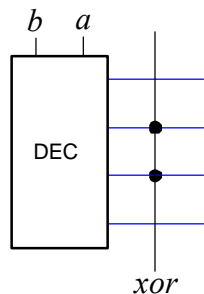
- 11.4 For unit pull-up resistance, solve $2R/P + 2R/(2P) + 2R/(4P) + 2R/(8P) = R$ to find $P = 15/4$. The logical effort is $(1 + P) / 3 = 19/12$ and the branching effort is $N/2 =$

$$3 + 5/6 + 1/3 + 5/6 = 7. D = NF^{1/N} + P = 24.8 \tau.$$

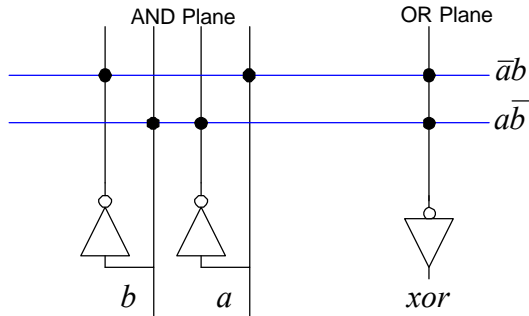
- 11.6 Design the footless domino decoder from Exercise 11.5(b) using self-resetting domino gates. Assume the inputs are available in true and complementary form as pulses with a duration of 3 FO4 inverters and can each drive 48λ of gate width. Indicate transistor sizes and estimate the delay of the decoder.

- 11.7 $H = 2^m$. $B = 2^{n-1}$ because each input affects half the rows. For a conservative estimate, assume that the decoder consists of an n -input NAND gate followed by a string of inverters. The path logical effort is thus $G = (n+2)/3$, so the path effort is $F = GBH = 2^{n+m}(n+2)/6$. The best number of stages is $N = \log_4 F \sim (n+m)/2$. The parasitic delay of the n -input NAND and $N-1$ inverters is $P = n + (N-1)$. Hence, the path delay can be estimated as $D = ((n+m)/2) (2^{n+m}(n+2)/6)^{2/(n+m)} + n + (N-1)$
- 11.8 In an open bitline, the sense amplifier compares the voltage on a bitline from the active subarray to the voltage on a bitline from a quiescent subarray. Power supply noise between subarrays makes sensing a small swing impossible. In a closed bitline, the two sense amplifier inputs come from bitlines in the same subarray, but only one of the two is activated. This design requires somewhat more layout area but eliminates most supply noise problems. It is still sensitive to coupling that affects one sense amplifier input more than the other. Twisted bitlines route the folded bitlines in such a way that each one sees exactly the same coupling capacitances, hence making coupling noise common mode as well. This is necessary in modern DRAM designs and costs slightly more area to perform the twists.

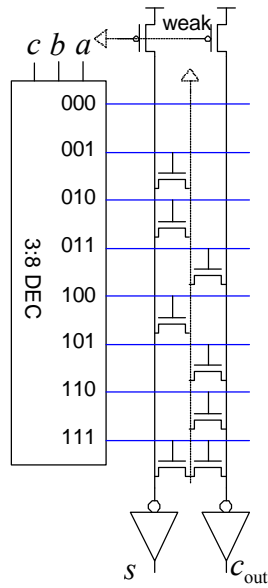
11.9



11.10



11.11



11.12 NAND ROMs use series rather than parallel transistors and one-cold rather than one-hot wordlines. They tend to be smaller than NOR ROMs because they do not require contacts between the series transistors, but they are also slower because of the series transistors.

11.13 The ROM cell is smaller than the SRAM cell. It presents one unit of capacitance for the transistor. Assume the wire capacitance is $1/2$ as much, so each cell presents $1.5C$ on the wordline. It has only a single transistor in the pull-down path on the bitline so the resistance is R . Hence, the logical effort is $1/2$, as compared to 2 for the SRAM cell.

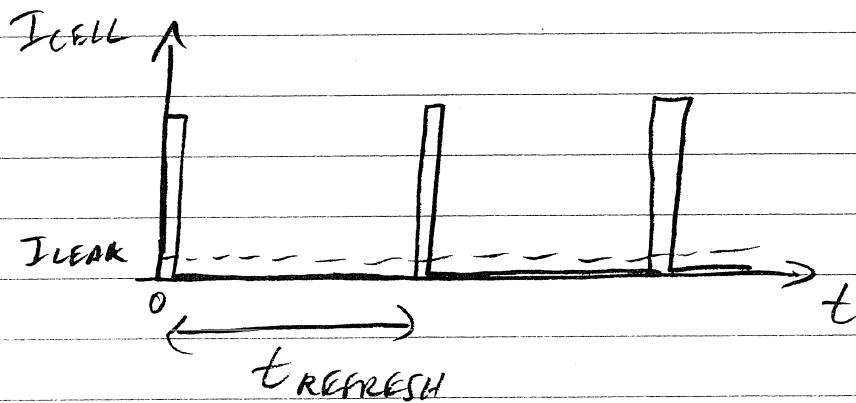
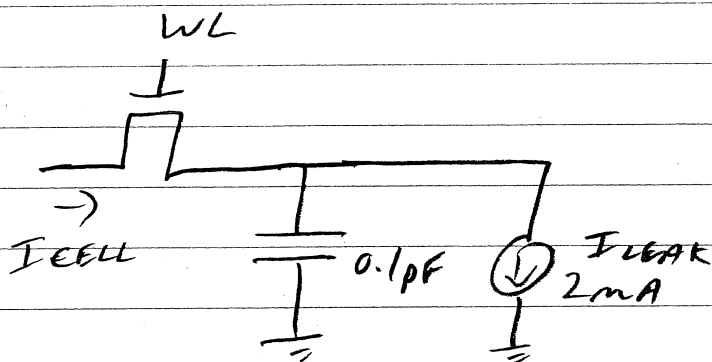
Q1)

a) Δt IS TIME TO DELAY TO $\frac{V_{DD}}{2}$

$$\Delta t = \frac{C \Delta V}{I_{LEAK}} = \frac{(0.1 e^{-12})(1.5)}{(2 e^{-9})} = 75 \mu s$$

$$t_{REFRESH} < \underline{\underline{75 \mu s}}$$

b)



$$I_{CELL-AVE} = I_{LEAK} = 2 \text{ mA}$$

$$P_{DISS} = (3V) (I_{CELL-AVE}) (2^{28}) = \underline{\underline{1.61 \text{ W}}}$$

Q2)

a)

$$\frac{W_1}{W_3} = \frac{(V_{DD} - V_A - V_{TN})^2}{2 \left[(V_{DD} - V_{TN}) V_A - \frac{V_A^2}{2} \right]}$$

$$2 = \frac{(2.1 - V_A)^2}{2 \left[(2.1) V_A - \frac{V_A^2}{2} \right]} = \frac{(2.1 - V_A)^2}{4.2 V_A - V_A^2}$$

$$8.4 V_A - 2 V_A^2 = 4.41 - 4.2 V_A + V_A^2$$

$$3 V_A^2 - 12.6 V_A + 4.41 = 0$$

$$V_A = \underline{\underline{0.39}} \quad \text{OR} \quad \cancel{3.81}$$

$$\begin{aligned} \text{b) } C_{WL} &= 256 \times 2 \times C_{ox} \times (0.5 \mu\text{m}) \times (0.25 \mu\text{m}) \\ &= \underline{\underline{384 \text{ fF}}} \end{aligned}$$

c) LAST INVERTER INPUT CAP SHOULD
EQUAL $\frac{C_{WL}}{A} = 96 \text{ fF}$

ASSUME $W_P = 2W_N$ $L_P = L_N = 0.25 \mu\text{m}$

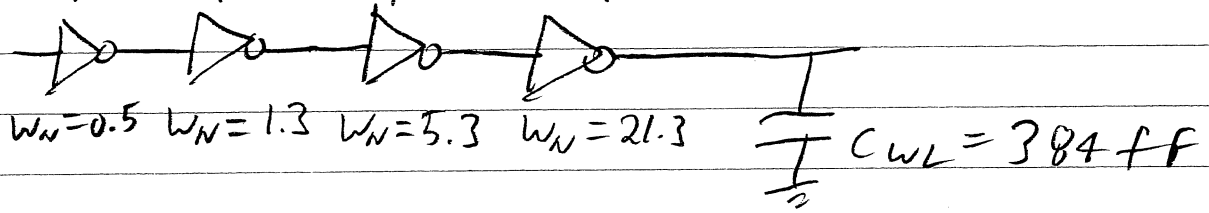
$$C_{IN} = 3 \times W_N \times L_N \times C_{ox} = 96 \text{ fF}$$

$$W_N = 21.3 \mu\text{m} \quad W_P = 42.7 \mu\text{m}$$

Q2

c) CONT'D

$$\omega_p = 1.0 \quad \omega_p = 2.6 \quad \omega_p = 10.6 \quad \omega_p = 42.7$$



Q3)

a) $L_{min} = 0.25 \mu m$

$$\frac{W_1}{W_3} = \frac{(V_{DD} - V_A - V_{EN})^2}{2 \left[(V_{DD} - V_{EN}) V_A - \frac{V_A^2}{2} \right]}$$

$$= \frac{(2.5 - 0.4 - 0.4)^2}{2 \left[(2.5 - 0.4) 0.4 - \frac{0.4^2}{2} \right]}$$

$$= 1.9$$

$$W_3 = L_{min}$$

$$W_1 = 1.9 L_{min}$$

$$W_3 = \underline{\underline{0.25 \mu m}}$$

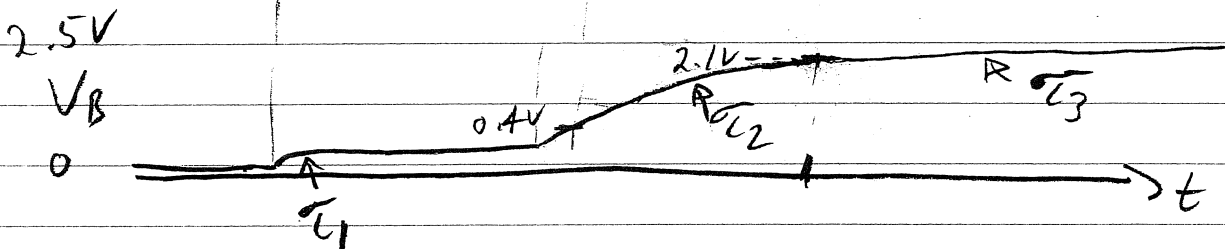
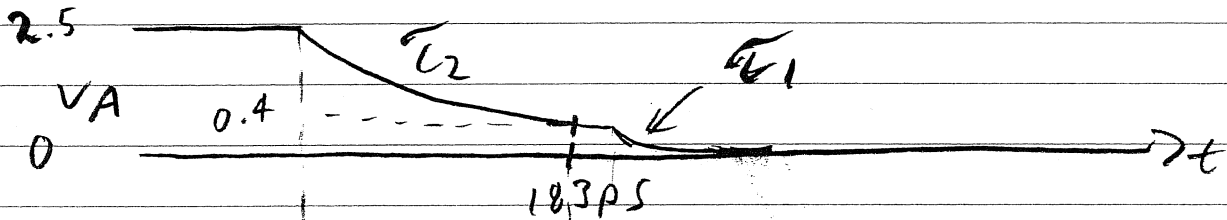
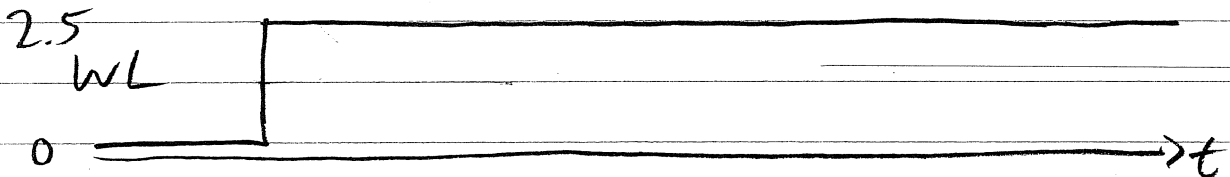
$$W_1 = \underline{\underline{0.48 \mu m}}$$

Q3 b)

$$\tau_1 = (1k)(10fF) = 10ps$$

$$\tau_2 = (10k)(10fF) = 100ps$$

$$\tau_3 = (100k)(10fF) = 1ms$$



$$2.5e^{-t/\tau_2} = 0.4 \Rightarrow t = 183ps$$