University of Toronto

Term Test 1

Date - Feb 11, 2009

Duration: 7:15pm - 9pm

ECE334 — Digital Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Assume the parameters on the parameter sheet (last page) unless otherwise stated (mosfets are from a 0.25um CMOS technology)

2. Single handwritten aid sheet allowed.

3. Only tests written in pen will be considered for a re-mark.

4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: _SOLUTIONS_

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

(T) F   CMOS microchips typically consist of both PMOS and NMOS transistors

T (F)   The "C" in CMOS stands for Complete

(T) F   A 2-input NOR gate is designed to have the same worst-case rise and fall times. The best-case fall time is smaller than the best-case rise time in this gate.

(T) F   The Body effect causes the threshold of an NMOS transistor to decrease when the V_{SB} is decreased.

T (F)   A chain of identical minimum sized inverters can achieve an overall delay smaller than that of a single minimum sized inverter assuming both drive the same load capacitance.

(T) F   A chain of three inverters has a total delay equal to the sum of delays of its individual inverters in the same chain.

T (F)   Two NMOS transistors in series with their gates both tied to V_{DD} can pull the source of the bottom transitor up to but not exceeding $V_{DD} - 2V_{tn}$.

(T) F   For the same driving capability, a two-input NAND gate has a smaller layout than a two-input NOR gate.

T (F)   The capacitance of a reversed biased junction increases as the reverse bias voltage is increased.

T (F)   Velocity saturation is more common in modern technologies as a result of the very thin gate oxide.

[6] Question 2:

$$V_{DD} = 2\,\text{V}$$

V_{in} V_{out} $\left(\dfrac{W}{L}\right)_n$
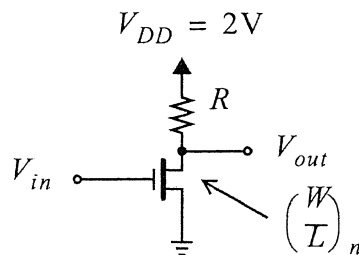
$$R = 1.8\,k\Omega$$

$$\left(\dfrac{W}{L}\right)_n = 27.8$$

Consider the RTL inverter shown above. Using the transistor values on the last page, find values for R and $\left(\dfrac{W}{L}\right)_n$ such that the logic low output value, $V_{OL} = 0.2\,\text{V}$ and the average power dissipated by the inverter, $P_{\text{diss}} = 1\,\text{mW}$ when the output has an equal probability of being either high or low. Ignore any capacitance in this question.

$$I_{DD\_AVE} = \frac{I_{DD\_H} + I_{DD\_L}}{2} \quad (\text{AVERAGE } I_{DD})$$

$$P_{DISS} = V_{DD}\, I_{DD\_AVE} \Rightarrow I_{DD\_AVE} = \frac{1\,mW}{2V} = 0.5\,mA$$

$$I_{DD\_H} = 0 \Rightarrow I_{DD\_L} = 2\, I_{DD\_AVE} = 1\,mA$$

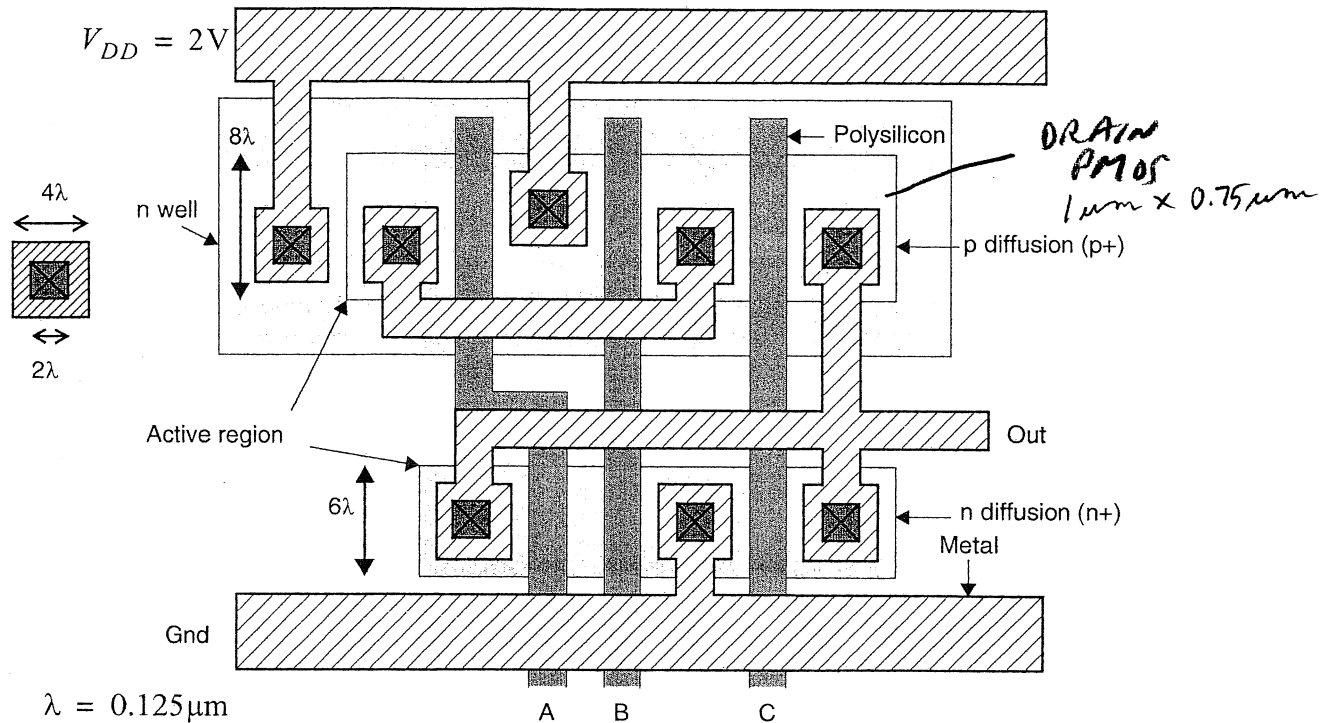$$I_{DD\_L} = \frac{V_{DD} - V_{OL}}{R} \Rightarrow R = \frac{1.8V}{1\,mA} = 1.8\,k\Omega$$

$$I_{DN} = \mu_N C_{ox} \left(\frac{W}{L}\right)_N \left((V_{GS} - V_{tN})V_{DS} - \frac{V_{DS}^2}{2}\right) = I_{DD\_L}$$

$$\left(\frac{W}{L}\right)_N = \frac{I_{DN}}{(\mu_N C_{ox})\left((V_{GS} - V_{tN})V_{DS} - \frac{V_{DS}^2}{2}\right)}$$

$$= \frac{1\,mA}{(120\,e-6)\left[(2 - 0.4)(0.2) - \frac{0.2^2}{2}\right]}$$

$$= 27.8$$

[6] Question 3:

$V_{DD} = 2\,V$

4λ ←→

2λ ↕

8λ

n well

Active region

6λ

Gnd

Polysilicon

DRAIN PMOS

$1\mu m \times 0.75\mu m$

p diffusion (p+)

Out

n diffusion (n+)

Metal

A   B   C

$\lambda = 0.125\mu m$
All transistor lengths are 2λ

a) Find the input capacitance of the input C (include overlap capacitance but no Miller effect)

$$W_N = 6\lambda = 0.75\,\mu m$$
$$L_N = 2\lambda = 0.25\,\mu m$$
$$W_P = 8\lambda = 1\,\mu m$$
$$L_P = 2\lambda = 0.25\,\mu m$$

$$C_{ox} = 6\,fF/(\mu m)^2$$
$$C_0 = 0.3\,fF/\mu m$$

$$\boxed{C_{in\_C} = 3.68}$$

$$C_{IN\_C} = C_{ox}\left[(1 \times 0.25) + (0.75 \times 0.25)\right]$$
$$+ C_0\left[(2 \times 1) + (2 \times 0.75)\right]$$

$$C_{IN\_C} = 2.625 + 1.05 = 3.68\,fF$$

Question 1 (continued)

b) Identify on the layout above the drain of the PMOS connected to the output and find the output capacitance due to this drain when the output equals 2V.

$$C_j = 2 \ fF/(\mu m)^2 \qquad \lambda = 0.125 \ \mu m$$

$$\boxed{C_{dp} = 2.4 \ fF}$$

$$C_{jsw} = 0.3 \ fF/\mu m$$

$$C_{jswg} = 0.15 \ fF/\mu m$$

$$C_{dp} = C_j \left(8\lambda \times 6\lambda \right) + C_{jsw} \left(6\lambda + 6\lambda + 8\lambda \right) + C_{jswg} \left(8\lambda \right)$$

$$= 1.5 \ fF + 0.75 \ fF + 0.15 \ fF$$

$$= 2.4 \ fF$$

c) Repeat b) for the case where the output equals 0V.

$$\boxed{C_{dp} = 1.33 \ fF}$$

ALL JUNCTION CAPACITANCES

SCALE BY

$$C_j = \frac{C_j}{\left(1 + \frac{V_R}{\phi_0} \right)^{0.5}} \Rightarrow \frac{C_j}{\left(1 + \frac{2}{0.9} \right)^{0.5}} = \frac{C_j}{1.8}$$

$$C_{dp} = \frac{2.4 \ fF}{1.8} = 1.33 \ fF$$

[6] **Question 4:** Consider a CMOS inverter with $V_{DD} = 2\,V$, $\left(\dfrac{W}{L}\right)_n = 4$, $\left(\dfrac{W}{L}\right)_p = 8$ and the

output capacitance equal to $100\,fF$.

$C_L = 100\,fF$

a) Find t_{df}.

$$R_{EQN} = \frac{2.5}{\mu_N C_{ox} \left(\frac{W}{L}\right)\left(V_{DD} - V_{tn}\right)}$$

$$= 3.25\,k\Omega$$

$$\boxed{t_{df} = 0.39\,ns}$$

$$t_{df} = 1.2\,R_{EQN}\,C_L = (1.2)(3.25k)(100f)$$

$$= 0.39\,ns$$

b) For a step input voltage (with zero rise time) from 0 to V_{DD}, sketch the **current**, I_{Dn}, through the NMOS transistor vs **time**. Label the points on your sketch where the transistor is in cutoff, active and/or triode and show the current and time values at the transitions of the different regions.
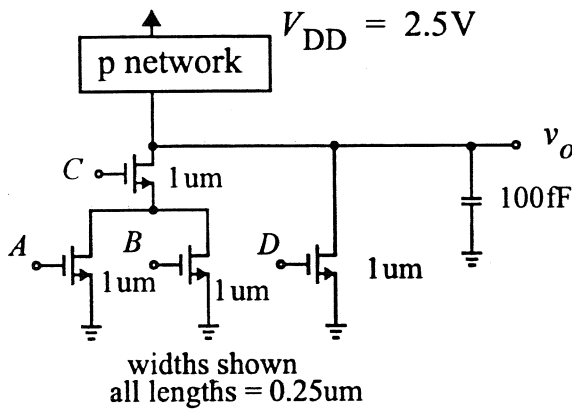

$C_L = 100\,fF$

DURING ACTIVE
CONSTANT I_{DN-SAT}

$$I_{DN-SAT} = C\frac{\Delta V}{\Delta t}$$

TRIODE

I_{DN} — ACTIVE
$614\,\mu A$
CUTOFF
0   65 PS t
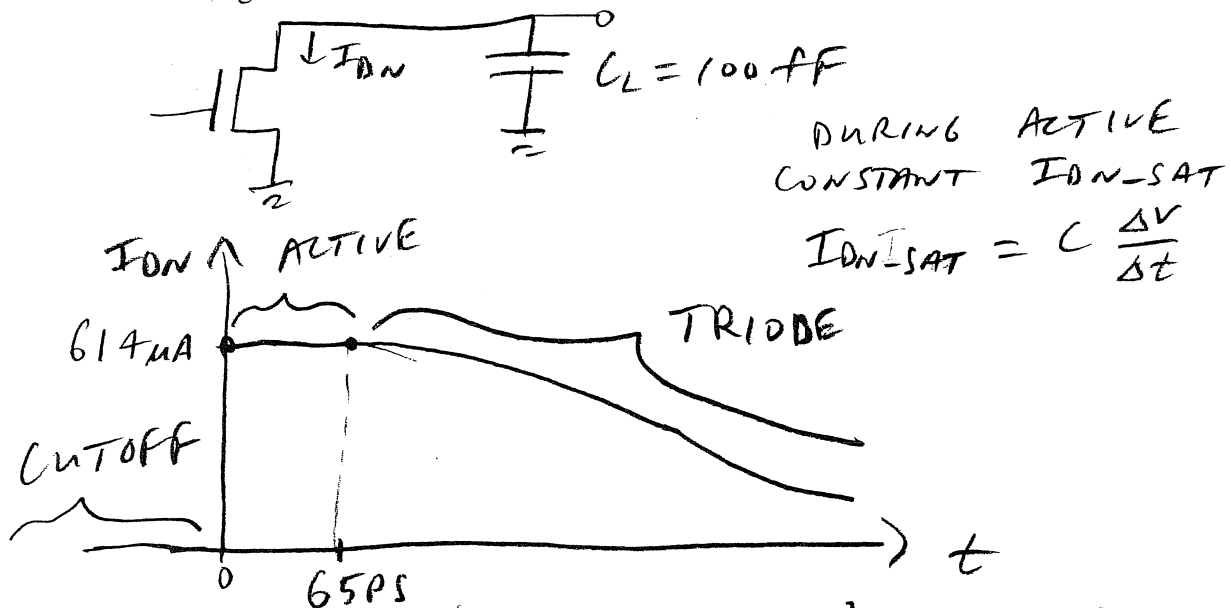
ACTIVE $I_{DN} = \left(\dfrac{\mu_N C_{ox}}{2}\right)\left(\dfrac{W}{L}\right)\left(V_{DD} - V_{tn}\right)^2 = 614\,\mu A$

LEAVES ACTIVE WHEN $\Delta V = 0.4\,V$ $V_O = V_{DD} - V_{tn}$

$$\Delta t = \frac{C\,\Delta V}{I_{DN-SAT}} = \frac{(100fF)(0.4)}{614\,\mu A} = 65\,PS$$
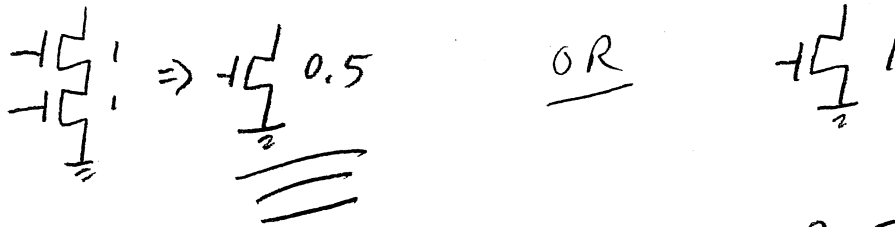
[6] Question 5: For the n portion of a complex CMOS gate shown below, find the slowest case, t_{df_slow} and fastest case, t_{df_fast} corresponding to different input patterns.

V_{DD} = 2.5V

p network

C —| 1um

A —| B 1um —| 1um D —| 1um

v_O

100fF

widths shown
all lengths = 0.25um

$$t_{df\_slow} = 600\ ps$$

$$t_{df\_fast} = 178\ ps$$

$\underline{t_{df\_SLOW}}$ EITHER $C(A+B)=1$ OR $D=1$
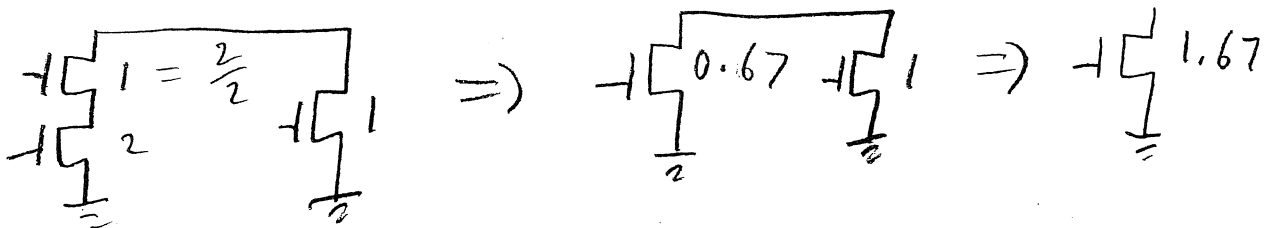
—| 1 —| 1 $\Rightarrow$ —| 0.5   OR   —| 1/2

$C(A+B)=1$ IS SLOWER $R_{EQN} = \dfrac{2.5}{(120e-6)\left(\frac{0.5}{0.25}\right)(2.5-0.4)}$

$= 5k$

$$t_{df\_SLOW} = (1.2)(5k)(100f) = 600\ ps$$

$\underline{t_{df\_FAST}}$ ALL $A=B=C=D=1$

—| $1 = \frac{2}{2}$ —| 1 $\Rightarrow$ —| 0.67 —| 1 $\Rightarrow$ —| 1.67
—| 2

$R_{EQN} = \dfrac{2.5}{(120e-6)\left(\frac{1.67}{0.25}\right)(2.1)} = 1.49\ k$

$$t_{df\_FAST} = (1.2)(1.49k)(100f) = \underline{178\ ps}$$

(blank sheet for scratch calculations)

ECE334F   Digital Electronics   Parameter Sheet

Physical Constants;

$\phi_T = kT/q = 26\text{mV (at 300K)}; \quad k = 1.38 \times 10^{-23} \text{ J/K}; \quad T = 300 \text{ K (at } 27°C); \quad q = 1.6 \times 10^{-19} \text{ C};$

$\varepsilon_o = 8.854 \times 10^{-12} F/\text{m}; \quad k_{ox} = 3.9; \quad \phi_s = 2|\phi_F| = 0.6V$

MOS Transistor; CMOS basic parameters. Channel length $= 0.25\mu m$, $m_j = 0.5$, $\phi_o = 0.9V$

	V_{T0} (V)	γ ($V^{0.5}$)	μC_{ox} ($\mu A/V^2$)	λ (V^{-1})	C_{ox} ($fF/\mu m^2$)	C_o ($fF/\mu m$)	C_j ($fF/\mu m^2$)	C_{jsw} ($fF/\mu m$)
NMOS	0.4	0.4	120	0.06	6	0.3	2	(see below)
PMOS	-0.4	0.4	30	0.1	6	0.3	2	(see below)

V_{T0} is the threshold voltage with zero bulk-source voltage.

γ is used to account for non-zero bulk-source voltage.

μC_{ox} is the transistor current gain parameter.

λ is to account for the transistor finite output impedance (channel length modulation).

C_{ox} is the gate capacitance per unit area.

C_o is the gate overlap capacitance per unit length.

C_j is the drain/source junction capacitance per unit area.

C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters **except under the gate**.

$C_{jsw} = 0.3 \, fF/\mu m$ for both NMOS and PMOS

C_{jswg} is the drain/sourc junction capacitance per unit length under the gate.

$C_{jswg} = 0.15 \, fF/\mu m$ for both NMOS and PMOS