University of Toronto

Term Test 1

Date - Feb 9, 2011

Duration: 1.5 hrs

ECE334 — Digital Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Equation sheet is on last page of test.

2. Only tests written in pen will be considered for a re-mark.

3. Calculator type unrestricted

4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

<table>
<thead>
<tr>
<th>Question</th>
<th>Mark</th>
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(last grade = 29)
[5] **Question 1:** Each correct answer is worth 0.5 marks.

For the questions below, circle one of True [T] or False [F].

- **T** F The capacitance of a reverse biased junction increases as the reverse bias voltage is increased.
- **T** F The output of a CMOS tri-state inverter is one of $V_{DD}$, $V_{DD}/2$, or 0.
- **T** F $C_{ox}$ is inversely proportional to the gate oxide thickness.
- **T** F Channel length modulation is generally important in analog circuits but not usually important in digital circuits.

For the questions below, consider the gate delay for a chain of identical CMOS inverters and only one parameter is changed. Circle one of “increase”, “unchanged” or “decrease” that corresponds to the new gate delay:

- **increase** unchanged decrease $C_{ox}$ is increased by 10%
- increase unchanged **decrease** $V_{DD}$ is increased by 10%
- increase unchanged decrease The widths of all transistors are increased by 10%
- **increase** unchanged decrease $|V_{tn}|$ and $|V_{tp}|$ are both increased by 10%
- **increase** unchanged decrease Temperature is increased by 10%
- increase unchanged **decrease** Electron and hole mobility are both increased by 10%
[6] **Question 2:** Consider the layout of 2 nmos transistors as shown below and use CMOS parameters on the equation sheet (last page).

\[ \lambda = 0.125 \mu m \]

\[ J_1 \quad \bar{\ldots} \quad J_3 \quad \bar{\ldots} \quad J_2 \]

\[ Q_1 \quad Q_2 \]

\[ J_1 \quad 10\lambda \quad J_3 \quad 10\lambda \]

\[ J_2 \quad 10\lambda \]

\[ \begin{array}{c}
J_1 \\
Q_1 \\
J_3 \\
Q_2 \\
J_2 \\
\end{array} \]

\[ \lambda = 0.125 \mu m \]

a) Find the input capacitance for the gate of a single transistor (ignore overlap capacitance).

\[ C_g = C_{oX} W L = (6)(10\lambda)(2\lambda) = (6)(1.25)(0.25) = 1.875 \text{ \mu F} \]

b) Find the overlap capacitance for the gate of \( Q_2 \) to junction \( J_2 \).

\[ C_{g\text{ov}} = C_o W = (0.3)(1.25) = 0.375 \text{ \mu F} \]

c) Find the drain-bulk capacitance at \( J_3 \) (using both area and sidewall capacitance).

\[ C_{dB} = C_j A_B + C_{jsw} \rho_B = (2)(1.25)(0.25) + (0.3)(2)(1.25 + 0.25) \]

\[ = 0.625 + 0.9 = 1.525 \text{ \mu F} \]

d) Find the drain-bulk capacitance at \( J_2 \) (using both area and sidewall capacitance).

\[ C_{dB} = C_j A_B + C_{jsw} \rho_B \]

\[ C_j A_B = (2)[(1.25)(0.25) + (0.375)(0.5)] = 1 \text{ \mu F} \]

\[ C_{jsw} \rho_B = (0.3)[10\lambda + 4\lambda + 6\lambda + 6\lambda + 4\lambda] = (0.3)(30\lambda) \]

\[ = (0.3)(3.75) = 1.125 \text{ \mu F} \]

\[ C_{dB} = 1 + 1.125 = 2.125 \text{ \mu F} \]
[6] **Question 3**: Consider the pass transistor logic shown below where $V_W$ is the input and $V_Z$ is the output. Use CMOS parameters on equation sheet (last page).

\[ V_W \rightarrow V_X \rightarrow V_Y \rightarrow V_Z \]

\[ V_{DD} = 2.5 \quad W = 1 \mu m \quad L = 0.25 \mu m \]

a) When $V_W$ is initially 0V and then goes to $V_{DD}$, find the final voltage values at $V_X$, $V_Y$, and $V_Z$.

\[ V_X = V_{DD} = 2.5 \text{V} \]

\[ V_Y = V_{DD} - V_{tn} = 2.5 - 0.4 = 2.1 \text{V} \]

\[ V_Z = V_{DD} - V_{tn} = 2.1 \text{V} \]

b) When $V_W$ is initially $V_{DD}$ and then goes to 0V, find the final voltage values at $V_X$, $V_Y$, and $V_Z$.

\[ V_X = 0 - V_{tp} = 0.4 \text{V} \]

\[ V_Y = V_X = 0.4 \text{V} \]

\[ V_Z = V_Y = 0.4 \text{V} \]
[6] Question 4: Using the concept of equivalent transistors, simplify the n-channel driver network shown below to a single pull-down transistor with a width of $W_n$ (all lengths are same and minimum). Find this equivalent transistor for 2 cases: $W_{n(\text{fast})}$ representing the input pattern with the fastest pull-down and $W_{n(\text{slow})}$ for the slowest pull-down input case.

\[ W_{n(\text{fast})} = \frac{14}{10} = 1.4 \]
\[ W_{n(\text{slow})} = 0.5 \]

(only widths shown, all length are minimum)

\[
W_{n(\text{fast})} \quad \text{ALL} \quad A - E \quad \text{HIGH}
\]
\[
\begin{align*}
\frac{1}{2} & \quad 6 = \frac{6}{1} \\
2 & = \frac{6}{5} \\
1 & = \frac{6}{6}
\end{align*}
\]
\[
\Rightarrow \quad \frac{1}{2} \quad \frac{6}{10} \quad \Rightarrow \quad \frac{11}{10}
\]

\[
W_{n(\text{slow})} \quad \text{EITHER} \quad A \quad \text{HIGH} \quad \text{OR} \quad B \quad C \quad A \quad \text{HIGH}
\]
\[
\begin{align*}
B & = \frac{4}{1} \\
2 & = \frac{4}{2} \\
1 & = \frac{4}{4}
\end{align*}
\]
\[
\Rightarrow \quad \frac{1}{7} \quad \frac{4}{7} \quad \Rightarrow \quad \frac{1}{0.5}
\]

\[
\text{since} \quad 0.5 < \frac{4}{7}
\]
\[
W_{n(\text{slow})} = 0.5
\]
[6] **Question 5:** Consider the following inverter circuit. Assume the current source is ideal until the voltage across it is 1mV at which point it linearly drops to 0mA at 0V across it. Use CMOS parameters on equation sheet (last page).

\[ V_{DD} = 2V \]

\[ I_{ON} = \frac{MN \cdot V_{GO}}{L} \left( V_{OL}^2 - \frac{V_{OS}^2}{2} \right) \]

\[ I_{ON} = 500 \mu A \]

\[ V_{OL} = 2V \]

\[ V_{ON} = 2V \]

\[ V_{OL} = 10 \]

\[ V_{OS} = V_{OL} \]

\[ 500 \mu A = (120 e^{-6})(10) \left( (2-0.4) V_{OL} - \frac{V_{OL}^2}{2} \right) \]

\[ 0.4167 = 1.6 V_{OL} - \frac{V_{OL}^2}{2} \]

\[ V_{OL}^2 - 3.2 V_{OL} + 0.833 = 0 \]

\[ V_{OL} = 2.91 \] or \[ 0.286 V \]

\[ V_{OL} = 0.29 V \]
ECE334  Digital Electronics  Equation Sheet

Constants: $k = 1.38 \times 10^{-23} \text{JK}^{-1} ; q = 1.602 \times 10^{-19} \text{C} ; V_T = kT/q = 26 \text{mV at 300} \text{K} ;$ 

$e_0 = 8.85 \times 10^{-12} \text{F/m} ; \quad \kappa = 9.0$ 

caps: $C_{ox} = (\kappa \varepsilon_0) / t_{ox} ; \quad C_g = C_g/(1 + \mu_p/(\phi_o)^{1/2})$ 

NMOS: $\beta_p = \mu_p C_{ox}(W/L) ; \quad V_{th} > 0 ; V_{ds} \geq 0$ ; (triode) $I_D = \beta_n(V_{gs} - V_{th})V_{ds} - (V_{ds}^2/2)$ ; (active) $I_D = 0.5\beta_n(V_{gs} - V_{th})^2$ ;

(triode) $V_{ds} \leq (V_{gs} - V_{th})$ ; (active) $V_{ds} \geq (V_{gs} - V_{th})$ ; $I_{on} = \tau(V_{gs} - V_{th})^2/(1 - e^{V_{gs} - V_{th}})$. 

(subthreshold) $I_D = I_{ds} e^{(V_{gs} - V_{th})/V_T}$.

PMOS: $\beta_p = \mu_p C_{ox}(W/L) ; \quad V_{th} < 0 ; V_{ds} \leq 0$ ; (triode) $I_D = \beta_p(V_{gs} - V_{th})V_{ds} - (V_{ds}^2/2)$ ; (active) $I_D = 0.5\beta_p(V_{gs} - V_{th})^2$ ;

(triode) $V_{ds} \geq (V_{gs} - V_{th})$ ; (active) $V_{ds} \leq (V_{gs} - V_{th})$.

Simple cap model: $C_g = C_{ox} W L$ ; if $\kappa_{min} ; C_{gw} = C_{ox} L_{min} ; C_g = C_{gw} W$ ; $C_d = C_{gd} W$ ;

CMOS inverter: $V_{th} = (V_{dd} + V_{th} + V_{in})/(1 + r)$ ; $r = \sqrt{\mu_p C_{ox}(W/L)} / (\kappa p/(W/L))$ ;

RC delay: $t_{df} = \tau = \kappa C (V_{dd} + V_{th})$ ; $R_{eq} = 2.5 / (\mu_p C_{ox}(W/L)) (V_{dd} - V_{th})$ ; $R_{eq} = 2.5 / (\mu_p C_{ox}(W/L)) (V_{dd} + V_{th})$ ;

$C_{o} = \sqrt{V_T} \cdot \sqrt{V_T}$ ;

Unit delay: $t_{del} = t_{del} (C_{ox} / C_g) ; \quad \text{total delay} = \frac{\text{delay}}{C_{ox}}$.

Power diss: $P_{dy} = P_{in} + V_{dd} V_{dd} / 2$. $P_{dy} = 0.5 P_{in} (V_{dd} V_{dd}) / (t_{dy} + t_{cis}) ; t_{dy} = 0.5 \beta_p(V_{th} - V_{ds})^2$ ;

Elmore Delay: $t_{dy} = \sum C_{ox} R_{in} ; \quad \text{dist RC, } t_{dy} = RC/2$.

Interconnect: $R = (\rho d)/(d^2)$ ; $R = 1 / t_{dy}$ ; $C = (C_{ox} w L) / 1$ ; $C = \varepsilon_0 l w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5}$.

Max delay constraint: $t_{dy} + t_{del} + t_{setup}$ Min Delay constraint: $t_{del} = t_{dy} + t_{del}$ Metastability: $MTBF = e^{-V_{th} / (t_{dy} F_{p} C_{in})}$.

SRAM: M3 is cell access transistor, M1 is inverter NMOS, M5 is inverter PMOS,

SRAM read: $W_1 / W_2 \geq (V_{dd} - V_{th})^2 / (2(V_{dd} - V_{th}) V_{th})$ ; $I_{cell} = (C_{ox} / 2)(W_1 / L) (V_{dd} - V_{th})^2$.

$\Delta V_{BE} = (I_{cell} / V_{BE}) C_{BE}$

SRAM write: $W_1 / W_2 \geq (\mu_p (V_{dd} - V_{th})^2) / (2 \mu_p (V_{dd} - V_{th}) V_{th})^2$.

MOS Transistor: CMOS basic parameters. Channel length: $0.25 \mu m ; m_j = 0.5 ; \phi_o = 0.9 V$.

<table>
<thead>
<tr>
<th>$V_{T0}$</th>
<th>$V$</th>
<th>$\gamma$</th>
<th>$\mu C_{ox}$</th>
<th>$\lambda$</th>
<th>$C_{ox}$</th>
<th>$C_o$</th>
<th>$C_j$</th>
<th>$C_{jsw}$</th>
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<tr>
<td>(V)</td>
<td>(V)</td>
<td>(V)</td>
<td>(\mu A/V^2)</td>
<td>(V^-1)</td>
<td>(fF/\mu m^2)</td>
<td>(fF/\mu m)</td>
<td>(fF/\mu m^2)</td>
<td>(fF/\mu m)</td>
</tr>
<tr>
<td>NMOS</td>
<td>0.4</td>
<td>0.4</td>
<td>120</td>
<td>0.06</td>
<td>6</td>
<td>0.3</td>
<td>2</td>
<td>0.3</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>0.4</td>
<td>30</td>
<td>0.1</td>
<td>6</td>
<td>0.3</td>
<td>2</td>
<td>0.3</td>
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$V_{T0}$ is the threshold voltage with zero bulk-source voltage; $\gamma$ is used to account for non-zero bulk-source voltage; $\mu C_{ox}$ is the transistor current gain parameter; $\lambda$ is to account for the transistor finite output impedance (channel length modulation); $C_{ox}$ is the gate capacitance per unit area; $C_o$ is the gate overlap capacitance per unit length; $C_j$ is the drain/source junction capacitance per unit area; $C_{jsw}$ is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters.